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GALLIUM ARSENIDE PILOT LINE FOR HIGH PERFORMANCE COMPONENTS

Contract No. F29601-87-C-0202

Final Report

May 28, 1992

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1.0 OVERVIEW (S. F. Nygren)

This contract for a Gallium Arsenide Pilot Line for High Performance Components was awarded to AT&T in March, 1987. As this was the third in a series of GaAs pilot lines sponsored by DARPA, we referred to this contract as Pilot Line III. The program goal was to develop a complete facility for fabricating GaAs memory and logic chips. To meet this goal, we provided a "User-Friendly" CAD system, a self-aligned GaAs E/D heterostructure FET technology, and a facility for fabricating GaAs circuits on 3" wafers. We designed and fabricated several process tester circuits, two 4K SRAMs and six 3000-5000 gate logic circuits. All circuits met the design target for speed: 200 MHz memory operation and logic circuits that operated at 200 MHz for 15-20 gate delays. To support this technology, we surveyed the industry for available high-pin-count high-speed packages, and we assembled our circuits into the most suitable available packages. We also characterized the radiation hardness and reliability of these circuits. Finally, in addition to this basic technology, we developed an advanced technology whose circuits operated at 400 MHz, and we investigated its manufacturing feasibility. This Final Report describes the accomplishments of the program. Besides this overview, the Report is divided into four sections: Circuit Designs, Design Tools, and Test Results; Pilot Production and Process Development; Radiation Hardness and Reliability; and Lessons Learned During the Contract. Also, there are four appendices: the Pilot Line III Design Rules, Process Control Modules, the Advanced Technology, and the Industry Survey of Available High-Speed Packages.

To achieve the goals of this program, we proceeded along two parallel paths that had to converge for the program to be successful. First, the basic LSI technology (including Molecular Beam Epitaxy support (MBE)) had to be developed and demonstrated. Second, suitable GaAs heterostructure design models had to be developed. For this to happen in an orderly way, we devised a series of process testers. Masksets PT-0, PT-1, PT-2L, and PT-2M provided increasingly complex stepping stones toward the full size circuits required by the contract. PT-0 wafers contained FETs from which we developed our initial models, and the PT-1 and PT-2 wafers contained small circuits to demonstrate 256-bit SRAMs and the three required logic design styles (full custom, standard cell, and cell array).

The program unfolded in three phases. At first, using preliminary design models and early MBE structures, we used PT-0, PT-1, PT-2L, and the standard cell Casino Test Chip[1] as vehicles for developing our wafer fab process and improving our design models. In this phase we demonstrated that 1) our design tools and design rule checker were capable of producing functioning circuits without layout errors, 2) the design models worked well enough to produce functioning circuits that easily met the speed requirements, 3) MBE structures could be routinely grown in a manufacturing environment, and 4) our wafer fab process was capable of producing acceptable circuit yields with 2μm interconnect lines and spaces and 1μm gate lengths. These things were accomplished in spite of the noticeable differences between the design models and the actual FET characteristics.

In the second phase, an improved design model included best and worst case noise margin models and information for both 25 and 125°C. While the models still weren't identical to the FET characteristics, they were much better. Moreover, MBE improvements placed the FET characteristics close to target, especially at the end of this phase. Our objectives were to demonstrate the functionality of full-size circuits (the custom and standard cell ALUs and the standard cell transversal filter), to prove in the cell array methodology (1000-gate cell array), and to explore the detailed characteristics of the 256-bit PT-2M SRAM in preparation for designing the full-size 4K SRAM. All these circuits were fully functional, and they satisfied our objectives. They also provided measured input/output voltage charactristics for use in designing circuits for the final phase.

---

[1] The Casino program was set up to provide a GaAs demonstration system for the Advanced On-Board Signal Processor (AOSP). The Casino Test Chip was designed to test various AOSP concepts.

In the final phase, we had an MBE structure that gave on-target FETs and a design model that matched it. We designed and fabricated five circuits to demonstrate the capability of the final version of our technology: 4K SRAMs I and II, a custom 32-Bit multiplier, a cell array Casino Test Chip (CA-CTC), and a supercomputer test chip. The multiplier and the supercomputer test chip are the best examples of the capability of our technology. 4K SRAM I was not expected to work over the full temperature range; and 4K SRAM II, which was designed to work from -55 to 125°C, failed to function due to a design flaw unrelated to the wider intended temperature range. The CA-CTC, our largest chip (11 mm square) had too few functional circuits for adequate characterization.

The 32-Bit Multiplier, with 6500 gates, was fully functional from -55 to 125°C on a 2V power supply. With 70 gates in its critical path, it functioned at about 100 MHz, equivalent to over 300 MHz with 20 gates in the critical path. It generally satisfies the I/O voltage requirements except for some degradation above 80°C and a V_{ol} that is slightly high. The supercomputer test chip was a speciality chip designed to demonstrate the use of GaAs in supercomputer applications. The emphasis was on speed and minimum power-delay product. We achieved 12% functional yield of 8.1 mm square chips. The average delay for a NOR gate was 193 ps, with a power-delay product of 158 fJ.

The memory program relied heavily on the PT-2M SRAM. It offered a relatively high yield of fully functional circuits to study design issues and yield limiters like shorts through the dielectric that is supposed to isolate power from ground. The PT-2M SRAM satisfied all design requirements except that its temperature range was only 0 - 80°C, instead of the required -55 to 125°C. The initial 4K SRAM was 16 times the size of the PT-2M SRAM. The initial 4K SRAM had low yield, but it was fully functional at 40°C and 50 MHz, and it satisfied the power supply and I/O voltage criteria at that temperature and speed. A second iteration 4K SRAM was designed to operate at 200 MHz over a wider temperature range. The intent was to do this by using a design that did a better job of turning off the wordline access transistors. Unfortunately, the second iteration was not functional; FETs with twice the normal gate length failed to perform as expected.

The full size logic circuits included both a custom and a standard cell ALU, a standard cell and a cell array Casino Test Chip, a standard cell Transversal Filter Chip, and a custom 32-Bit Multiplier. Except for the standard cell Casino Test Chip, all these circuits were fully functional in their initial designs. All subcircuits of the standard cell Casino Test Chip worked on at least one chip, but no single chip was fully functional. This was not surprising since this circuit was designed during phase one of the program, before the design models adequately represented the actual FETs. In general, the circuits worked from -55 to 125°C, from V_{DD} = 1.8 to 2.2 V, and at the equivalent of 200 MHz for 20 gate delays, all as required, although few chips could achieve all these criteria simultaneously. The main shortcoming was that the chips could not consistently comply with the I/O voltage requirements, although the multiplier of phase 3 came quite close.

HCAD, the "User-Friendly" CAD System developed for this program, supports full custom, macrocell (standard cell), and gate array styles of layout. There are 45 elements in the macrocell library and 30 elements in the gate array library. The gate array floorplan will support designs with up to 3500 used gates. The capabilities of HCAD were demonstrated in three of the circuits designed for this program. The initial standard cell library was used in the Standard Cell Casino Test Chip. Using the macrocell library, the Standard Cell Transversal Filter Chip was deigned entirely within HCAD. Finally, the Cell Array Casino Test Chip was designed entirely within HCAD. The initial designs were fully functional for both the Transversal Filter Chip and the Cell Array Casino Test Chip. The custom design capabilities were demonstrated on a small silicon circuit. To make HCAD "user-friendly," the development effort concentrated on achieving a consistent, predictable look and feel across all the design tools contained in HCAD.

The basic technology is a Self-Aligned Refractory-Gate Integrated Circuit process for making Heterostructure Field Effect Transistors (SARGIC-HFETs). The process uses MBE layers which are grown by our operating shop, not by engineers. During the program, the operating and maintenance procedures were refined so that we averaged only 22% downtime over the last 11 months of the program; this is very close to the calculated minimum downtime of 20%. Through process refinements, we achieved within-wafer sheet resistances that are constant within only 1.2% on average, and we reduced the average defect density to only 84 per square centimeter. Almost 1900 MBE wafers were used in wafer fab for this program.

The basic technology required development of material-selective etchants for defining enhancement- and depletion-mode FETs, a tungsten silicide refractory gate technology, an implant/anneal process that would preserve the two-dimensional electron gas integrity while allowing low source resistances, and low stress silicon oxynitride for final device passivation and for insulation between metal layers. These developments went relatively smoothly. The most difficult part of process development was to make the EFET and DFET characteristics reproducible enough to allow circuit fabrication with acceptable yields. While the circuit yields never reached 10%, the contract goal, we succeeded in achieving good FET control. For the final 16 wafer fab lots, EFET $I_{ds}(V_{gs}=0.5V)$ was 61 ± 15 mA/mm (mean ±standard deviation), and DFET $I_{ds}(V_{gs}=0.0V)$ was 85 ± 21 mA/mm. The targets are 55 mA/mm and 85 mA/mm. From the mechanical defect point of view, analysis showed we could expect a 30% yield loss due to shorts between power and ground, and a 46% yield loss due to bad vias, both in circuits the size of the 4K SRAM. Mechanical defects turned out to be the weakest link in our technology. We could produce designs which were right without any corrections being needed, and we could control FET characteristics within acceptable limits, but yields remained relatively low.

The advanced technology successfully reached its goal of 400 MHz circuits with manufacturing yields about 20 - 30% of the basic technology. This was accomplished by developing a faster implementation of the SFFL logic gate, and by developing an aluminum interconnect metallization scheme that gave good yields for 1.5μm lines and spaces.

To describe the radiation hardness of our technology, we used the PT-2M SRAM and the custom ALU. The SRAM lived up to expectations for total dose (best results = 1×10^8 rad (GaAs)), and it exceeded expectations for transient dose (best results = 1×10^{10} rad (GaAs)/sec). But the single event upset result was disappointing due to the large upset cross section for particles with large LET values and the small memory off-driver voltage (best results = 1.3×10^{-3} errors/bit day). For the ALU, the best result for total dose was the same as for the SRAM. For transient dose, the ALU was in operation while it was irradiated, and we measured the highest dose for which it would continue working. This was a much more stringent test than the SRAM received. The best ALU result was 3×10^8 rad (GaAs)/sec.

In our reliability studies, we completed two rounds of High Temperature Operating Bias (HTOB) reliability experiments with the PT-2M SRAM. This memory is known to have lower resistance to bit flipping than was intended for the second iteration of the 4K SRAM. Nevertheless, after 2000 hours of aging in the second round, this SRAM achieved reliability similar to other GaAs circuits: the maximum failure rate at 65°C over ten years is less than 1 FIT at the ten year mark.

This section concludes by putting the achievements of the program in perspective. We believe our SARGIC-HFETs are the only ones in production. Other manufacturers offer HEMTS, but they are recessed gate rather than planar. Compared to ion-implanted MESFETs without buried p-layers, SARGIC-HFETs offer sharper turn-ons and higher g_ms close to pinchoff. The sharper turn-on allows operation at a lower power supply voltage and a correspondingly lower power dissipation. Ion-implanted MESFETs can have improved turn-on sharpness by using the additional complication of a buried p-layer. They can also get the same current as an HFET by using smaller devices and shorter interconnects than are required for HFETs; alternatively, they could use increased doping and thinner layers, which makes them more like an HFET. Of course, small devices and thinner layers lead to increased difficulty in obtaining reproducibility.

Other gallium arsenide suppliers have chosen to use ion-implanted MESFETS. Vitesse uses an implanted EFET/DFET process with four levels of metal (compared to our two). With this technology, they have achieved much higher gate counts than we produced in this program. TriQuint also has an implanted EFET/DFET process. But we have found that there are substantial performance advantages with our EFET/DFET HFETs. Using SARGIC-HFETs, AT&T

manufactures a preamplifier for use in lightwave applications. Compared to MBE-based recessed gate MESFETs, the HFETs have higher f_Ts for a given gate length, and they have lower noise figures. The use of SARGIC-HFETs makes this a manufacturable circuit; we had poor performance and yields with MESFETS. Building on this success, AT&T now also has EFET-only and DFET-only versions of the SARGIC-HFET technology.

In MBE, we don't have enough data to make a meaningful comparison to other manufacturers. We grew several thousand MBE wafers during this program, and we have meaningful statistics about reproducibility based on FET device results. For the final 16 wafer lots of this program, we grew 96 MBE wafers under as identical conditions as possible. We achieved DFET I_{ds} of 85 mA/mm ± 21 mA/mm (mean ± sigma) and EFET I_{ds} = 61 mA/mm ± 15 mA/mm. Although these data represent MBE uniformity convoluted with processing uniformity, they show a reasonably good yield; about 51% of these wafers passed our wafer screening tests. For comparison, we sampled MBE wafers provided by Picogiga. Some of their wafers had the required doping and thickness, and others did not; we didn't purchase enough to develop any meaningful statistics. It was our impression that most of Picogiga's customers are less demanding on thickness control than we are. Their customers mostly make recessed gate FETs, so they use an extra processing step to compensate for layer thickness variations.

HCAD, our "User-Friendly" CAD system, was the result of some pioneering work using a framework system for producing a consistent user interface and for integrating tools from various vendors. It proved competent at designing custom, standard cell, and cell array circuits. HCAD was completed two years ago. Since that time, commercial vendors have developed a second generation framework, and the other tools have two years of additional development. If we were to bring HCAD up to date, we'd use these upgraded tools; we'd also probably use one of the new gate array tools that have become available, and we'd use VHDL for logic simulation. But this discussion simply indicates how rapidly software is being developed. When HCAD was developed, it served Pilot Line III well, and all three circuits designed with it worked correctly.

Finally, in testing, this program took advantage of some of the hardware that is even now just becoming available. At the beginning of this program, no commercial hardware was capable of using thousands of test vectors to characterize complex logic circuits much above 100 MHz. After Pilot Line III started, the Hewlett-Packard 82000 became available for testing such circuits at the required 200 MHz. While the 82000 doesn't run fast enough for volume manufacturing, we developed it for use in characterizing our circuits on experimental basis.

2.0 CIRCUIT DESIGNS, DESIGN TOOLS, AND TEST RESULTS

2.1 Design Strategy (H. C. Kirsch, K. W. Wyatt, C. H. Tzinis, and S. F. Nygren)

The Pilot Line III program was structured so that four key (and interdependent) elements would be developed in parallel.

1) We had to develop design-worthy heterostructure device models, starting from an existing MESFET model. Initially, we had no data for the SARGIC devices we would be building.

2) Given a manufacturing process where FET characteristics were only beginning to come into control, a standard cell library had to be developed for use in the standard cell circuits. The Standard Cell Casino Test Chip that went to mask only thirteen months after the program started.

3) An MBE heterostructure device growth technique had to be transferred from research to manufacture and then proven-in.

4) The SARGIC-HFET LSI processing technology had to be developed and demonstrated at AT&T's Reading location. Defect densities in this technology would have to be low enough to allow adequate circuit yields.

This report is organized so that Section 2 discusses all the design issues, including the modeling program, the standard cell development, and the designs of the individual circuits. Section 3 describes the wafer fab technology, including MBE.

As a guide to the circuit designs, Figure 1 shows the evolution of the various circuit families (memory, custom logic, standard cell logic, cell array logic). A series of process testers (on maskset sequence PT-X (not shown in Figure 1), PT-0, PT-1, and PT-2) was designed to study materials, processing, modeling, and design issues. PT-X contained three processing levels (metal, dielectric, metal) and was designed to test processing capabilities in structures like ohmic contacts, vias, crossovers, and capacitors. PT-0 contained our first SARGIC FETs; initial SARGIC device models were taken from PT-0 FETs. PT-1 contained small circuits to test our design capabilities, and PT-2 contained somewhat larger circuits to refine our design capabilities. The overall PT-sequence was designed to give us the data and experience needed to design the 4K SRAMs and 5000-gate logic circuits required by this contract.

Figure 2 shows the circuit evolution on a timeline, indicating the design model and the MBE type for each circuit, as well as the wafer fab intervals. The wafer fab intervals show the time between the first wafer start and the last wafer completion. There are three distinct phases within this program. First, using early models (no models through SargicS.8) and early MBE structures (prototypes through ED7), we designed and fabricated PT-0, PT-1, PT-2L, and the Standard Cell Casino Test Chip. In this phase, the design models and FET characteristics had not yet converged, and we were more interested in developing models and wafer fab processing than in outright circuit performance. Nevertheless, all the circuits were functional (except for the PT-2L memory tester, which had a mask error). Also, the circuits all exhibited propagation delays that were clearly short enough to achieve the required 200 MHz operation for 15-20 gate delays. So in this phase we demonstrated all the components we would need for the balance of the program:

- The design tools and design rule checker were capable of producing functioning circuits without layout errors.
- The design models worked well enough to produce functioning circuits that met the circuit speed requirements.
- MBE structures could be grown routinely in a manufacturing environment.
- The SARGIC-HFET process was demonstrated capable of reasonable circuit yields with 2μm interconnect lines and spaces and 1μm gates.

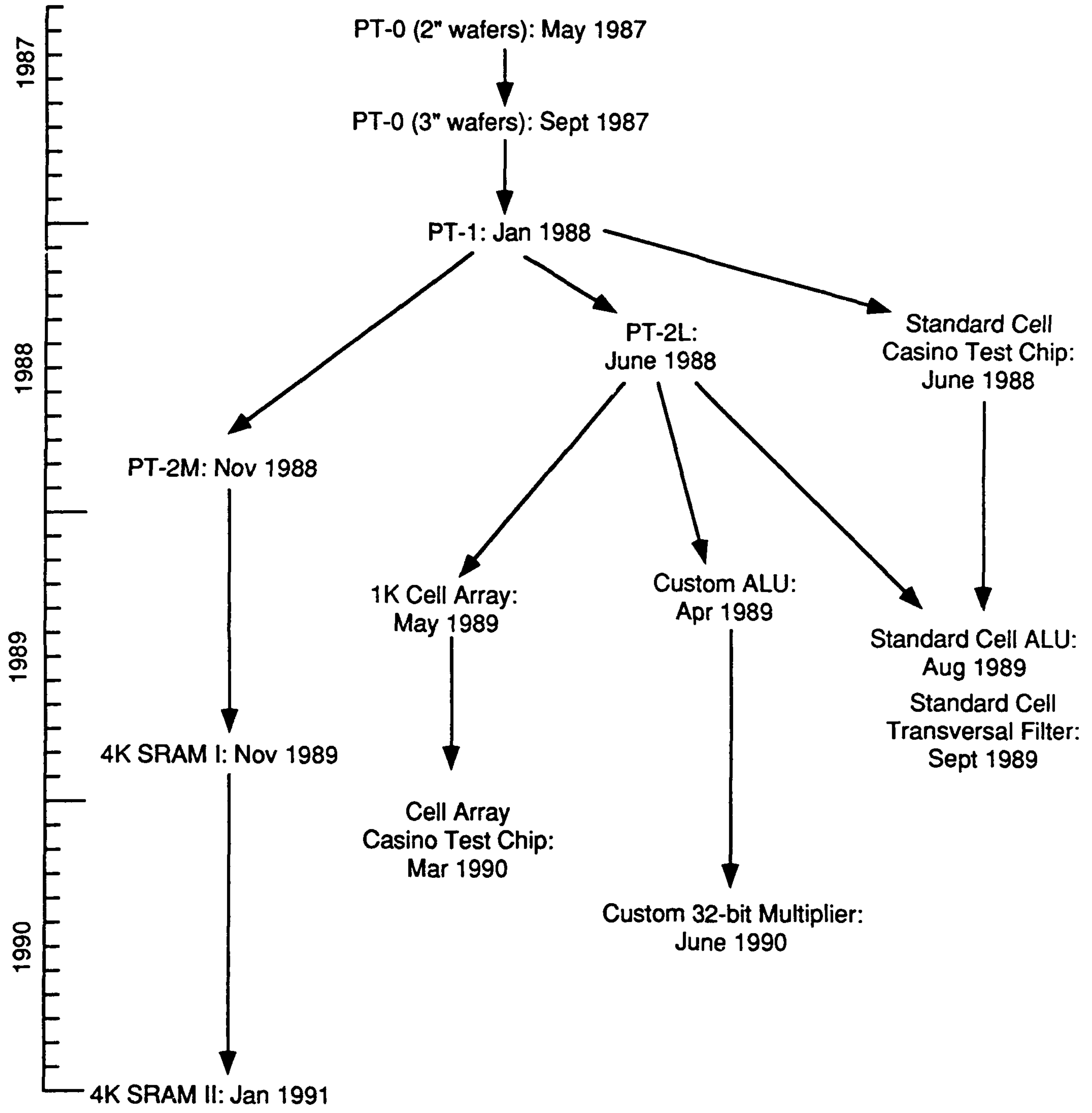

1987
1988
1989
1990
PT-0 (2" wafers): May 1987
PT-0 (3" wafers): Sept 1987
PT-1: Jan 1988
PT-2L: June 1988
Standard Cell Casino Test Chip: June 1988
PT-2M: Nov 1988
1K Cell Array: May 1989
Custom ALU: Apr 1989
Standard Cell ALU: Aug 1989
Standard Cell Transversal Filter: Sept 1989
4K SRAM I: Nov 1989
Cell Array Casino Test Chip: Mar 1990
Custom 32-bit Multiplier: June 1990
4K SRAM II: Jan 1991

Figure 1 - GaAs Pilot Line Circuit Development; Dates for Initial Wafer Fab

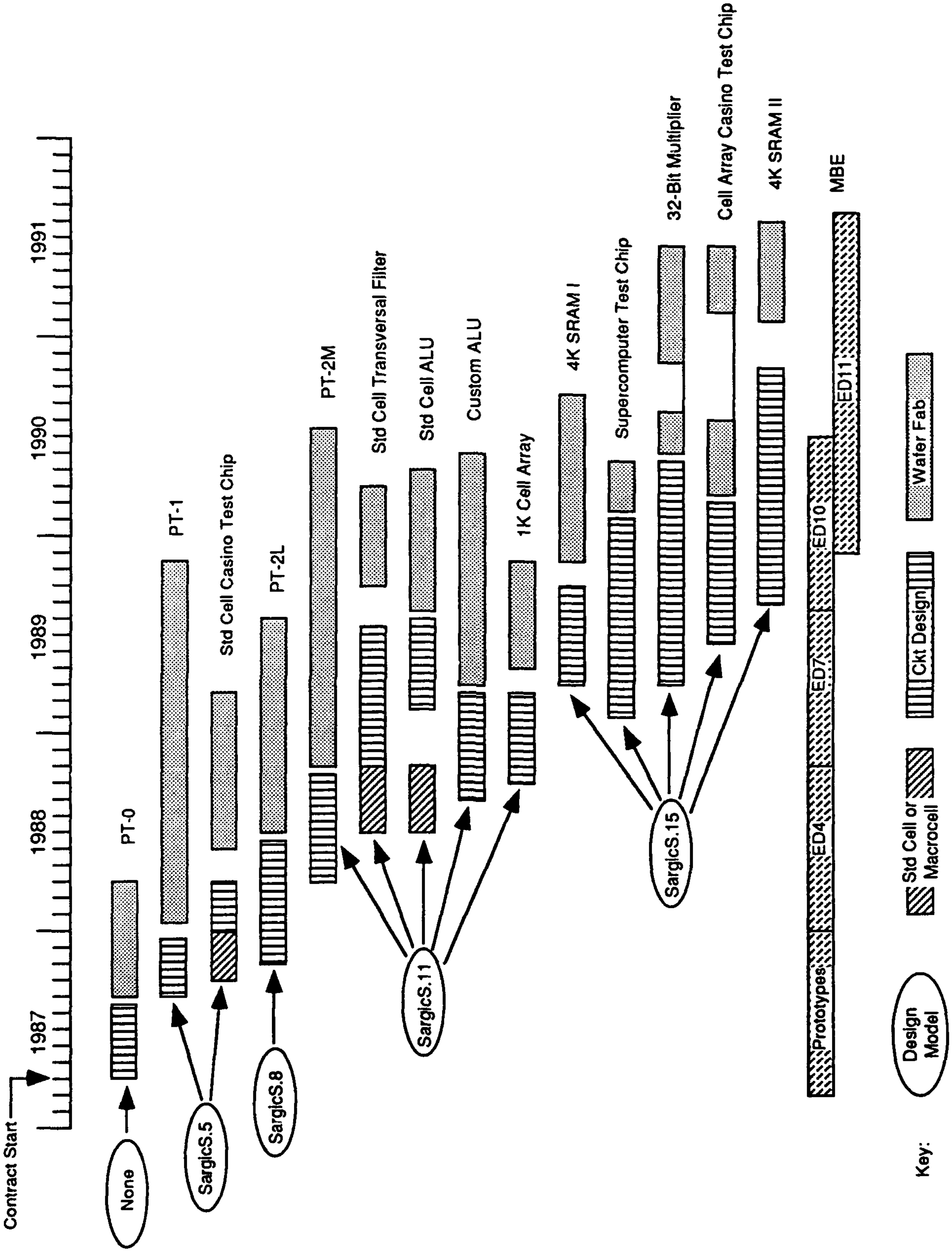


Figure 2 - MBE, Circuit Design, and Models

By the end of this phase, we had also clearly identified where further work was needed: 1) The circuit design models needed to better represent the FET characteristics so that we could better model switchpoints and logic levels. 2) The MBE structure needed to be modified to produce the target FET thresholds.

For the second phase, we had both better models and a sequence of MBE structures that ended with FETs close to target. The SargicS.11 model included best and worst case noise margin models and information for both 25 and 125°C. The initial MBE structures, ED7, gave DFETs whose thresholds were too positive, but the subsequent ED10 and especially ED11 were very close to target. During this phase we designed and fabricated the PT-2M SRAM, custom and standard cell ALUs, a standard cell Transversal Filter Chip (TFC), and a 1000-gate cell array. In these circuits, the match between design models and FET characteristics was still not perfect, so our objectives were to demonstrate functionality of full-size circuits (the ALUs and the TFC), to prove-in the cell array methodology, and to explore the detailed characteristics of the 256-bit PT-2M SRAM in preparation for designing the full-size 4K SRAM. Another important objective was to examine the I/O voltage characteristics of these circuits in preparation for designing the final circuits, where full specifications were supposed to be met from -55 to 125°C. These circuits were all fully functional, and they helped us crystallize the strategies that would be used in the final phase for design models and MBE structures.

In the final phase we had, for the first time, an MBE structure (ED11) that produced on-target FETs and a design model (SargicS.15) that matched it. The SargicS.15 model represented the culmination of a revised strategy that began with SargicS.12: Rather than have the model represent currently available FETs, so that revised MBE or processing could obsolete the model by the time circuits were actually fabricated, the model was held essentially constant and was a target for the FETs to match. This strategy worked well, and after correcting a problem with etching the EFET tubs, we concluded the program with FETs that were very close to the target set by the model. In this final phase, we designed and fabricated two iterations of a 4K SRAM, a custom 32-Bit Multiplier, a Cell Array Casino Test Chip (CA-CTC), and a supercomputer test chip. Of these, the 32-Bit Multiplier and the supercomputer test chip are the best examples of the capabilities of AT&T's SARGIC-HFET technology. The CA-CTC, our largest chip, had too few fully functional circuits for adequate characterization; 4K SRAM I was not expected to work over the full temperature range; and 4K SRAM II, which was designed to work from -55 to 125°C, failed to function due to a design flaw unrelated to the wider intended temperature range.

The 32-Bit Multiplier has 6500 gates, 70 of which are in the critical path. On a 2.0V power supply, it is fully functional from -55 to 125°C, and its speed is about 100 MHz (equivalent to 350-470 MHz for 15-20 gates in the critical path). It generally satisfies the I/O voltage requirements except for some degradation over 80°C and a V_{ol} that is slightly high.

The supercomputer test chip was a specialty chip designed to demonstrate the use of GaAs in supercomputer applications. Because it would operate at a closely controlled temperature, it was designed as DCFL (Direct Coupled FET Logic) rather than the SFFL (Source Follower FET Logic) used for all the other circuits. The objective of this circuit was to maximize speed and minimize the delay-power product. We achieved a 12% functional yield of 8.1 mm square chips. The average delay for a NOR gate was 193ps, and the average power was 0.8 mW, so the average delay-power product was 158 fJ using a 2.0V power supply.

The remainder of Section 2 discusses each individual circuit and all the design tools. Before starting that, the following paragraphs summarize in one place the key features and results for each SFFL circuit. (The DCFL supercomputer test chip is excluded from the following paragraphs. It is described in Section 2.21.) Table 1 lists the key features of each SFFL circuit.

Table 1 - Circuits Design for Pilot Line III

	STYLE	Report Section	SIZE	Chip Size (mm x mm)	First Wafer Starts	Total Number of Wafer Starts
PT-0	Custom	2.11	FETS Only		May 1987 (2") Sept. 1987 (3")	109
PT-1	Various Various	2.5	Small Logic Unclocked 256-bit SRAM		Jan. 1988	598
PT-2L	Various	2.12	364-2211 Logic Gates		Jan. 1988	198
PT-2M	Various Custom	2.6	91-283 Logic Gates Clocked 256-bit SRAM		Nov. 1988	244
1K Cell Array	Cell Array	2.19	738 Logic Gates		May 1989	58
4K SRAM I	Custom	2.7	4096-bit SRAM	5.3 x 5.3	Nov. 1989	108
4K SRAM II	Custom	2.8	4096-bit SRAM	5.3 x 5.3	Jan. 1991	48
32-Bit Multiplier	Custom	2.14	6500 Logic Gates	9.5 x 8.5	Jun. 1990	54
ALU	Custom	2.13	3571 Logic Gates	7.8 x 7.8	Apr. 1989	116
ALU	Std. Cell	2.17	3452 Logic Gates	7.7 x 7.7	Aug. 1989	42
Transversal Filter	Std. Cell	2.18	5190 Logic Gates	9.1 x 9.2	Sept. 1989	42
Casino Test Chip	Std. Cell	2.16	3700 Logic Gates	8.3 x 8.6	Jun. 1988	68
Casino Test Chip	Cell Array	2.20	4126 Logic Gates	11.7 x 11.7	Mar. 1990	78

A rigorous evaluation of each circuit would consider five criteria:

Functionality	Logic: pass all test vectors at 25°C Memory: all bits work at 25°C
V_{DD}	Works for $1.8 < V_{DD} < 2.2V$
I/O	Complies with all I/O voltage specifications $V_{IH} \le 0.9$, $V_{IL} \ge 0.3$, $V_{OH} \ge 1.0$, $V_{OL} \le 0.2V$
Speed	Logic: works at 200 MHz for 15-20 gate delays Memory: works at 200 MHz
Temperature	Works from -55 to 125°C

Table 2 shows specific test results for each circuit. For both memory and logic, each entry shows when a milestone was first accomplished. For the full-size circuits, the entries also show the yield. The table should be read from left to right. For example, for memory wafer probe at 40°C, only memory sites where all bits work from $V_{DD} = 1.8$ to 2.2 were tested to see if they conform to the I/O level specification.

We had a sizeable yield of working 256-bit PT-2M memory circuits, although none of them worked at 125°C. Only one working 4K SRAM I was found, and the 4K SRAM II had a design flaw that prevented it from working.

We had fully functional logic circuits on the first design pass for all circuits except the Memory Tester (which had a mask error that was never corrected) and the Standard Cell Casino Test Chip (where all subcircuits worked on various chips, but there was no single chip where all subcircuits worked). Most circuits passed all the wafer probe criteria on one chip or another, but there were no chips where all wafer probe criteria were satisfied simultaneously.

The best test results for the full-sized circuits are given in Table 3. For some circuits, more than one example is given.

Table 2a - Memory Circuit Performance

Memories	40°C Wafer Probe			Package Test			Full Spec Device	Comment
	All Bits Work V_{DD}=1.8-2.2	I/O Levels	All Tests At Speed	At Speed	0 to 80°C	-55 to 125°C		
PT-2M (256 bits)	March 1989 Yield=1562/55925 50 MHz	March 1989 Yield=604/1562	Oct 1989 Yield=70/604	June 1989 Yield=185/295	Sept 1989 Yield=3/91			Ripple & Pipeline 200MHz for 0-80°C 50MHz with reduced specs for -55 to 125°C
4K SRAM I (4096 bits)	June 1990 Yield=1/1765 50 MHz	June 1990 Yield=1/1765 50 MHz						
4K SRAM II (4096 bits)	Yield=0/3746							Design Flaw Not functional

Table 2b - Key for Memory Circuit Performance

All Bits Work, V_{DD}=1.8 - 2.2	— all bits work for $1.8 < V_{DD} < 2.2V$
I/O Levels	— all bits work for $1.8 < V_{DD} < 2.2V$ and $V_{OH} > 1.0V$, $V_{OL} < 0.2V$, $V_{IH} < 0.9V$, $V_{IL} > 0.3V$.
All Tests at Speed	— meets all specs, and the part is faster than 5ns.
Package at Speed (Frequency)	— functional packaged devices work at 200 MHz. In addition, all bits work and pass disturb tests for $1.8 < V_{DD} < 2.2V$ and $V_{OH} > 1.0V$, $V_{OL} < 0.2V$, $V_{IH} < 0.9V$, $V_{IL} > 0.3V$.
0 to 80°C	— meets all specs over 0 to 80°C
-55 to 125°C	— meets all specs over -55 to 125°C
Full Spec Device	— meets all requirements. Customer agrees "this is what I want".

Table 2c - Logic Circuit Performance

	Total Gates	Wafer Probe				Package Test		Full Spec Device	Comment
	Gates in Critical Path	Pass Test Vectors	V_{DD}	I/O	Prop Delay	At Speed	-55 to 125°C		
PT-2M Adder	91 9	March 1989 - 1 MHz							Brief testing to *Demonstrate Functionality*
PT-2M Multiplexer	283 4	March 1989 - 1 MHz							Brief testing to Demonstrate Functionality
PT-2L Adder	364 9	Nov 1988 - 1MHz Yield=123/300	Feb 1989 Yld=121/123	Feb 1989 Yld=33/121					Work for -55 to 125°C Pkg ≥ 400 MHz
PT-2L Multiplier	1778 40	Nov 1988 - 1 MHz Yield=88/240	Feb 1989 Yld=55/88	Feb 1989 Yld=19/55					Work for -55 to 125°C 7ns prop delay
PT-2L ALU	2211 33	Feb 1989 - 1MHz Yield=36/240	Feb 1989 Yld=11/36	Feb 1989 Yld=1/11					Work for -55 to 125°C Pkg = 178 MHz
PT-2L Memory Tester	1723								Layout Error Not Functional
1K Cell Array	738 27	Sept 1989 - 10 MHz* Yield=256/1826	Oct 1989* Yld=62/498	Jan 1990* Yld=1/123		Yld=1/136			Work for -55 to 125°C Pkg = 200 MHz V_{DD}=2.2V
Custom Multiplier	6500 70	Oct 1990 - 60 MHz Yield=25/1040	Apr 1991 Yld=16/25	Apr 1991 Yld=5/16		Yld=0/30			Pkg = 100 MHz
Custom ALU	3571 26	June 1989 - 1 MHz Yield=136/2998	Nov 1989 Yld=11/37	Yld=0/11		Yld=0/68			Work for -55 to 125°C Pkg = 170 MHz
Std. Cell ALU	3452 26	Nov 1989 - 1 MHz Yield=8/867	Dec 1989 Yld=3/8	Yld=1/3		Mar 1990 Yld=1/3**			≥100 MHz at Room Temp **100 MHz
Std. Cell Transversal Filter	5190 23	Nov 1989 - 1 MHz Yield=12/400	Apr 1990 Yld=5/12	Apr 1990 Yld=4/5					40 MHz at Wafer Probe (Test Set Limit)
Std. Cell Casino Test Chip	3700								Never Fully Functional
Cell Array Casino Test Chip	4126 18	Oct 1990 - 80 MHz Yield=1/867							

*Three different testing schemes

Table 2d - Key for Logic Circuit Performance

Pass Test Vectors	— at some power supply voltage
V_{DD}	— passes test vectors for $1.8 < V_{DD} < 2.2V$
I/O	— passes test vectors for $1.8 < V_{DD} < 2.2V$ and $V_{OH} > 1.0V$, $V_{OL} < 0.2V$, $V_{IH} < 0.9V$, $V_{IL} > 0.3V$.
Prop Delay	— faster than 5ns for 17.5 gates in critical path for all test vectors while meeting V_{DD} and I/O voltage level specifications.
At Speed	— functional packaged devices work at equivalent of 200 MHz for 17.5 gate delays. In addition, all test vectors are passed for $1.8 < V_{DD} < 2.2V$, $1.8 < V_{DD} < 2.2V$ and $V_{OH} > 1.0V$, $V_{OL} < 0.2V$, $V_{IH} < 0.9V$, $V_{IL} > 0.3V$.
-55 to 125°C	— meets all specs over -55 to 125°C
Full Spec Device	— meets all requirements. Customer agrees "this is what I want."
Comment	— In this column, "work" means passes all test vectors. This column is used to show speed and temperature performance of circuits that work but do not fully conform to specifications for power supply and/or I/O voltage levels.

Table 3 - Best Circuit Results

Memory	
•PT-2M	- Satisfies functionality, V_{DD}, I/O, and speed for 0-80°C - Satisfies functionality, I/O, and temperature at 50 MHz over part of the V_{DD} range.
• 4K SRAM I	- Satisfies functionality, V_{DD}, and I/O at 40°C and 50 MHz
• 4K SRAM II	- Not functional. Design flaw.
Custom	
• ALU	- Satisfies functionality, speed, and temperature at V_{DD} = 2.0V, but fails one of the four I/O specifications. - Satisfies functionality, V_{DD}, and speed over 25-125°C, but fails one of four I/O specifications.
• 32-Bit Multiplier	- Satisfies functionality, speed, and temperature between V_{DD} = 2.0 and 2.2V, but fails one of the four I/O specifications. - Satisfies functionality, V_{DD}, and speed at -55°C.
Standard Cell	
• Standard Cell Casino Test Chip	- Inferred to be functional because each subcircuit works on at least one chip, but no single chip is fully functional.
• ALU	- Satisfies functionality, V_{DD}, and I/O at 125 MHz and 25°C.
• Transversal Filter	- Satisfies functionality, V_{DD}, and I/O at room temperature up to 40 MHz (the limit of the test equipment)
Cell Array	
• 1K Cell Array	- Satisfies functionality, V_{DD}, and I/O at 100 MHz and 25°C. - Satisfies functionality, speed, and temperature at 2.2V, but fails one of the four I/O specifications.
• Cell Array Casino Test Chip	- Satisfies functionality at V_{DD} =2.2V up to at least 80 MHz.

These circuits draw from 2 to 7 watts. Figure 3 shows both the simulated (s) and measured (m) powers for seven of the full-size circuits. In each case, the simulation gives a good approximation of the actual power, with the measured power being slightly lower than simulation in all cases.

To put these results in perspective, recall that the Statement of Work for this program emphasized 200 MHz operation, minimal power consistent with that clock speed, and functionality over the military temperature range from -55 to 125°C. In general, our circuits achieved these goals. Extensive testing demonstrated functionality at 200 MHz (normalized to 20 gate delays where necessary) for the PT-2M SRAM, the Custom ALU and 32-Bit Multiplier, and the 1K Cell Array. Functionality was maintained over the military temperature range for the Custom ALU, the 32-Bit Multiplier, and the 1K Cell Array. And low power was achieved; the 140 fJ/gate delay-power product reported for the 32-Bit Multiplier in Section 2.14 is considerably lower than fast silicon parts that are around 1000 fJ/gate. Our other logic circuits had less extensive testing, but we would expect them to be consistent with these results. The only major shortcoming of our circuits was that our chips could not consistently comply with the I/O voltage requirements, although the 32-Bit Multiplier came close.

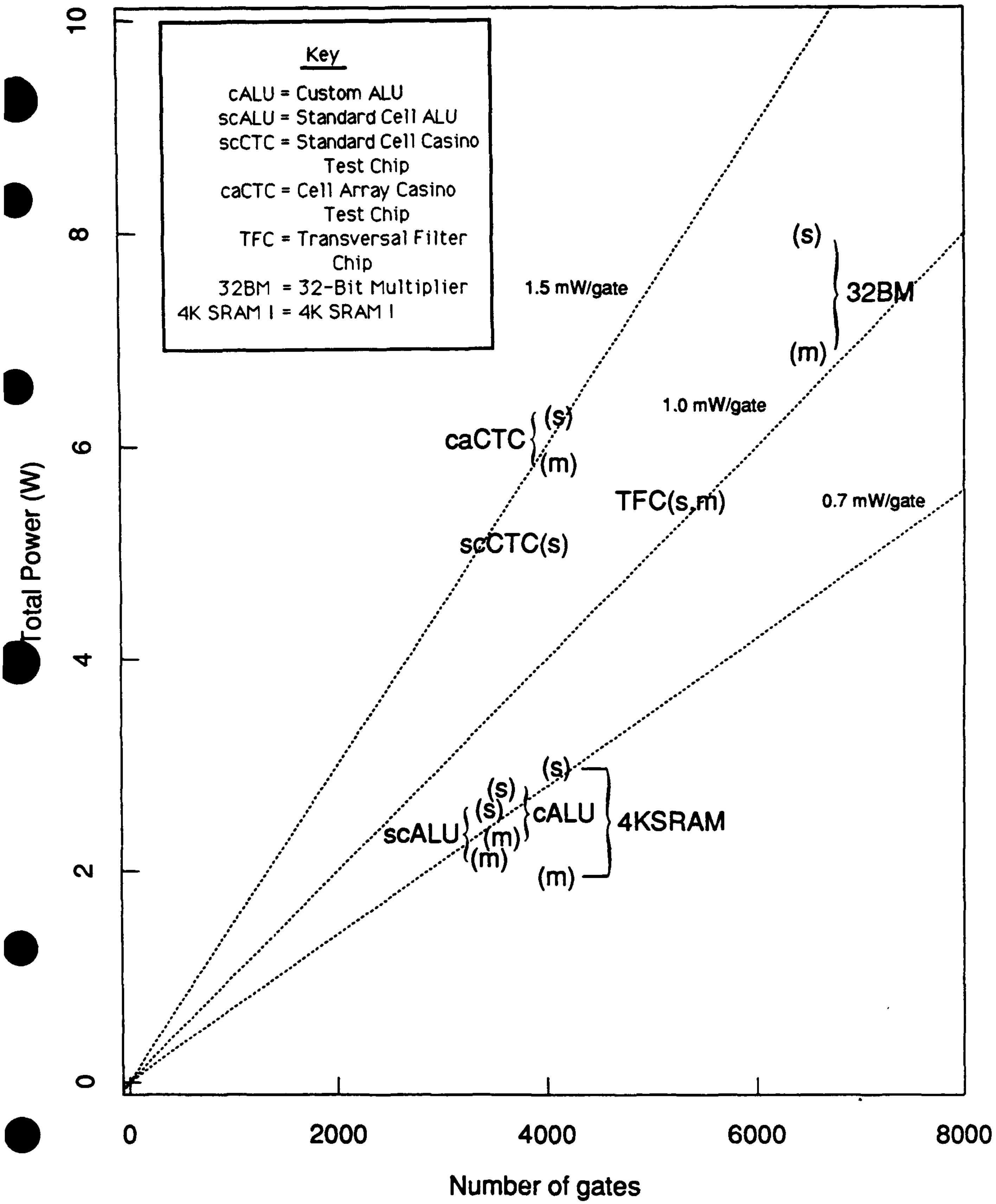


Figure 3 - Measured and Simulated Power for Pilot Line Circuits

2.2 Logic Family (A. I. Faris and P. J. Robertson)

The circuits in this program were required to operate at 200 MHz over the military temperature range of -55 to 125°C. Power dissipation was to be minimized, but speed and operating temperature range were given higher priority by the Statement of Work. To choose a logic family, we compared four possibilities: Direct-coupled FET Logic (DCFL), FET Injection Logic (FIL), Source Follower FET Logic (SFFL), and Depletion-mode Source Follower FET Logic (DSFFL).

Figure 4 illustrates simulations of two key parameters, noise margin and propagation delay. The figure shows that DCFL has no noise margin low (NML) at 125°C, eliminating it from contention. Of the remaining three families, SFFL is substantially faster. Additional information on speed in shown in Figure 5, which shows the simulated delays per fanout and per fF of capacitive load. FIL is subject to much more delay per fanout than SFFL or DSFFL. Considering all the elements of Figures 4 and 5, SFFL was the clear choice. By providing a 1.5V logic swing, it has good noise margins and will provide circuits that are robust as temperature changes. In addition, SFFL gates can tolerate ±150 mV variation in EFET threshold voltage without a serious loss is margin or performance.

An SFFL 4-input NOR is illustrated in Figure 6. NAND and OAI structures are also available in SFFL. As shown in Figure 7, the power dissipation for an unbuffered SFFL gate is about 550μW. For a buffered gate, it is around 2 mW. While this is larger than the other logic families, it must be accepted, given the higher priorities placed on speed and noise margin. In any case, this power dissipation should be acceptable for the size circuits planned for this program.

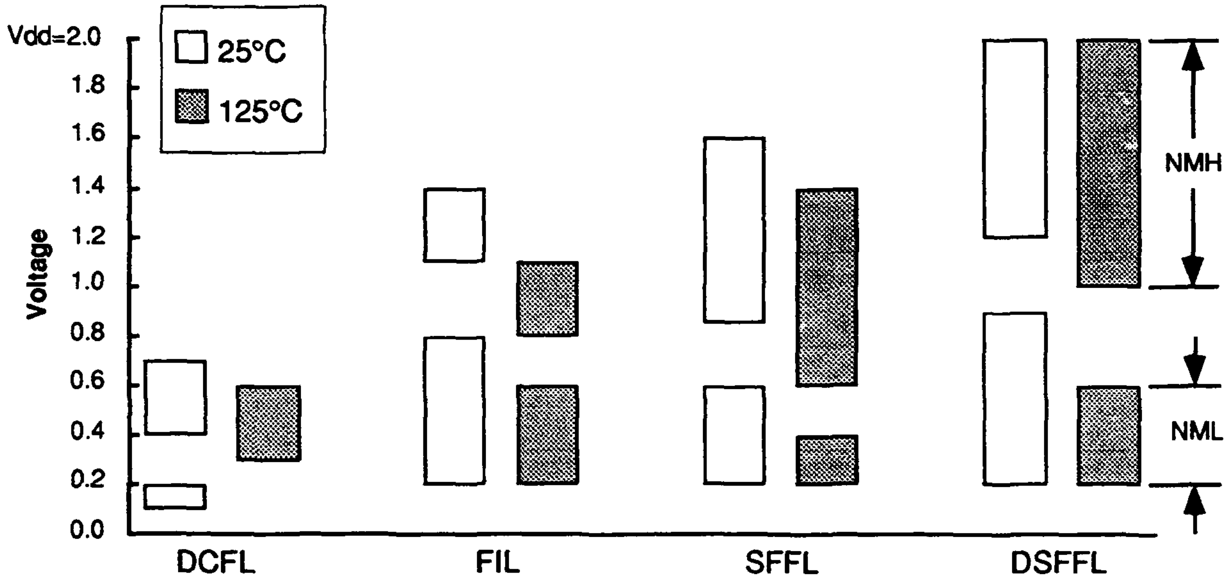
2.3 Parameter Extraction and Modeling (A. D. Brotman, R. D. Pierce, P. G. Flahive and J. L. Lentz)

Over the course of this program, a series of FET model parameters were established for AT&T's ADVICE in circuit simulator. Using global nonlinear-least-squares optimization techniques, DC parameters were extracted from measurements at 25°C and 125°C on nominal EFETs and DFETs. AC parameters were based on capacitances extracted from S-parameter measurements using a linear microwave model. This approach permitted a wider sampling of the bias space, and was first validated by comparing the derived capacitances with direct CV measurements.

As device processing evolved, and processing variations were reduced, the models were continually improved both to represent the FETs more accurately and also to set the targets for the characteristics of typical FETs. The early models (versions 1-9) tracked FET data to extract model parameters. The versions named SargicS.1-8 were based on data from the PT-0 maskset, and SargicS.1-5 were simply early attempts at characterizing our FETs.

SargicS.6, 7, and 8 were evolutionary upgrades primarily involving the E-tub diode models. SargicS.9 was the first version to include best and worst case noise margin models. It was an engineering estimate based on the first PT-1 baseline wafer set, intended to simulate ±1σ variations in EFET threshold voltage and E/D current ratio. Designer experience with SargicS.9 showed that it was unacceptable. The EFET threshold voltage was too high, limiting high noise margins. The current ratio was too low, impacting circuit FET width ratios, and the threshold variation was too wide.

SargicS.10 and 11 represent a strategy of response to design community needs. They addressed the shortcomings of SargicS.9, iteratively introducing characteristics acceptable to the design community, and thereby establishing targets for material growth and device fabrication. Some key characteristics of these models are shown in Figure 8.


Noise Margins

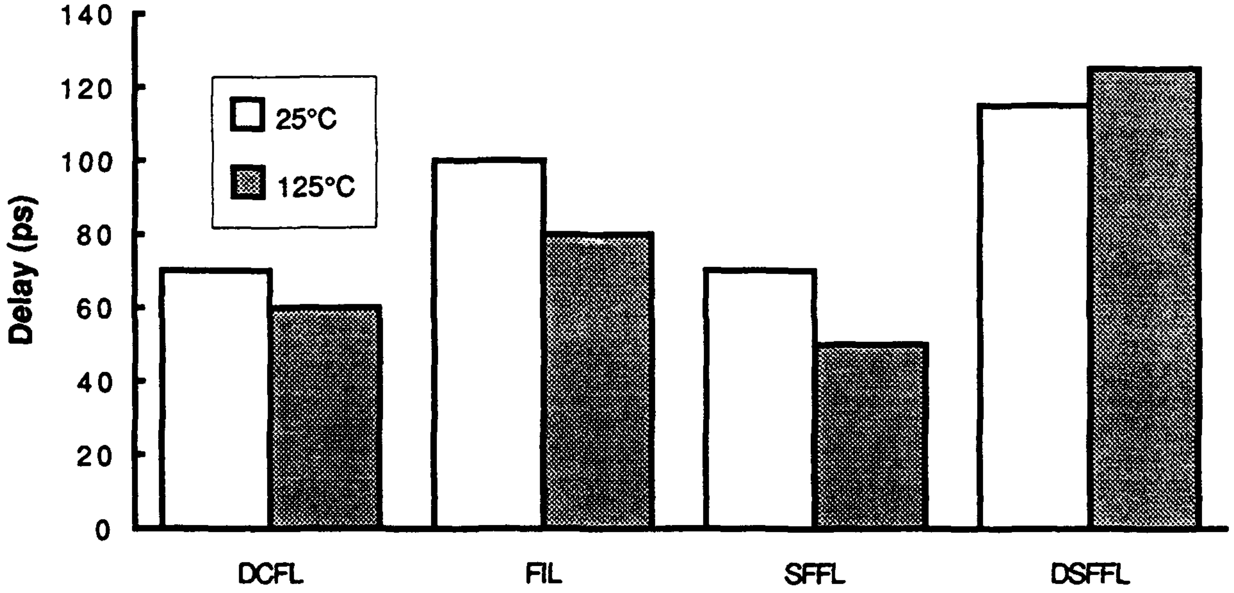

Propagation Delay
(Vdd=2V, Fanout=2)

Figure 4 - Noise Margins and Propagation Delays for Four Logic families: Direct Coupled FET Logic (DCFL), FET Injection Logic (FIL), Source Follower FET Logic (SFFL), and Depletion-mode Source Follower FET Logic (DSFFL). NMH is Noise Margin High, and NML is Noise Margin Low.

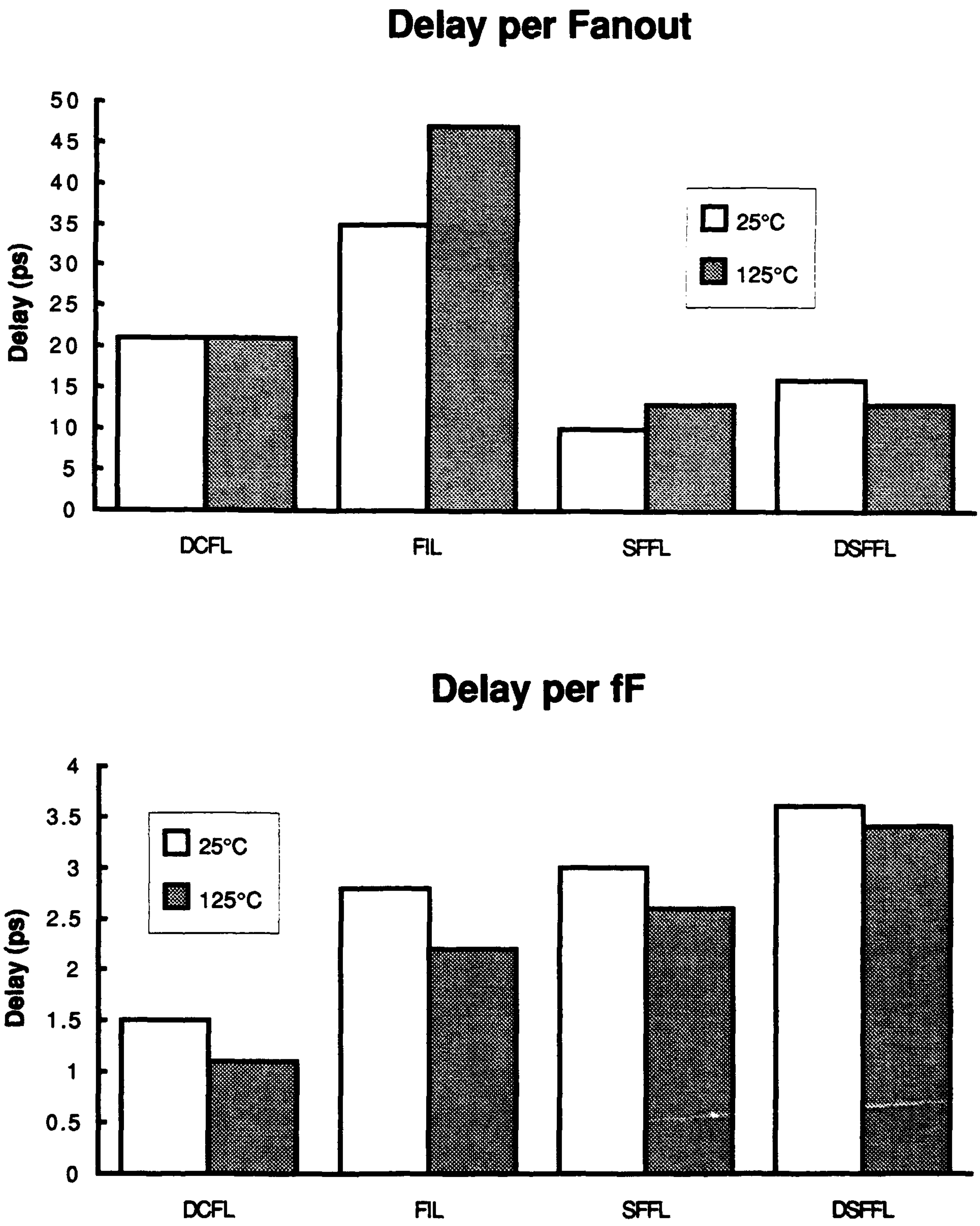


Figure 5 - Delay per Fanout and Delay per fF of Capacitive Load for Four Logic Families.

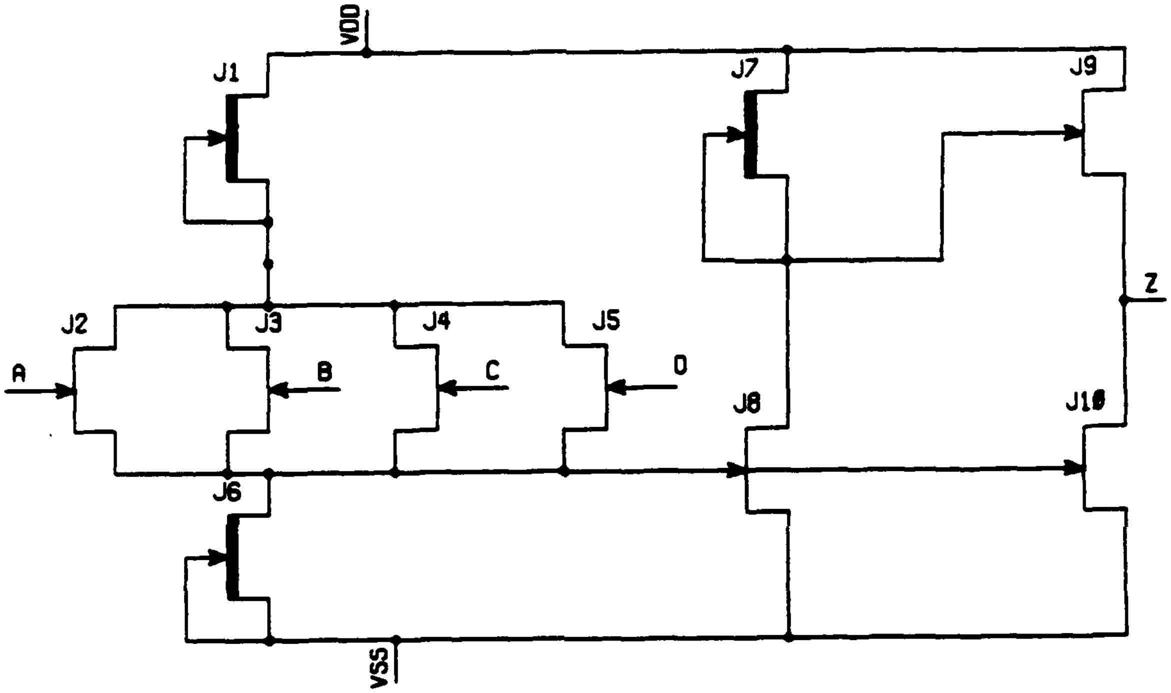

VDD
J1
J7
J9
J2
J3
J4
J5
Z
A
B
C
D
J8
J10
J6
VSS

Figure 6 - SFFL 4-Input NOR

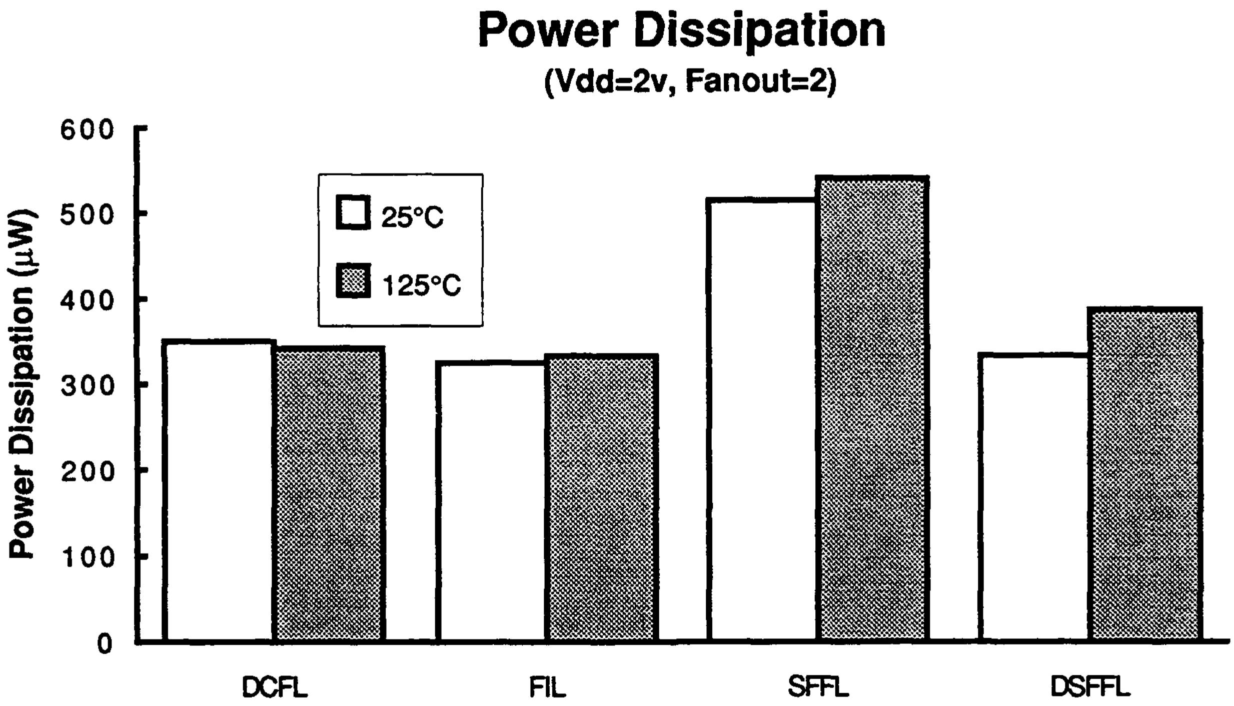


Figure 7 - Power Dissipation per Unbuffered Gate for Four Logic Families

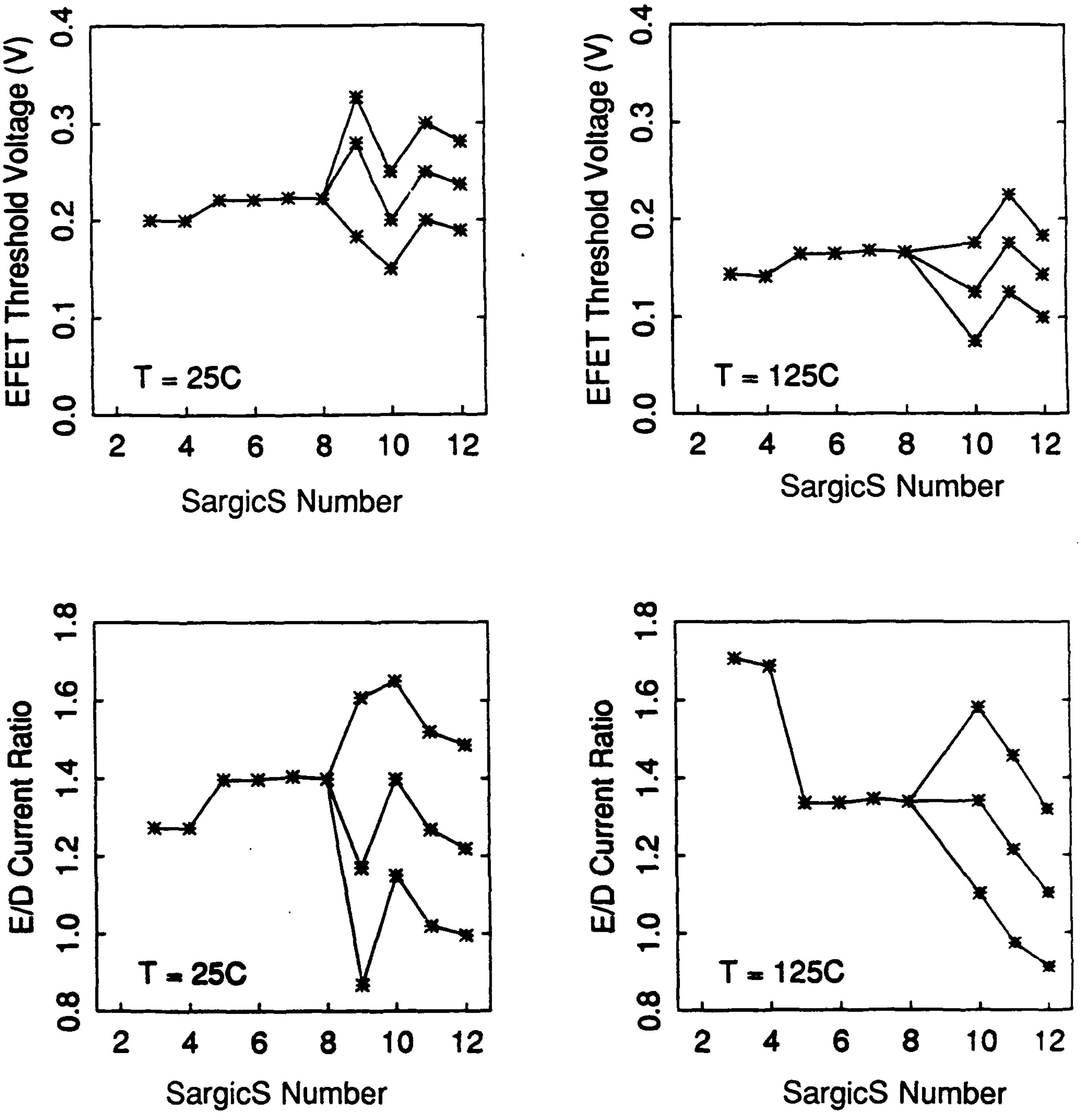


Figure 8 - Comparison of SargicS FET Model Parameters

SargicS.12 adopts a strategy of material engineering and device simulation, using the one-dimensional device simulator SIGMA. That is, for the first time, the models are used as targets for the characteristics of processed FETs. This provides a stable model for use in the design community, and gives processors targets for wafer fabrication. SIGMA calculates the equilibrium charge distribution and band structure of a GaAs/AlGaAs heterojunction device at a given gate bias by self consistently solving Poisson's equation with Schrödinger's equation for the device. The charge density under the gate is integrated to yield the sheet charge, N_S, from which threshold voltage can be extracted.

For SargicS.12, we used the GADVICE FET model which incorporates SIGMA results in a straightforward way and includes an improved capacitance model. The characteristics of SargicS.12, shown in Figure 8, are similar to those of SargicS.11. The following table compares the AC characteristics of SargicS.9 through 12 with measured data. SargicS.12 maintains good agreement for expected ring oscillator delays and shows improved agreement for small signal microwave characteristics such as f_T.

Parameter	PT-1 Baseline Wafers	SargicS.9	SargicS.10	SargicS.11	SargicS.12 (prelim.)	
R.O. Gate Delay (ps)	75-100	64	75	71	65	ps
Parasitic Load (fF)	—	5	5	5	5	fF
EFET f_T (GHz)	20-22	11.7	12.3	12.6	19.7	GHz
DFET f_T (GHz)	16-18	10.2	11.0	11.0	17.9	GHz

The sensitivity of threshold voltage to variations in material thickness and doping was also calculated using SIGMA, and the results are listed below.

	Sensitivity	
Material Parameter	DFET	EFET
Donor Layer Thickness	5.3mV/Å	2.6mV/Å
Undoped Layer Thickness	2.1mV/Å	1.8mV/Å
Doping	4.0mV/1E15cm^{-3}	1.4mV/1E15cm^{-3}

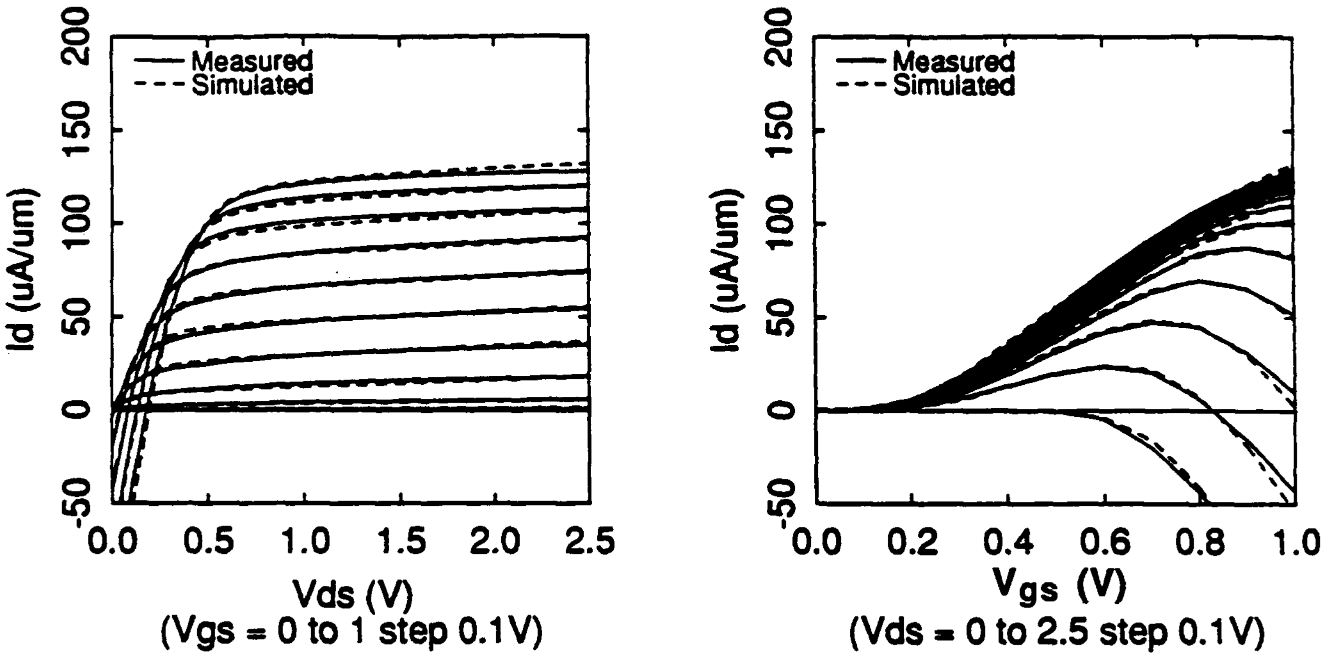
Threshold voltage is most sensitive to variations in the thickness and doping of the donor layer. These sensitivities imply that ±2% control of material variations is required to maintain threshold voltage within the ±50mV required by our current circuit designs.

For SargicS.13-15, the final three versions of the Sargic.S model, the compact model equations in the circuit simulator, GADVICE, were modified to better reflect measured FET performance. These modifications included an exponential subthreshold current and a frequency dependent output conductance. These three model files include ±50mV variation in threshold voltage and a 20% variation in E/D current ratio. A new set of PCM parameters, which are measured directly, were defined.

The conduction parameters for the compact model files 13 and 14 were generated from the one dimensional physical simulator, SIGMA. Parameter set 14 represents modifications made based on preliminary FET data. When sufficient FET data for the new material structure became available, parameters were extracted from data, resulting in parameter file 15. A subthreshold term accounts for more accurate modeling of the 2% I_{dss} point in parameter sets 13-15 relative to parameter set 12. The frequency dependent output conductance allows us to have the larger DC value which rolls off to the AC value at ~10 MHz as is observed experimentally.

Curves describing the final model, SargicS.15, are shown in the Device Terminal Characteristics section of the Design Guide (Appendix A, page A-44 through A65). A comparison of measured and simulated device characteristics is shown in Figure 9.

sargicS EFET, 25C



sargicS DFET, 25C

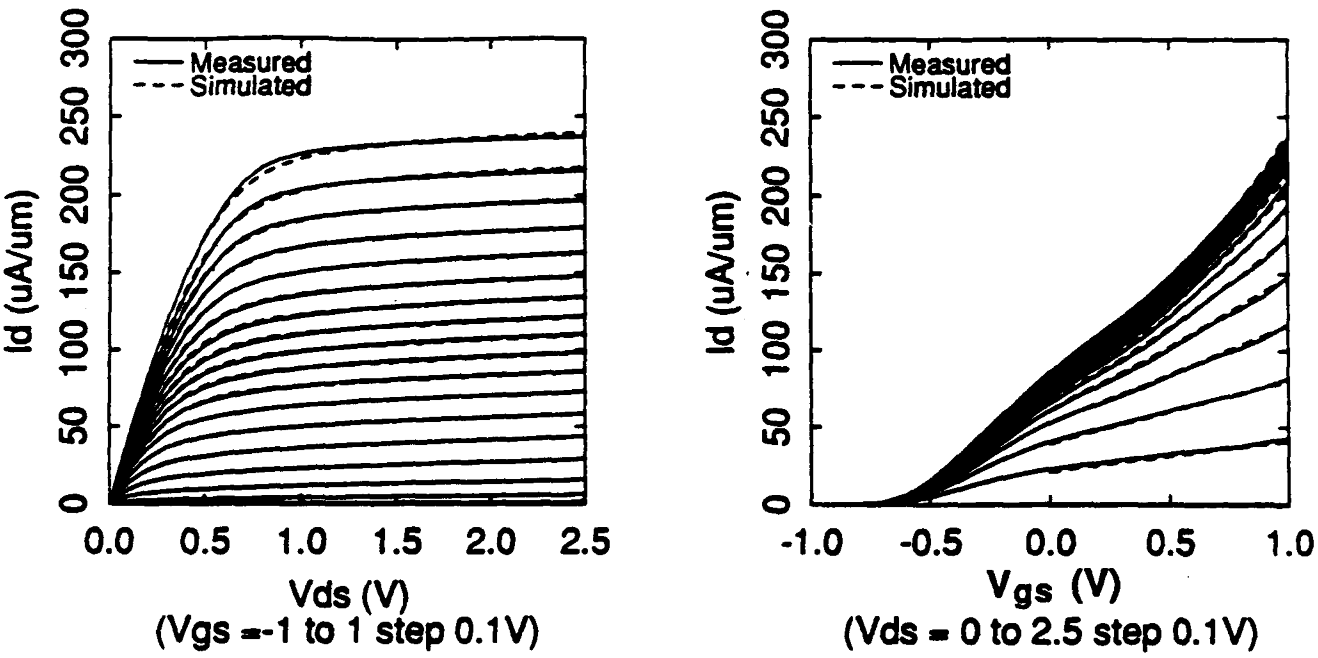


Figure 9 - 25°C Measured and Simulated DC EFET and DFET Characteristics

2.4 HCAD: A User Friendly CAD System (L. Fisher and M. Nguyen)

Development Effort

The development effort that resulted in HCAD began in the second half of 1987. Initially, the intention was to leverage existing DARPA-funded CAD development efforts. However, development schedules and product availability precluded using the fruits of those efforts. Instead, it was decided to use a commercially available CAD system as the basis of HCAD. Following a survey of several vendors, the Cadence Edge product line was selected to form the basis of HCAD. Once the foundation for HCAD was selected, development effort was undertaken to build libraries and to integrate tools into the HCAD environment.

Standard Cell, Macro Cell, and Gate Array libraries were developed. The standard cell library was the first to be captured in HCAD (it was designed at AT&T). This library was used in the standard cell version of the Casino Test Chip. The process technology changed during the course of the Program, however, obsoleting the first standard cell library. In mid-1988, the development of a macro cell library was undertaken at AT&T, and later captured in HCAD. This library was used in designing the Transversal Filter Chip (the chip consists of approximately 5K gates, and was functional in the first lot!). The final library to be developed and captured in HCAD was for the 5K gate array. The library was used in designing the cell array version of the Casino Test Chip. Along the way, many versions and iterations on the three libraries were transferred between AT&T and Hughes. In HCAD, all three libraries included logic simulation models, fault simulation models, circuit simulation models, timing models, layouts, and layout abstracts. Extensive verification procedures were used to ensure the accuracy and correctness of the various parts of the libraries.

Hits, N.2, and Gate Station had to be integrated into HCAD in order to provide a more complete CAD environment beyond that which is available from Cadence. A set of Hughes-developed tools was also integrated into HCAD to provide support for scan-based ATPG in designs using set-scan. These tools include a scan partitioner (Prospect) and a fault analyzer (ast). Integration involved the development of both data interfaces (netlists, vectors, faults), control interfaces (execution models), and user interfaces (menus, fill forms, etc.).

Both the libraries and the integration code have been well documented, with library data books and software specifications included among the deliverables given to AT&T.

HCAD System Overview

HCAD consists of a collection of tools (a layout editor, for example), several libraries and technology files, and an integration framework that ties the tools and libraries together. Many of the tools and the integration framework are part of the Edge or Opus design environment from Cadence. This approach to constructing HCAD provides a flexible environment, allowing a consistent, predictable look and feel across many tools.

The backbone of HCAD is the Cadence Design Framework. The Cadence Design Framework, like the other Cadence tools, uses the UNIX® operating system. The Design Framework offers a sophisticated multiwindow, multitasking environment in which multiple applications can be run simultaneously. User interaction with the application programs is through hierarchical pop-up menus that are manipulated by a mouse. A command line interface can also be used. Several of the programs also support stand-alone use - that is, they may be invoked from the UNIX® shell as well as from within HCAD.

Pop-up menus make the entry and execution of commands easy and fast. In the HCAD system, the pop-up menus are hierarchical. From one level of a menu, the user can traverse up or down the hierarchy easily by selecting the "arrow" symbol. This capability is useful since it helps reduce menu clutter by partitioning the items depending on the application selected. In Design Framework, menus and menu items are modifiable, i.e. the CAD software developer can change the menu layout style or add a complete new set of menus as desired. By allowing this capability, new application software or user-designed tools can be customized and integrated into the Design Framework and HCAD with ease.

With each menu or menu item, on-line help files exist to provide the user with necessary help information for each command. The Design Framework allows new on-line help files to be created and added for each new menu item and command. Figure 10 illustrates the design functions provided by HCAD.

At the center of the HCAD architecture is Cadence's unified database. It provides the capability to store and access all information in one consistent form. With a single unified interface to the design data, the Design Framework promotes tool modularity. Thus, user tools can be "plugged" into the system easily. Data translation from one tool to another becomes unnecessary.

The HCAD unified database provides a common interface between the tool and the design information. In a similar fashion, the HCAD human interface provides a single interface between the tool and the designer to alleviate the problem of different interfaces for each tool. Multiple-window graphics, fixed and pop-up menus, and hierarchical text forms are used in the consistent human interface that is available in HCAD.

To access the unified database and use the human interface, a development environment based on the proprietary language SKILL is provided by Cadence. Based on the artificial intelligence language LISP, SKILL has a C-like syntax and supports the combined features of C and the powerful list processing capabilities of LISP. SKILL was used extensively in the development of HCAD, both as a support tool (to automate repetitious processes) and as a development tool (to support tool integration). In addition, a library of useful SKILL routines has been included with HCAD.

As depicted in Figure 11, HCAD offers a unified user interface and a unified database. The various design tools can be "plugged" into the framework. Although many of the tools are provided by Cadence, the overall design environment is flexible enough to accommodate both user and vendor's tools. This capability was one of the key factors in the selection of Cadence to form the basis of the HCAD System. The Design Framework plays a major role in satisfying the HCAD requirements for user friendliness, portability, system modularity, and maintainability.

TYPICAL DESIGN FUNCTIONS

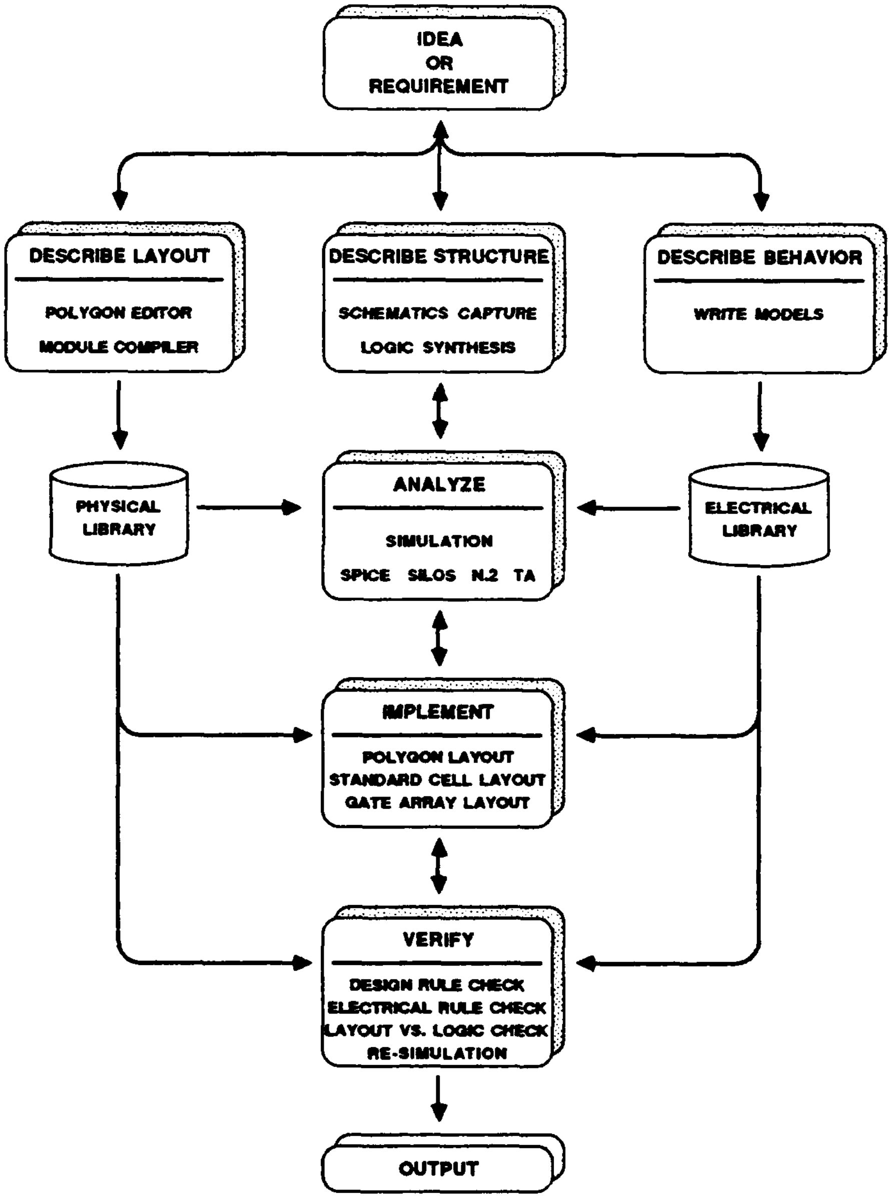

IDEA
OR
REQUIREMENT
DESCRIBE LAYOUT
POLYGON EDITOR
MODULE COMPILER
DESCRIBE STRUCTURE
SCHEMATICS CAPTURE
LOGIC SYNTHESIS
DESCRIBE BEHAVIOR
WRITE MODELS
PHYSICAL LIBRARY
ANALYZE
SIMULATION
SPICE SILOS N.2 TA
ELECTRICAL LIBRARY
IMPLEMENT
POLYGON LAYOUT
STANDARD CELL LAYOUT
GATE ARRAY LAYOUT
VERIFY
DESIGN RULE CHECK
ELECTRICAL RULE CHECK
LAYOUT VS. LOGIC CHECK
RE-SIMULATION
OUTPUT

Figure 10 - Design Functions Supported in the HCAD System

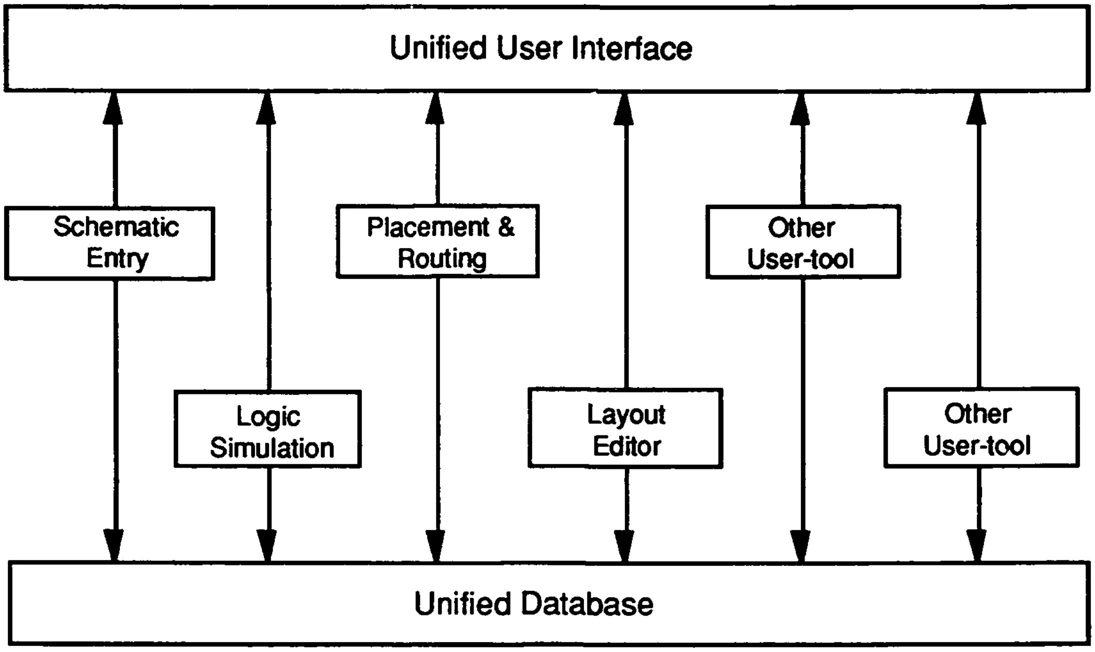


Figure 11 - The Design Framework architecture offers a unified database and user interface. User-specific applications or modules from either Cadence or other vendors can be added to the system.

A Users Manual is provided in addition to the software and libraries that make up HCAD. The users manual is not intended to provide instruction in the detailed use of the commercial tools in HCAD, nor is it intended to provide detailed information about the Library. Other documents provide that information. Rather, it provides an overview of the commercial tools and the AT&T library, and guidance on how to make the different parts of HCAD play together. With sufficient information on how to operate each subsystem of HCAD, a designer should be able to design, analyze, and lay out a complete circuit. Throughout the manual, many references to the applicable vendor documentation are furnished to help the designer acquire more in-depth knowledge about the available facilities supported by both HCAD and the Cadence Design Framework.

HCAD Applications

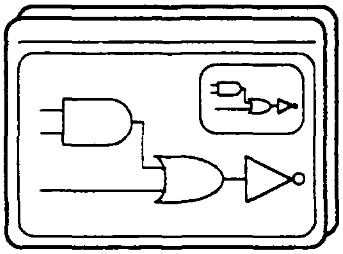
HCAD provides a rich set of applications supporting capabilities ranging from architectural simulation through circuit simulation and full custom (polygon) layout through fully automatic standard cell and gate array layout.

Figures 12 and 13 illustrate some of the features of the applications provided in HCAD. Front-end design functions are those associated with design capture and simulation, while back-end design functions are those associated with layout and layout analysis.

The HCAD System is heavily based on the commercial IC design system from Cadence. This IC design system provides both a state-of-the-art design capability and user interface as well as a unique tool integration framework allowing tight integration of non-Cadence tools into the Cadence environment. Table 4 lists the different tools used in HCAD and shows what functions they perform.

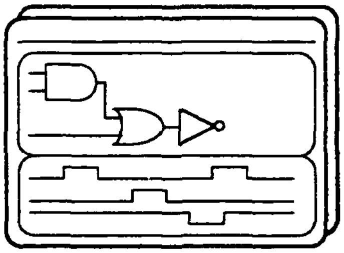
FRONT-END DESIGN FUNCTIONS

SCHEMATICS CAPTURE



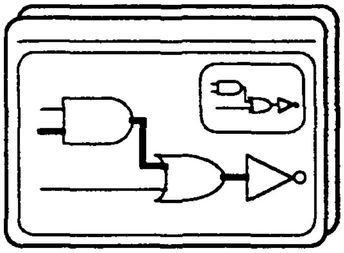
- MULTI WINDOW
- MULTI DESK
- ON-LINE HELP
- CONTEXT SENSITIVE POP-UP MENUS
- VIDEO LS, FILL FORMS
- SELECTION BY POINTING, AREA, LAYER
- USER-DEFINED KEYS

LOGIC SIMULATION



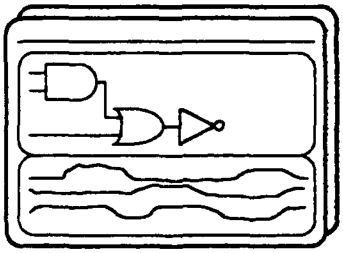
- NET PROBING
- WAVEFORM DISPLAY
- COLOR COORDINATION
- TIME RULER
- 12 STATE

TIMING ANALYSIS



- VISUAL DISPLAY OF CRITICAL NETS
- TIMING DIAGRAMS
- VECTOR INDEPENDENT
- MIXED LEVEL TIMING LOGICAL AND ELECTRICAL
- WORKS WITH SCHEMATICS AND EXTRACTED LAYOUTS WITH PARASITICS

CIRCUIT SIMULATION

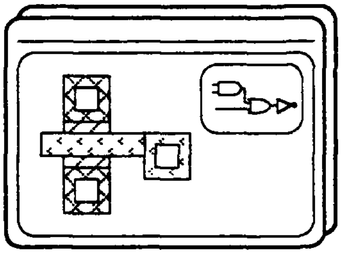


- NET PROBING
- WAVEFORM DISPLAY
- COLOR COORDINATION
- HSPICE - INDUSTRY STANDARD
- LOCAL OR REMOTE SIMULATION

Figure 12 - Front-End Design Application Features

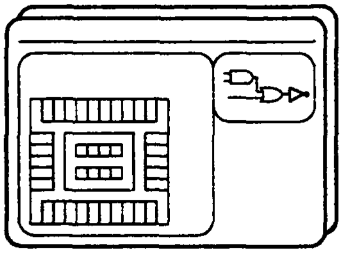
BACK-END DESIGN FUNCTIONS

LAYOUT



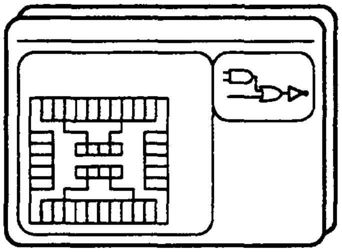
- ALL ANGLE GEOMETRIES
- 128 LAYERS
- ON-LINE DESIGN RULE CHECKING
- MULTI-WINDOW
- STRUCTURE COMPILER

AUTO PLACE



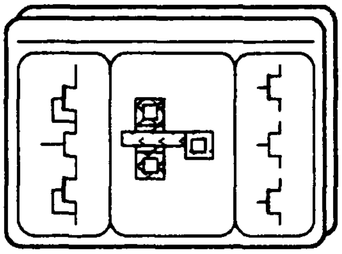
- SCHEMATIC OR EDIF NETLIST AS INPUT
- AUTOMATIC OR MANUAL PLACEMENT
- TEXT-DRIVEN PLACEMENT
- VARIABLE ASPECT RATIO
- MULTIPLE PLACEMENT REGIONS

AUTO ROUTE



- GLOBAL AND DETAIL ROUTING
- NET ORDERING, PRIORITY
- AUTOMATIC OR MANUAL ROUTING
- AUTOMATIC POWER AND GROUND ROUTING
- CURRENT-DEPENDENT LINE WIDTH

VERIFICATION



- COMPARE CONNECTIVITY-EXTRACTED LAYOUT VS. SCHEMATIC
- CROSS PROBING BETWEEN EXTRACTED LAYOUT AND SCHEMATIC
- MISMATCHES HIGHLIGHTED
- EXTRACT NETLIST, PARASITICS, PARAMETERS

Figure 13 - Back-End Design Application Features

Table 4. Summary of HCAD System Tools

Function	Tool
Schematic Edit	Cadence Edge Graphics Editor
Logic Simulation	SILOS
Behavior/Functional ("C" Program, etc.)	Endot N.2
Automatic Placement and Route - Gate Array	Mentor Gate-Station
Automatic Placement and Route - Standard-Cell	Cadence StandardEdge
Full-Custom Layout Editing (Polygons)	Cadence Graphics Editor
Layout-Based Timing Simulation	SILOS
Static Timing Analysis	Cadence TA
Circuit Simulation	HSPICE
Layout Verification (DRC, Extract, LVS)	Cadence PDCheck, PDExtract, PDCompare
Test Vector Generation	HITS
Fault Simulation	SILOS
DFT Support	Hughes tools

HCAD Libraries

The current version of HCAD fully supports full custom, macrocell and gate array styles of layout. A macrocell library with over 45 elements is included, as is a gate array library with 30 elements.

The gate array floorplan included will support designs with up to 3,500 used gates. Table 5 lists the elements in the gate array library and Table 6 lists the elements in the macro cell library.

Table 5. Summary of HCAD Gate Array Library

Cell Name	Cell Function
ninrb	low drive inverter
minrb	medium drive inverter
hinrb	high drive inverter
nnr2	low drive nor2
mnr2	medium drive nor2
hnr2	high drive nor2
nnr3	low drive nor3
mnr3	medium drive nor3
hnr3	high drive nor3
nnr4	low drive nor4
mnr4	medium drive nor4
hnr4	high drive nor4
nnr5	low drive nor5
mnr5	medium drive nor5
hnr5	high drive nor5
nmux21	low drive 2-to-1 mux
mmux21	medium drive 2-to-1 mux
hmux21	high drive 2-to-1 mux
noai22	low drive or-and-invert
moai22	medium drive or-and-invert
hoai22	high drive or-and-invert
nfd1s2ax	low drive flip-flop
mfd1s2ax	medium drive flip-flop
hfd1s2ax	high drive flip-flop
ckdrv	clock driver
sigdrv	signal driver
mca50rlp	output pad
mca50tbp	output pad
mcainrlp	input pad
mcaintbp	input pad

Table 6. Summary of HCAD Standard Cell Library

Cell Name	**Cell Function**
aoi3333	and-or-invert
barsrb4	barrel shifter
bclab4	adder
bme	multiplier/encoder
bmfab4	booth multiplier
bmhab4	booth multiplier
bmmuxb4	booth multiplier
ckdrv_m	clock driver
clab4	adder
clcb4	carry lookahead
ctrdb4	down counter
ctrdpb4	down counter
ctrub4	up counter
ctrudb4	up/down counter
ctrudpb4	up/down counter
ctrupb4	up counter
daoi22	dual and-or-invert
daoi32	dual and-or-invert
daoi33	dual and-or-invert
decb4	decoder
dinrb	dual inverter
dmux	dual multiplexor
dnr2	*dual nor*
dnr3	dual nor
dnr4	dual nor
dnr5	dual nor
dxnor	dual exclusive nor
dxor	dual exclusive nor
fadd	adder
fd1s2ax_m	flip-flop
fd1s2dx_m	flip-flop
fd1s2nx_m	flip-flop
fd1s5f_m	flip-flop
hadd	adder
regfb44	register file
scanrfb4	register file
sigdrv_m	driver
srmxpib4	shift register
srpipob4	shift register
srpisob4	shift register
srrfb4	shift register
srsipob4	shift register
tbrin_m	tri-state buffer

Future Potential

A significant portion of HCAD is based on commercial capabilities. Even though no further development effort is being expended on HCAD itself, Cadence and the other vendors are continuing to expend a considerable amount of effort in refining existing tools and developing new tools.

Those who invest in HCAD are also investing in these vendors and will reap continuing benefits as their tools continue to improve. Even now, Cadence is readying a new release of their tools that is substantially improved, especially in the area of Framework capabilities and design data management. Since the last release of HCAD, Cadence has added symbolic layout and compaction, as well as new tools to support library development.

The commercial tools in HCAD provide for long term functional stability and growth. In addition, the flexibility of the tools and consistency of their user interface means that the same tools used in HCAD for AT&T Pilot Line III designs can be used with little effort on designs targeted for other foundries using other technologies. This maximizes the end-user's return on the investment in CAE tools.

2.5 PT-1 Memory (M. V. DePaolis and W. R. Ortner)

Our initial memory designs were placed on the PT-1 maskset. As the PT-1 memories were being designed, we knew that both the design models and the FET characteristics were still changing and being refined. SargicS.5 was the best model available when the PT-1 memories were designed, and we later learned that it was inadequate. Similarly, PT-1 used MBE structures ED4 through ED7 (see Section 4.2). So while we hoped that these memories would work, we didn't expect them to conform to all the design objectives.

Five memory test sites were included in PT-1.

Site 1 - Basic 256-bit cell array tester with and without current limiting resistors.
Site 2 - Rad-hard 256-bit cell array tester with and without current limiting resistors.
Site 3 - Wordline driver and sense amplifier tester.
Site 4 - Non-clocked 256-bit SRAM with basic resistor cell.
Site 5 - Non-clocked 256-bit SRAM with rad-hard resistor cell.

ADVICE simulations were performed on the PT-1 memories. In addition, a full chip circuit model was used for simulating the overall performance of the 256-bit SRAM. Worst case analysis (1.8V and 125°C) showed an address access time of 1.5 ns. Cell write time simulated as 0.5 ns. The simulations also showed that a new row of cells would be selected only after the previously accessed row was deselected.

Using a fully automated Teradyne J937 test system, we tested the memories on 150 PT-1 wafers (7500 memory sites). The results are summarized in Table 7.

Table 7- PT-1 Test Results, Sites 4 and 5

Bin	Description	Rad Hard		Standard		Total	
31	Shorts	910	24.27%	767	20.45%	1677	22.36%
30	Contact Failure	380	10.13%	414	11.04%	794	10.59%
29	Non Functional Hi Power	1050	28.00%	1114	29.71%	2164	28.85%
28	Non Functional	1400	37.33%	1450	38.67%	2850	38.00%
10	Functional Hi Power	1	0.03%	0	0.00%	1	0.01%
2	Functional	9	0.24%	5	0.13%	14	0.19%
1	Good	0	0.00%	0	0.00%	0	0.00%
		3750		3750		7500	

Shorts failures are devices in which at least one power or signal lead draws more than 10ma at 100mv with all other leads at ground. Contact Failures are devices where at least one power or signal lead fails to conduct at least 50 microamps, even though mechanical contact has clearly been made between the probes and the chip. Functional devices have 256 independent working memory cells capable of storing both a one and zero logic state. Non-Functioning devices fail to meet the above criterion. Devices failing the maximum I_{DD} (108ma) or I_{DDA} (36ma) are binned at HI Power. A Good device passes all specified tests.

These memories were an encouraging start for our memory program. First, even though we anticipated a poor correlation between device models and actual FET characteristics, there were 14 functional devices. Second, the standard and rad hard designs had equivalent performance, so we concluded that the rad hard design enhanced radiation hardness without sacrificing manufacturing yield. The following two paragraphs elaborate on these conclusions.

Testing the PT-1 memory on the IDS-5000 e-beam prober revealed a problem with the row select-deselect timing. Contrary to simulation, these measurements showed multiple rows being selected, causing potential cell to cell interaction and upset of data. This is evidence that the device models were not giving us actual device size ratios that emulated real circuit performance.

A comparison of working cells for Rad Hard vs. Standard designs, at 50 MHz and 200 MHz, is shown in Figure 14. The first point contains the number of devices which had from 0 to 9 working cells, and the last point contains the number of devices which had from 250 to 256 working cells. Intermediate points are 10 to 19 ... etc. The number of working cells seems randomly distributed, with a slight increase at 220-256, and large number at zero. We believe that this is not due to processing failures. Rather, the problem is that the actual FET characteristics were not sufficiently close to the design targets. This figure also shows that standard and rad hard designs have equivalent yields.

2.6 PT-2M Memory (M. V. DePaolis, W. R. Ortner, and C. H. Tzinis)

Maskset PT-2M contained the second in our series of memories. The PT-2M memory was a 256 bit clocked SRAM with many of the features that would be incorporated in the 4K SRAM design. A block diagram of PT-2M is shown in Figure 15. This design was based on the SargicS.11 model files. The SargicS.11 models were expected to resolve the discrepancies between simulations and measurements that were seen with the PT-1 memory. In particular, input buffer minimum high levels (V_{ih} - min) measured 300 mV greater than the simulations used to design PT-1.

Three fully functional 256 bit arrays were found on the first wafer probed. Unlike the PT-1 memories, these three particular sites passed all up-down and disturb tests in the Teradyne test program. The circuits were tested in both the pipeline and ripple through modes. The cell array was found to be functional at 125°C. Cell to cell access time variation was about 300 picoseconds. Pipeline mode access time was 1.8 nanoseconds.

Three problem areas were discovered and addressed. We extensively probed internal critical circuit nodes. As in PT-1, special probe pads were added to the layout to allow for easy node access. During Teradyne and bench testing a problem was discovered with the Chip Enable Bar (CEB) circuit. The chip is normally active with CEB held "low". When CEB "high" is latched in, the data output driver is disabled. All circuits tested exhibited a problem where the output could be disabled, but not re-enabled. Fortunately the circuit always powered-up with the output enabled and we were able to test the memory. A WINDOW1 feature was found placed where a WINDOW2 feature should have been between METAL1 and METAL2 runners. The wrong window feature caused an open and prevented the CEB latch from being reset. An early GaAs version of GEMINI, our connectivity checking program, was used for checking PT-2M and failed to detect the open. The program has since been modified and this type of error is now detected. The window reticles were corrected.

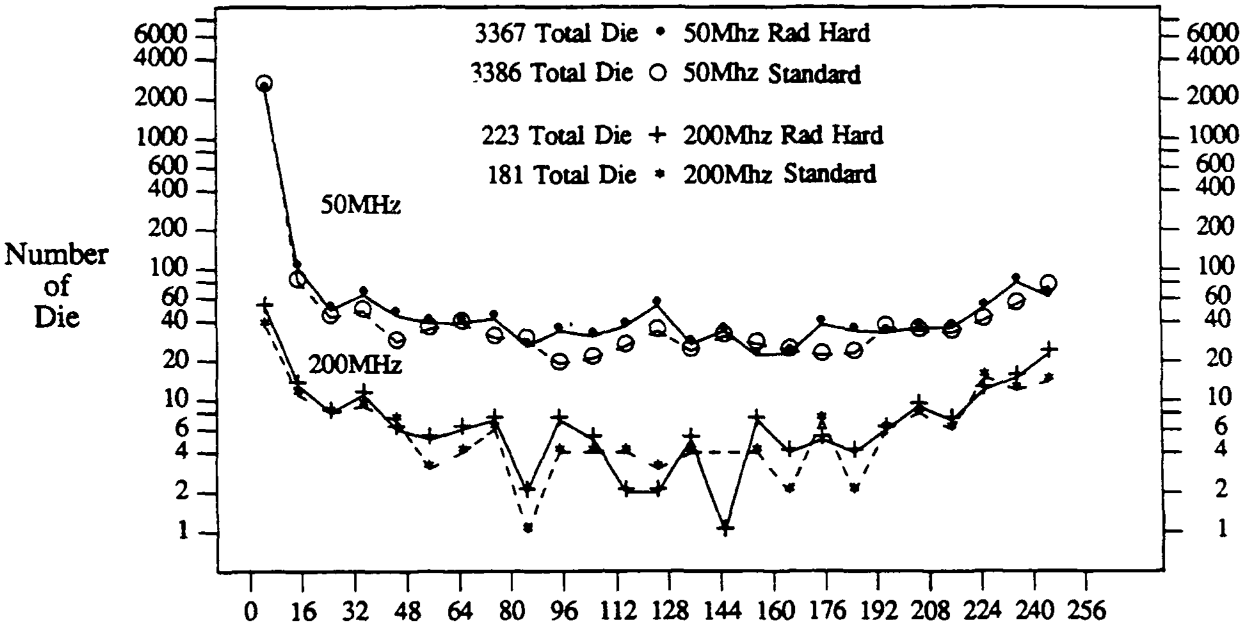


Figure 14 - Number of Working Cells in PT-1 Memories

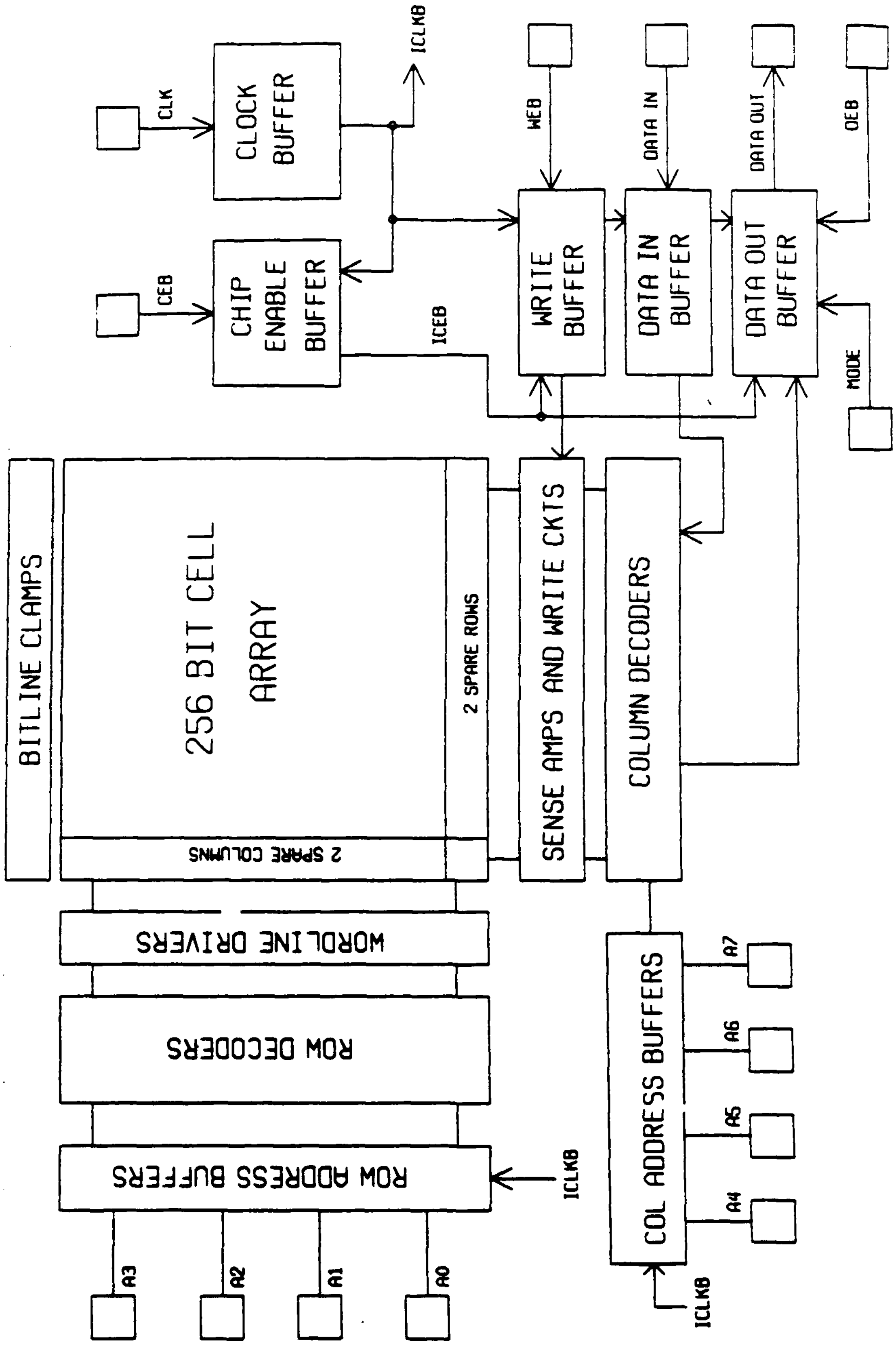

CLK
CLOCK BUFFER
ICLKB
CEB
CHIP ENABLE BUFFER
ICEB
WEB
WRITE BUFFER
DATA IN
DATA IN BUFFER
DATA OUT
DATA OUT BUFFER
OEB
MODE
BITLINE CLAMPS
256 BIT CELL ARRAY
2 SPARE ROWS
2 SPARE COLUMNS
SENSE AMPS AND WRITE CKTS
COLUMN DECODERS
WORDLINE DRIVERS
ROW DECODERS
ROW ADDRESS BUFFERS
ICLKB
A3
A2
A1
A0
COL ADDRESS BUFFERS
A7
A6
A5
A4
ICLKB

Figure 15 - Clocked 256-bit SRAM Block Diagram

The second problem was found while working on the bench test set. A number of memory sites were found where the data output "low" level was higher than expected; simulation results did not predict this finding. The output buffer is shown in Figure 16. Valid signal levels were measured at the input to this circuit. It was suspected that signal level on the gate of JQD24 was not low enough to shut it "off". This level is controlled, in part, by DFET JQD16. The layout of JQD16 is a 54 µm wide device broken into two 27 µm segments. Using a laser on a top metal runner, one of the segments was successfully disconnected on one site showing this problem. The site was retested and the output then reached a valid "low" level (<200 mV). The metal change was made on the top metal reticle and all subsequent PT-2M lots have this modification.

Third, we used liquid crystal techniques to locate hot spots in PT-2M 256-bit clocked SRAMs. Detailed visual inspection identified the hot areas as decoder circuits, especially the areas where top metal crossed over a bottom-metal-to-ohmic via. A new top metal reticle was generated to eliminate this crossing. Test results from wafers with this modification show no signs of shorts in the decoder area.

Wafer Test Results

We tested wafers in two major groups. During the six month interval of April through September, 1989, nine PT-2M lots with a total of 42 wafers were tested at the Cedar Crest Memory Test Facility. The 20 best wafers are shown in Table 8. All wafers were tested at 40°C; lots 32800 and 32880 had exceptionally good yield and were subjected to further testing at 80°C, 100°C, and 125°C. Access Time was found to lengthen significantly with increasing temperature; however, a total of 63 chips were still fully functional at 50 MHz and 125°C. No chips functioned at 200 MHz and 125°C. In Table 8, a functional chip is anything that works as a memory and passes the up/down test (that is, any chip in bins 1-27).

Between October 1989 and March 1990, another 21 wafers were fully probed. In this case, the devices were characterized according to how well they met the design requirements. At the lowest level, the memory simply had to work at some V_{DD} (1.8 to 2.2V), some V_{in} (0 to 1.2V), and $V_{out} = 0.6V$. At the other extreme, a "Bin 1" memory meets all requirements at 200 MHz. Two wafers had significant Bin 1 yields at 40°C: 33823 (9.2%) and 33824 (3.5%). See Table 9; "Bin 1" devices are indicated by entries in the right-hand column. All data in Table 9 are for 40°C, except that additional temperatures were used for wafers from lot 33820.

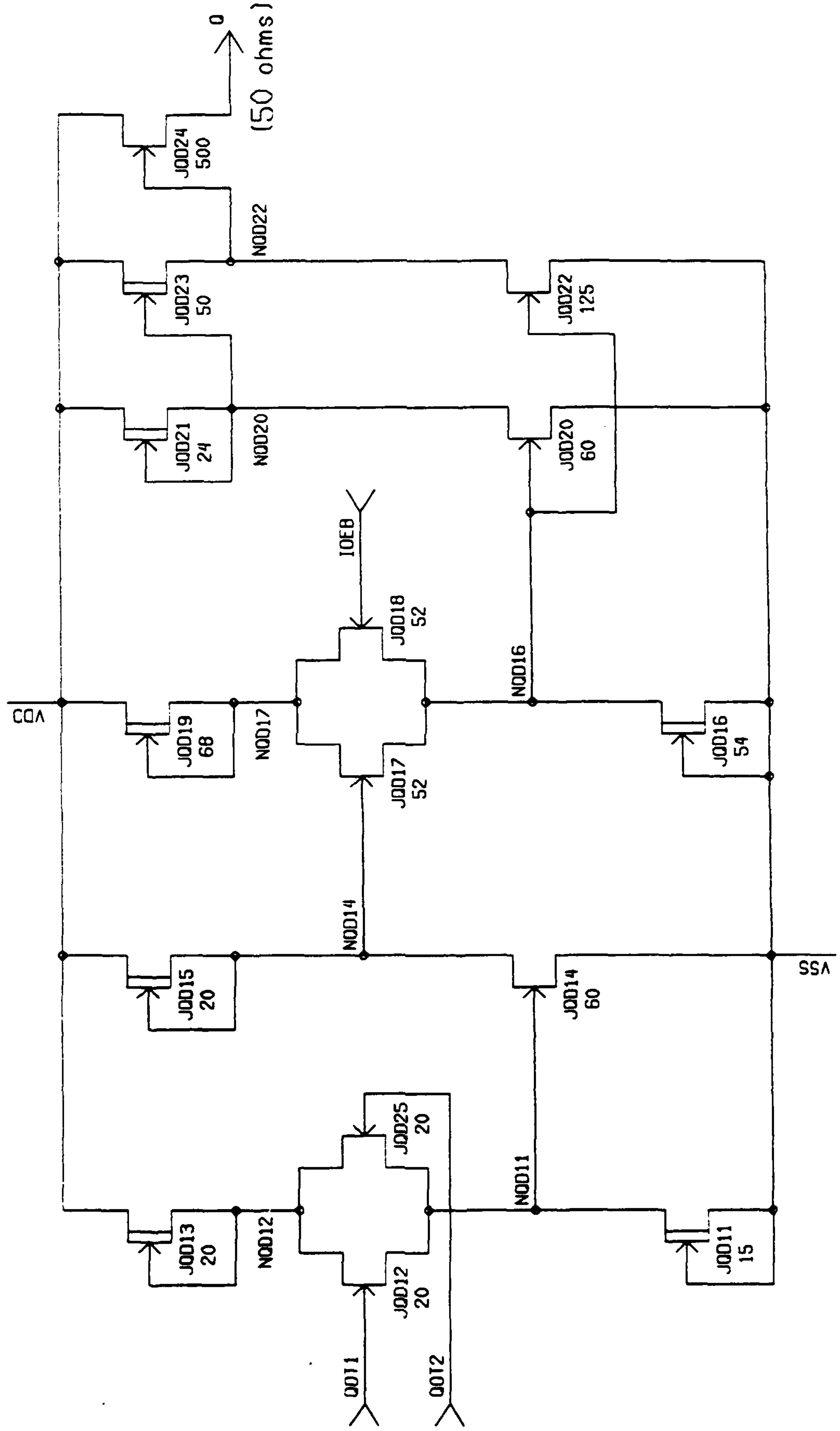

Q
(50 ohms)
JQD24 500
NQD22
JQD23 50
JQD22 125
JQD21 24
NQD20
JQD20 60
IOEB
JQD18 52
NQD16
VDD
JQD19 68
NQD17
JQD17 52
JQD16 54
NQD14
JQD15 20
JQD14 60
VSS
JQD25 20
NQD11
JQD13 20
NQD12
JQD12 20
JQD11 15
QOT1
QOT2

Figure 16 - Output Driver (PT-2)

Table 8 - PT-2M Wafer Test Results - April through September, 1989

Wafer†	°C	Number of Working†† Chips			
		Ripple		Pipeline	
		50 MHz	200 MHz	50 MHz	200 MHz
32503	40	34	3	13	9
32504	40	2	0	0	0
32505	40	5	1	1	2
32508	40	3	1	2	1
32691	40	4	0	4	2
32743	40	31	0	23	8
32792	40	18	0	3	0
32793	40	7	0	4	0
32794	40	6	0	1	0
32795	40	35	0	21	1
32796	40	19	0	10	0
32803	40	65	1	58	9
32803	80	61	0	57	0
32803	100	58	0	54	0
32803	125	32	0	30	0
32804	40	11	0	6	0
32805	40	8	0	1	0
32806	40	47	0	39	5
32881	40	180	35	170	47
32881	80	24	0	24	1
32881	100	1	0	1	0
32882	40	200	10	194	82
32882	80	178	15	176	21
32882	100	139	0	136	0
32882	125	7	0	8	0
32883	40	14	0	16	2
32883	80	24	0	24	1
32883	100	25	0	26	1
32883	125	21	0	25	0
32885	40	156	26	156	47
32885	80	40	2	36	16
32885	100	2	0	2	0
32885	125	0	0	0	0
32886	40	84	17	93	19
32886	80	41	0	43	3
32886	100	14	0	15	0
32886	125	9	0	10	0
Total @ 40 °C		**929**	**94**	**815**	**234**

†There are 543 chips per wafer.
†† Work at 40°C over the entire Power Supply Range (1.8V to 2.2V).
These are anything in Bins 1-27.

Table 9- PT-2M Wafer Test Results - October 1989 through March 1990

Wafer	°C	Meet Design Goals			
		Work	Power Supply	I/O Levels	Speed
33611	40	33	6	0	0
33612	40	51	13	0	0
33613	40	78	57	0	0
33614	40	38	26	0	0
33615	40	17	10	0	0
33616	40	61	42	1	1
33722	40	27	6	4	0
33723	40	15	1	1	0
33724	40	11	2	1	0
33725	40	67	25	18	0
33726	40	101	54	35	0
33823	40	174	161	130	50
33823	80	112	85	43	0
33823	100	47	33	9	0
33824	40	181	143	125	19
33824	80	191	166	111	3
33824	100	109	88	37	0
33824	120	95	81	1	0
33825	40	118	47	17	0
33825	80	60	14	0	0
33825	100	18	5	0	0
33825	120	7	2	0	0
33826	40	156	90	56	0
33826	80	54	17	1	0
33826	100	20	4	0	0
33826	120	2	0	0	0
34431	40	0	0	0	0
34432	40	0	0	0	0
34433	40	0	0	0	0
34434	40	0	0	0	0
34435	40	3	0	0	0
34436	40	0	0	0	0
Total at 40°C		**1131**	**683**	**388**	**70**

1. There are 543 chips per wafer.
2. Work - at some V_{DD} (1.8V to 2.2V), V_{in} (0V to 1.2V) and V_{out} .6V.
3. Power Supply - Work over entire V_{DD} Power Supply Range at the above V_{in} V_{out} Levels.
4. I/O Levels - Work over entire V_{DD} Range Vih (.3 to .9) and Vout (.2 to 1.0).
5. Speed - Meet all requirements at 200 MHz (i.e. Bin 1 Devices at the indicated temperature).

PT-2M Package Test Results

In each of the four quarters, we delivered to DARPA 20 of the best PT-2M devices available at that time. While all the delivered devices meet some of the requirements, March, 1990, was the first time all 20 devices met all requirements at 25°C.

PT-2M Package Results (Deliverables)

	Number of Bin 1's Delivered†				
	125°C	80°C	25°C	0°C	-55°C
June 1989	0	0	0	0	0
Sept. 1989	0	2	0	0	0
Dec. 1989	0	3	5	1	0
Mar. 1990	0	1	20	8	0

† Bin 1 Devices Meet all Requirements at 200 MHz.

Device Characterization

We used data from twenty delivered packages to characterize device performance and to relate performance to temperature and EFET threshold. As seen in Figure 17, Ripple Mode Access Time (Tar), which ultimately determines the maximum pipeline cycle rate, is a minimum at -55°C and increases gradually with increasing temperature until 80°C, where it increases rapidly beyond 5 ns. Speed and power are maximum at -55°C. (In this figure and Figures 18, 20, and 21, the dashed lines indicate the specification limits.)

In Figure 18, for 25°C, we show that access times and currents correlate well with EFET threshold. Devices having lower thresholds are observed to be faster and to consume more power. Since lower threshold results in higher drain current for a given drive level, this result is expected. The distribution of access time (Tar) indicates there will be some yield loss for 200 MHz operation.

The EFET threshold, measured at the open source DOUT signal lead, decreases with increasing temperature (see Figure 19). At first, this might seem incompatible with the observed speed and power sensitivity to threshold (i.e., speed and power are maximum at -55°C). however, other physical mechanisms, like free carrier mobility, come into play as temperature varies, and they dominate behavior with temperature.

Figure 20 shows the input and output voltages as a function of temperature. The minimum voltage for a logic "1" and the maximum voltage for a logic "0" are well within specification. That is, $V_{oh} > 1.0V$, $V_{ol} < 0.2V$. There is a problem with the input switchpoint. PT-2M was designed for a 0.6V switchpoint, but the SargicS.11 model was somewhat inaccurate. The actual switchpoint is about 0.8V, leading to some devices that fail the requirement for $V_{ih} < 0.9V$. (All devices pass the requirement for $V_{il} > 0.3V$.)

As shown in Figure 21, the input Setup and Hold Times generally meet the specification. There will be some yield loss for hold time.

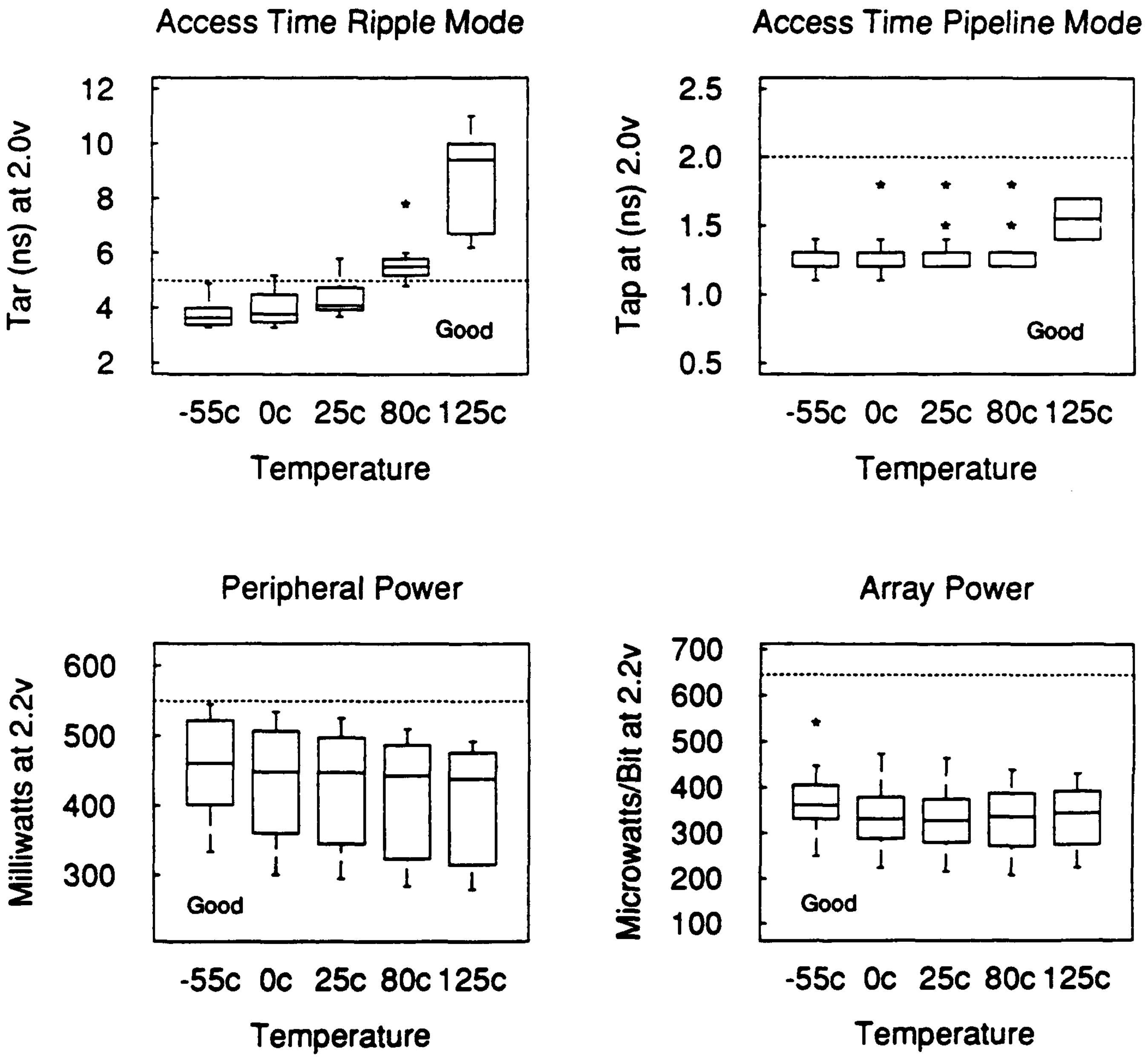


Figure 17 - PT-2M: Speed and Power vs. Temperature

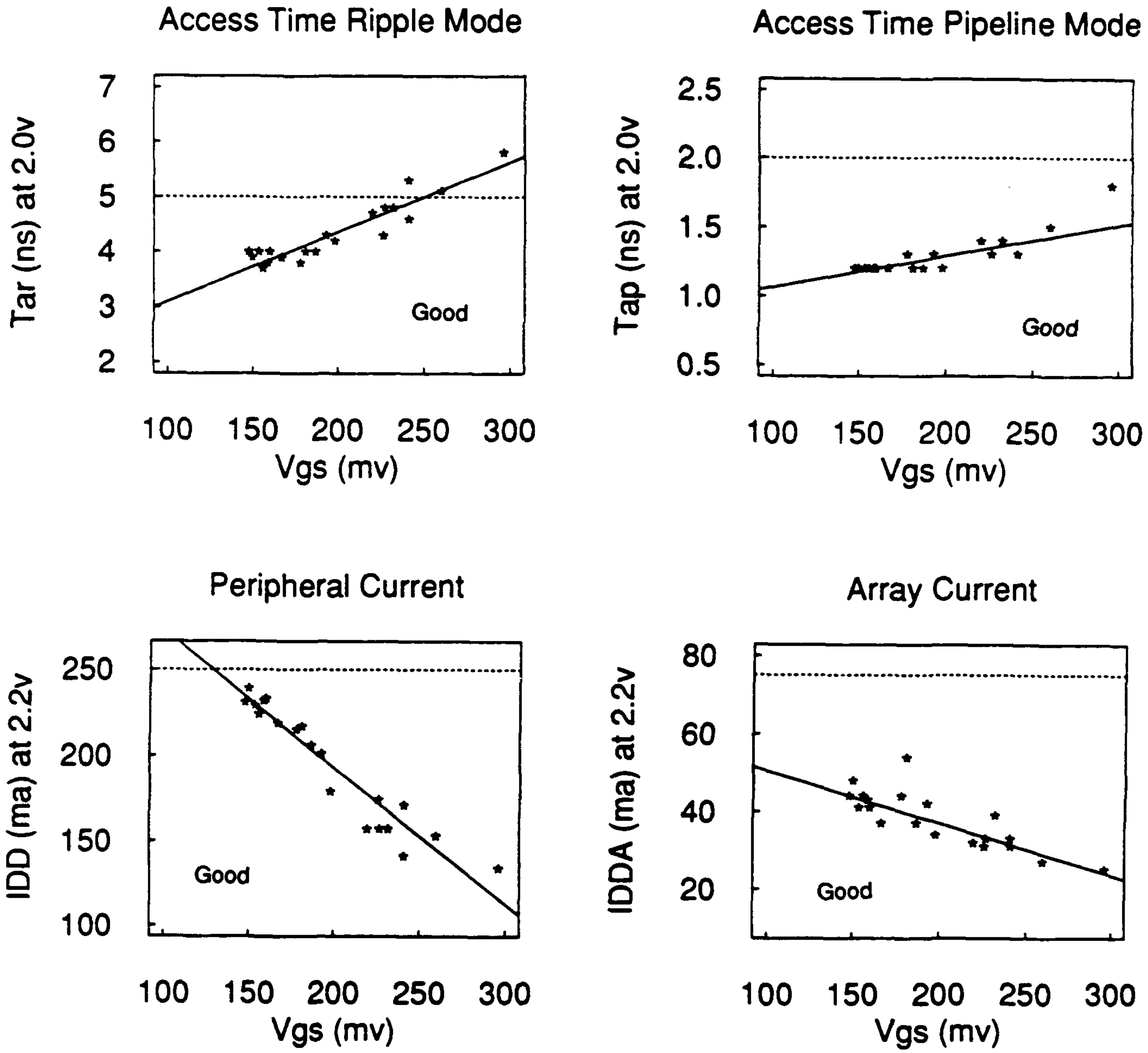
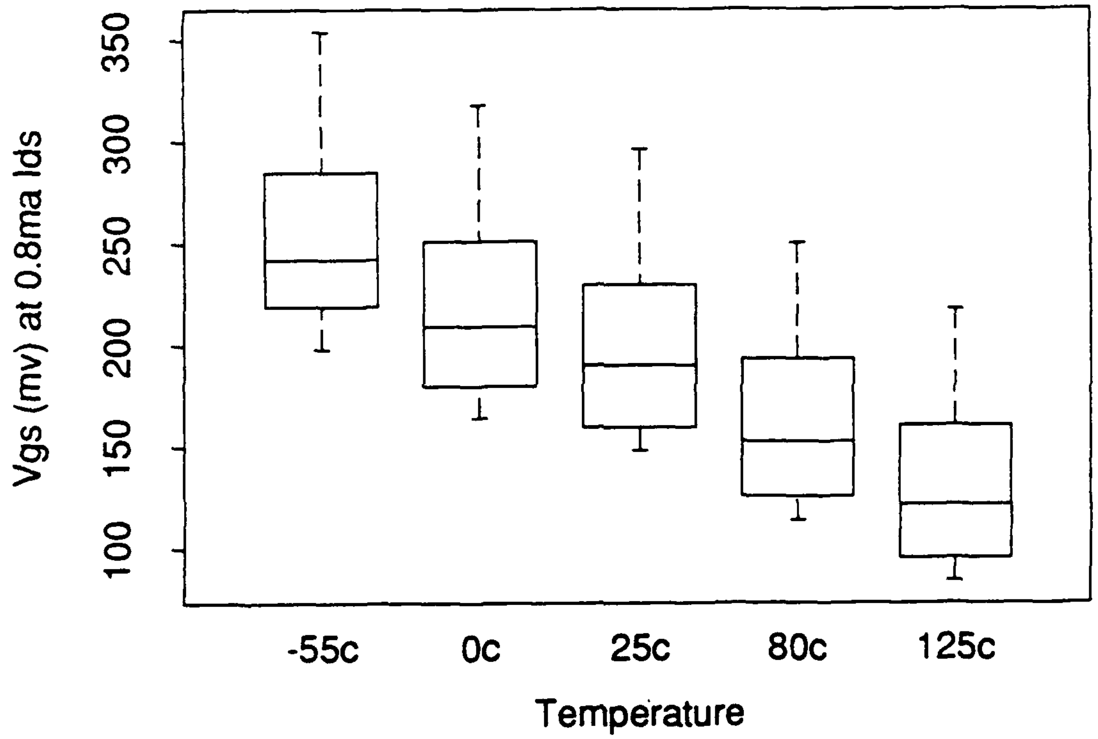
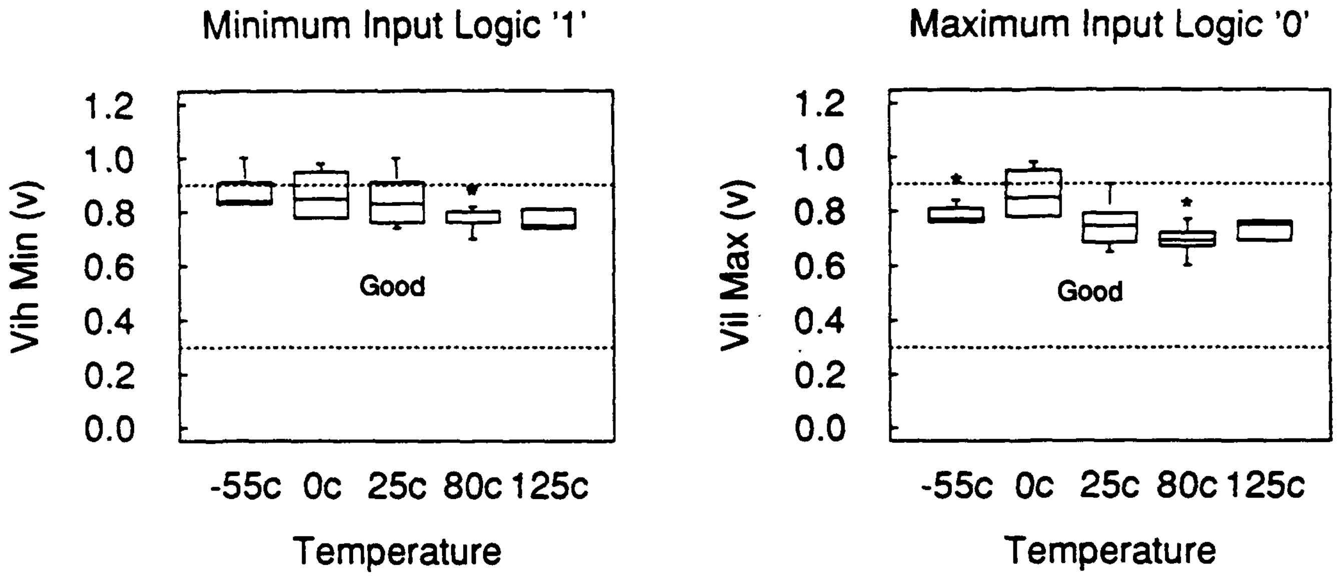


Figure 18 - PT-2M: Speed and Power vs. Effective Threshold (Vgs) at 25°C



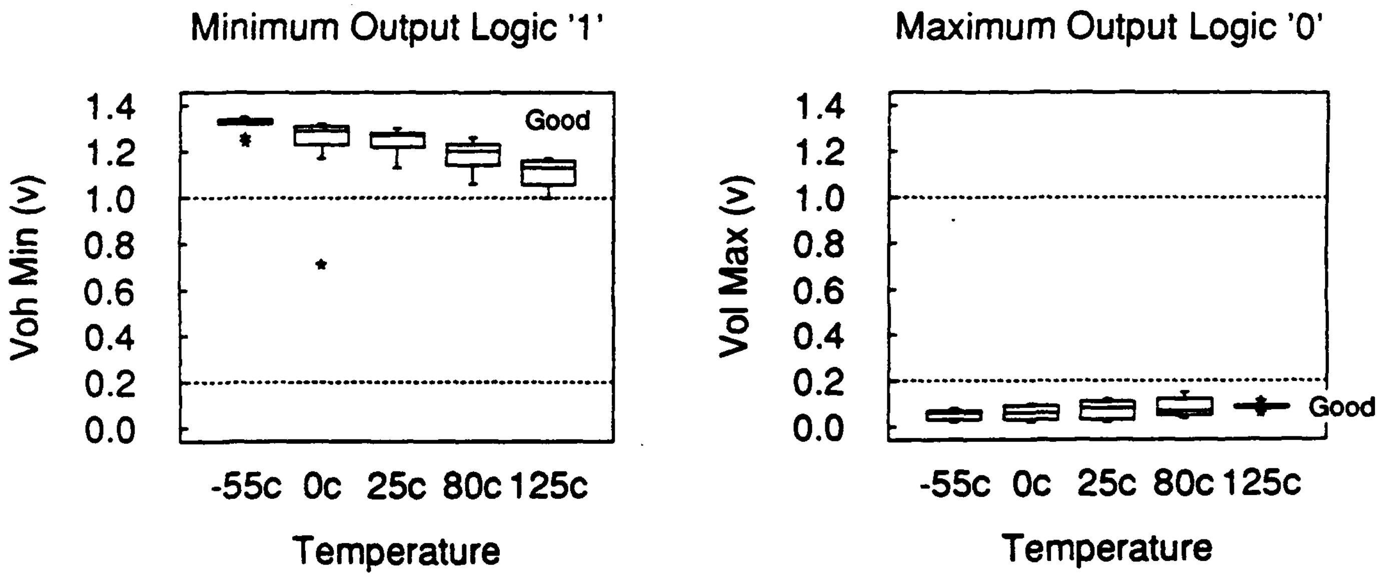
Vgs is Measured On Each Device Using The DOUT Signal Lead
(The Output is an Open Source EFET)

Figure 19 - PT-2M: EFET Effective Threshold (Vgs) vs. Temperature



Minimum Input Logic '1'

Maximum Input Logic '0'



Minimum Output Logic '1'

Maximum Output Logic '0'

Figure 20 - PT-2M: Input and Output Signal Levels vs. Temperature

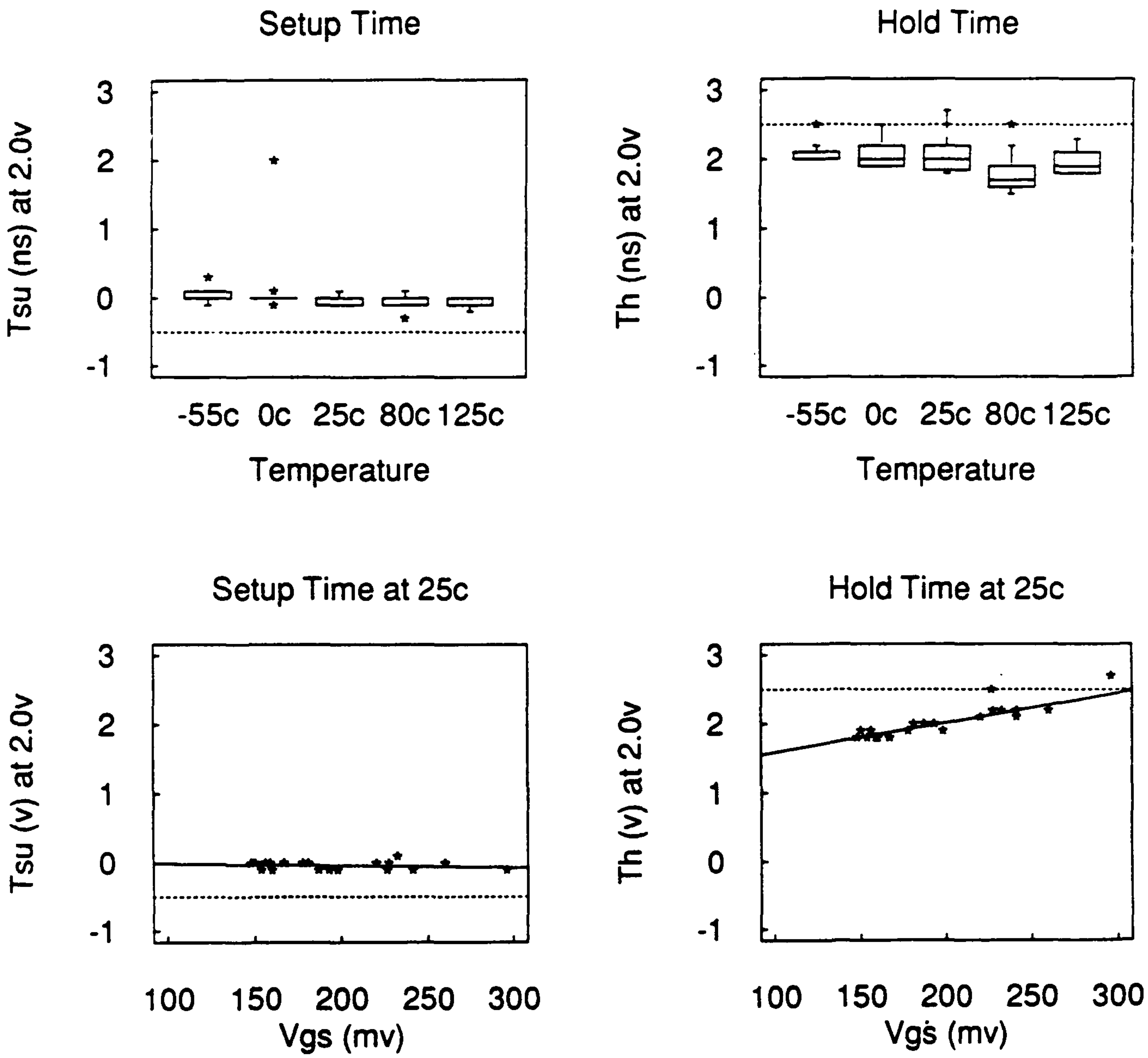


Figure 21 - PT-2M: Setup and Hold Time vs. Temperature and vs. EFET Effective Threshold (Vgs) at 25°C

PT-2M Device Performance vs. FET Characteristics

EFET and DFET data from PCM sites were plotted with PT-2M memory test results to characterize memory yield as a function of FET parameters. In Figures 22 and 23, the EFET and DFET saturation current (I_{ds}) and threshold voltage (V_{th}) are scatter plotted according to functional yield. In the upper left plot, each data point indicates PCM data on a wafer whose yield was ≥0; the lower right plot shows data for wafers with yields ≥50%. In each figure, the rectangle shows the design targets for Ids and Vth. In general, the highest yield wafers have data points inside the rectangles. This is strictly true for EFETS (Figure 22), and approximately true for DFETS (Figure 23). The discrepancy for DFETS indicates a shortcoming of the SargicS.11 model that was used to design the PT-2M memory. Empirically, the best yields are obtained when EFETs have $I_{ds} = 40$ mA/mm and $V_{th} = 260$ mV, and DFETS have $I_{ds} = 100$ mA/mm and $V_{th} = 550$ mV.

In Figure 24, the E/D current ratio is scattered plotted against Functional Yield and Ripple Mode Access Time. A smooth fit curve is shown. Both parameters are optimized at an E/D current ratio of 0.4.

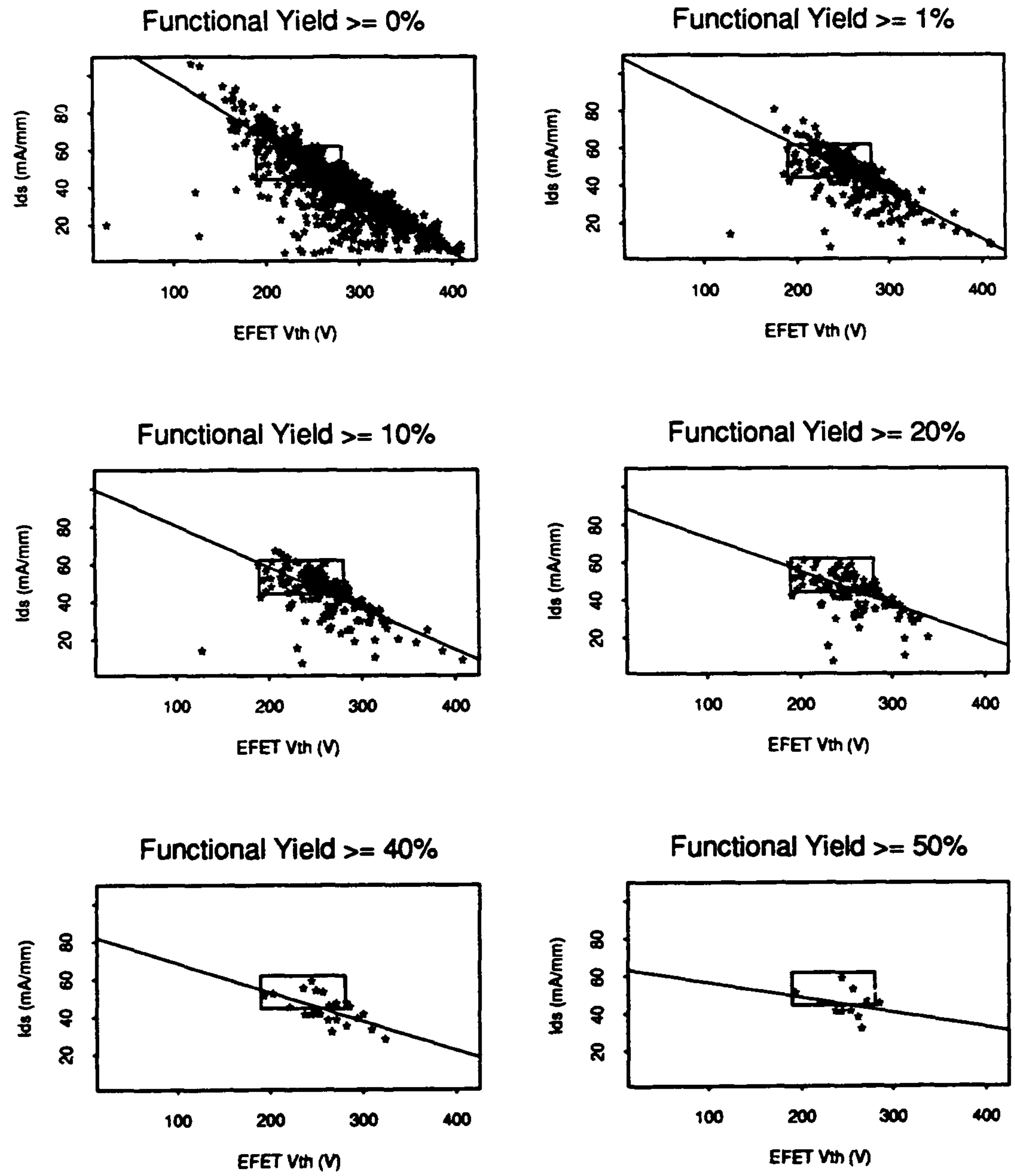
Toward the end of the PT-2M program, we ran additional simulations to discover why measurements of PT-2M circuits did not agree with the original simulation results. SargicS.15 models were used for these simulations. The switch point of an input buffer circuit was simulated under nominal conditions and found to be 0.75 volts. The measured switch point of PT-2M circuits with nominal processing was closer to 0.80 volts. Simulations run with the older SargicS.11 models (with which the PT-2M memory was designed) predicted a 0.65 volt switch point. This shows the inaccuracy of the SargicS.11 model predictions and gives more confidence in the SargicS.15 models which were used in the design of the 4K SRAM.

2.7 4K SRAM I - First Iteration (M. V. DePaolis, W. E. Werner, W. R. Ortner, and C. H. Tzinis)

Design Considerations

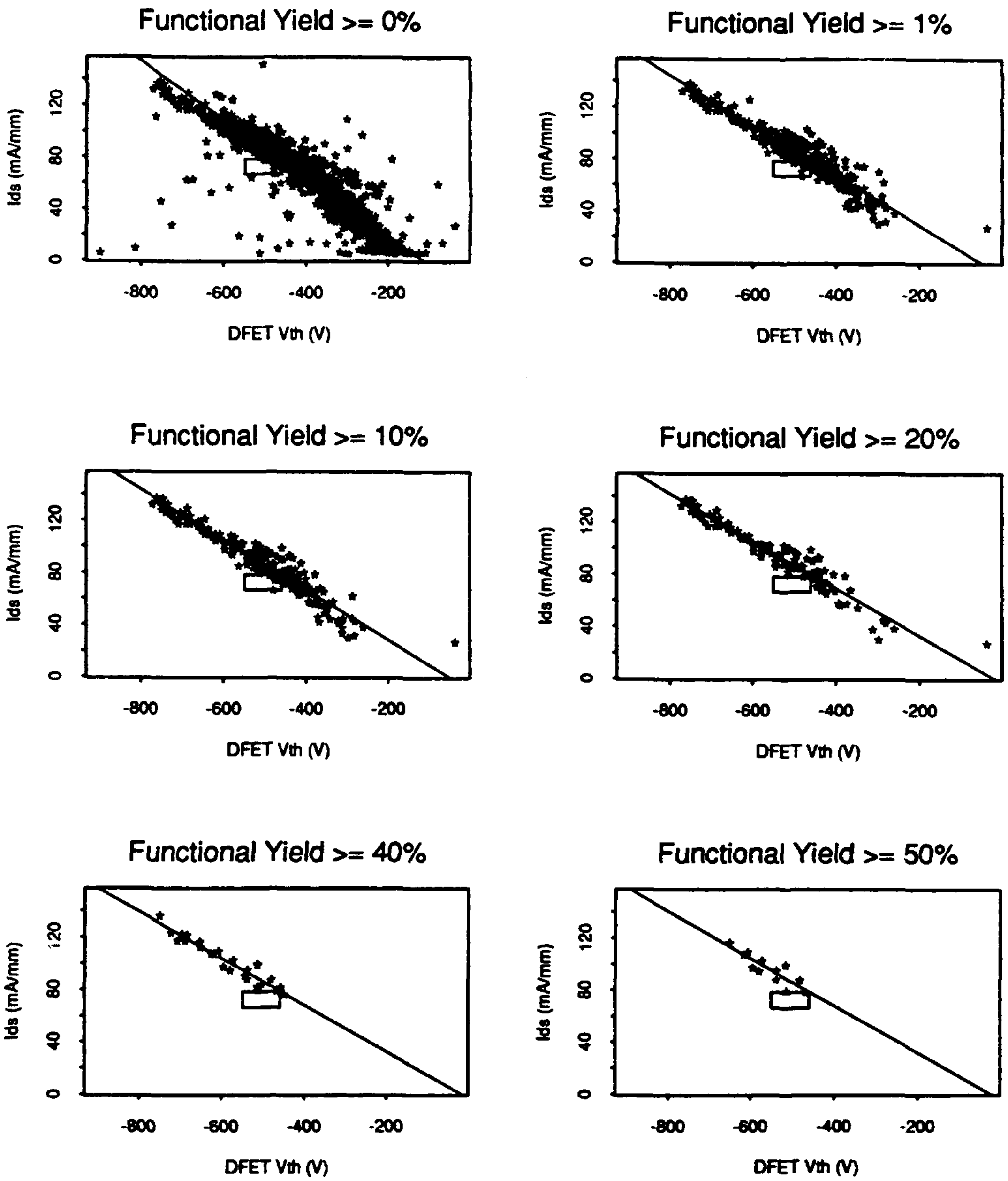
We based our initial design for the full 4K SRAM on the results we obtained from the PT-2M memory. Several architectural options were evaluated for the 4K SRAM. The final decision was to have each of the 4 array sections organized as 64 rows by 16 columns. A block diagram of the 1K x 4 clocked GaAs SRAM is shown in Figure 25. Another decision was to use only the radiation-hardened cell array, based on radiation test results from PT-2M. The cell size was increased to avoid areas where shorts or opens could occur because of top metal crossings.

Concerns about the output low level on PT-2M prompted redesign of the output driver section of the 4K SRAM. Also the write select circuit was modified to reduce the subthreshold leakage contribution of the write transfer EFETs. Full chip simulations were run on the 4K SRAM with layout extracted capacitance values. Some minor circuit modifications were needed to drive the capacitance load of long parallel runners.



Boxed Area is sargic.11 Model Values Used to Design PT-2M

Figure 22 - EFET Characteristics vs. PT-2M Yield


Functional Yield >= 0%

Functional Yield >= 1%

Functional Yield >= 10%

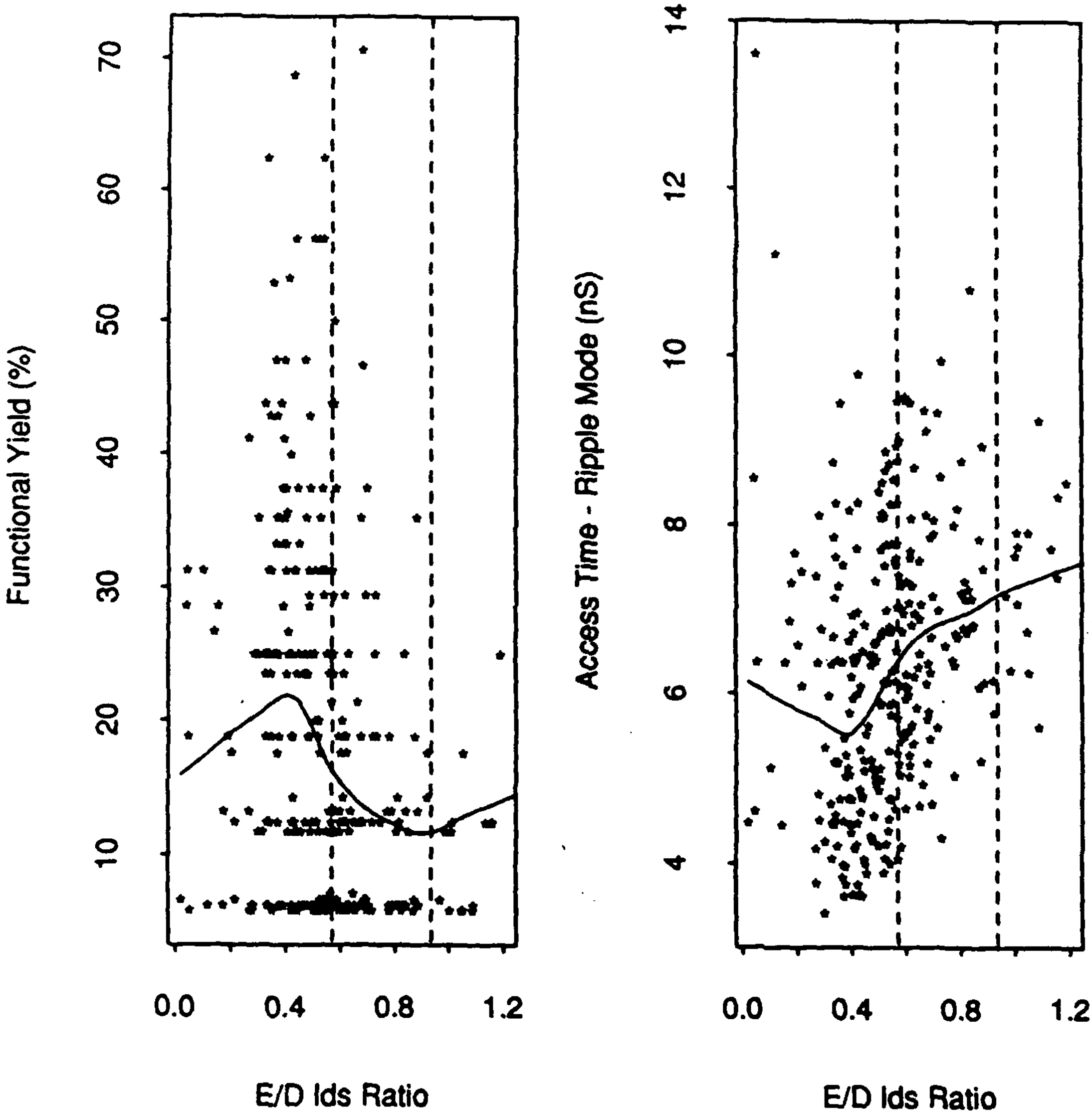
Functional Yield >= 20%

Functional Yield >= 40%

Functional Yield >= 50%

Boxed Area is sargic.11 Model Values Used to Design PT-2M

Figure 23 - DFET Characteristics vs. PT-2M Yield



Dashed lines are the sargic.11 model extremes used to design PT-2M

Figure 24 - E/D Ids Ratio vs. PT-2M Yield and Access Time

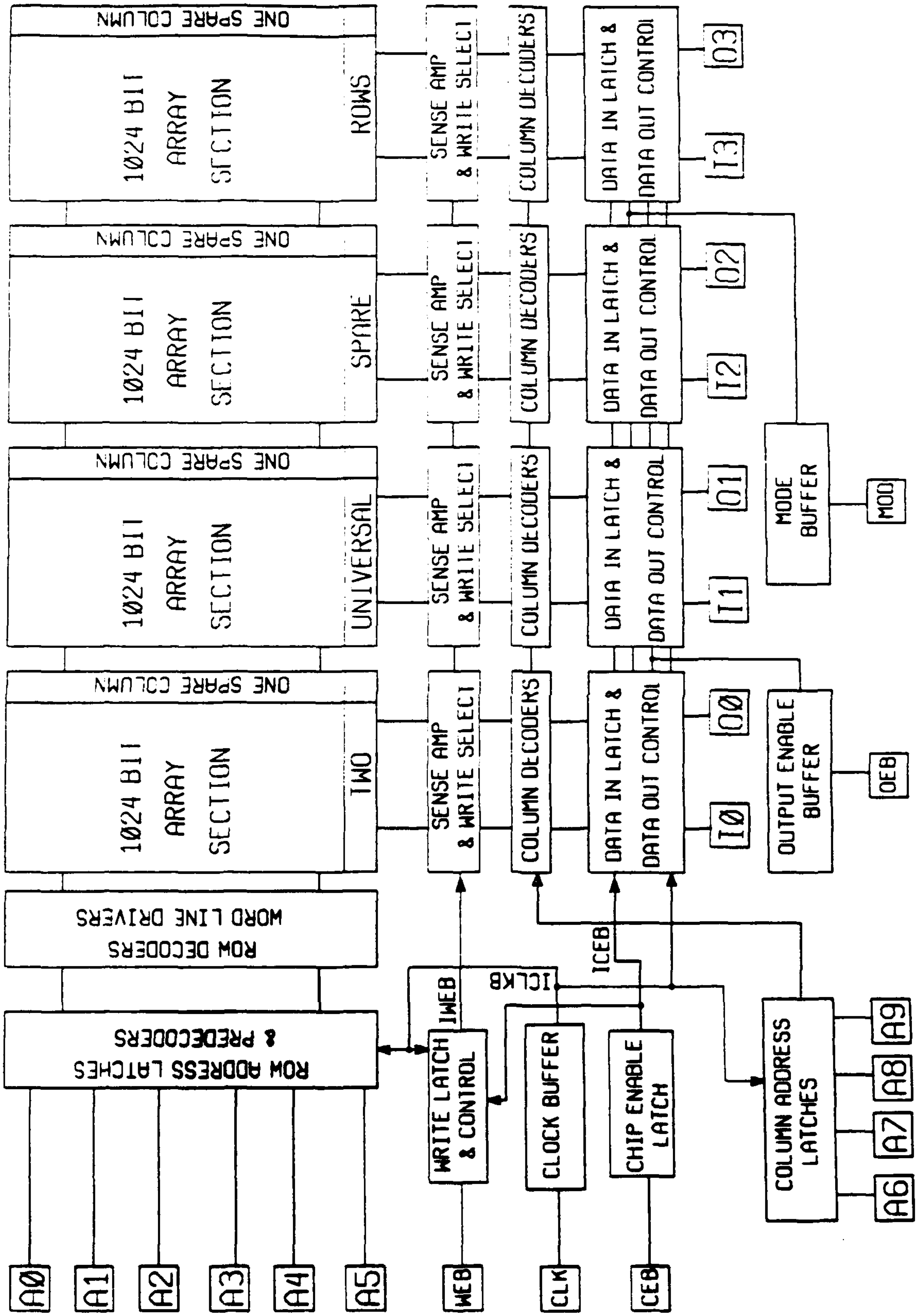

ONE SPARE COLUMN
1024 BIT ARRAY SECTION
ROWS
ONE SPARE COLUMN
1024 BIT ARRAY SECTION
SPARE
ONE SPARE COLUMN
1024 BIT ARRAY SECTION
UNIVERSAL
ONE SPARE COLUMN
1024 BIT ARRAY SECTION
TWO
SENSE AMP & WRITE SELECT
SENSE AMP & WRITE SELECT
SENSE AMP & WRITE SELECT
SENSE AMP & WRITE SELECT
COLUMN DECODERS
COLUMN DECODERS
COLUMN DECODERS
COLUMN DECODERS
DATA IN LATCH & DATA OUT CONTROL
DATA IN LATCH & DATA OUT CONTROL
DATA IN LATCH & DATA OUT CONTROL
DATA IN LATCH & DATA OUT CONTROL
O3
I3
O2
I2
O1
I1
O0
I0
MODE BUFFER
MOD
OUTPUT ENABLE BUFFER
OEB
ROW DECODERS WORD LINE DRIVERS
ROW ADDRESS LATCHES & PREDECODERS
IWEB
ICLKB
ICEB
WRITE LATCH & CONTROL
CLOCK BUFFER
CHIP ENABLE LATCH
COLUMN ADDRESS LATCHES
A9
A8
A7
A6
A0
A1
A2
A3
A4
A5
WEB
CLK
CEB

Figure 25 - 1K x 4 Clocked GaAs SRAM

Wafer Test Results

Three of the earliest lots had poor PCM characteristics and were used to debug the probe card, fixturing, and testing software. Some of the next lots had 40-80% PCM yields (the yield is the fraction of PCM sites simultaneously satisfying $40 < I_{dss}$ (EFET) < 70 mA/mm, $65 < I_{dss}$ (DFET) < 120 mA/mm, $2000 <$ via chain resistance $< 20{,}000$ ohms). Finally, many of the last lots had considerably poorer yields, as EFET threshold control was lost (see Section 4.3). We tested 1765 die from 32 wafers. The significant results are:

1. 70 dice have at least one working I/O section at some V_{DD} (2V ± 10%).
2. 3 dice are fully functional in Ripple Mode at some V_{DD} (wafers 35122, 35202, and 35626).
3. 1 die is fully functional in Ripple Mode over the entire V_{DD} range (wafer 35122).
4. Ripple Mode Access Time averages 8.9 ns with a standard deviation of 1.5 ns.
5. For input voltage, V_{IH} (min) averages 0.86V (the specification is $V_{IH} \leq 0.9V$).

Packaged Device Test Results

Twenty partially functional 4K SRAM I packages were delivered to DARPA. Thirteen of the packages had 90% of the bits working in Ripple Mode at $V_{DD} = 2.0V$ at room temperature and 50 MHz.

Failure Analysis of Shorts and Missing Bits

A memory is an ideal vehicle for assessing the defect densities in a wafer fabrication process. There is a high density of FETs, and the memory cells can be individually electrically addressed. In this batch of 4K SRAMs, we examined two significant causes of device failure: power supply shorts and missing bits.

Power Supply Shorts: The dominant failure mechanism for this group of 4K SRAMs was shorts between the V_{DD} and ground buses (see Table 10). Electrically, this appeared as a linear current-voltage characteristics and a low resistance when the circuits were examined on a Hewlett-Packard 4145 Analyzer. We used the liquid crystal technique developed for PT-1 to identify the location of the shorts. With the memory under low power, the liquid crystal apparatus showed dark regions where there was local heating. The shorts (dark regions) were defects where V_{DD} buses cross over the ground bus. (The two buses should be isolated by electric.) We stripped the dielectric and used an SEM to examine the defects and their relative location within the layer structure. Even after we removed the top gold metallization, we could not achieve an unambiguous chemical identification of the defects by using X-ray fluorescence. So we used a focussed ion beam to selectively ion mill vertical walled craters that revealed cross-sections of the defects. Most of the shorts are due to metal and dielectric particles. They are believed to be lift off residues and particles created by the dielectric deposition chamber. New guidelines have been established to minimize their presence.

Table 10 - Shorts in 4K SRAMs

Lot #	% Shorts
34720	88.5
34780	31.7
34910	53.2
35120	33.1
35200	11.0
35240	37.3
35620	23.0
35790	23.5

We can use a Y_0, D_0 model to estimate the density of these defects. For yield (Y), we use the equation

$$Y=Y_0\left(\frac{1-\exp(D_0A)}{D_0A}\right)^2$$

where we use D_0 = defect density, A = active area, and we use $Y_0 = 1$. The total area of the power bus crossovers is 2.55 x $106\mu m^2$. Experimentally, the average yield of sites without shorts is 68.2%. This gives a D_0 of about 15 cm^{-2}. This clearly indicates why we took action to reduce this particular type of defect.

Missing Bits: The automated memory testing produces maps which identify individual bits that do not function. By optical inspection, we found mechanical damage in bits that fail all tests (scratches, missing metal, defective patterning, particles). When a bit passed some tests and failed others, no visual defects were apparent.

2.8 4K SRAM II - Second 4K SRAM Iteration (W. E. Werner and W. R. Ortner)

Design Considerations

4K SRAM II was our planned second iteration of a 4K SRAM. Test results from 4K SRAM I showed that functional I/O sections existed over a limited temperature range. This limitation was found to be a direct result of subthreshold leakage of the wordline access transistors in the cells. As the temperature increases, the FET's threshold is reduced, and for a given gate to source voltage a higher subthreshold leakage current will be seen. When a cell's wordline access transistors cannot be properly shut off, cells in the same column will not be isolated from each other, and cell interaction will cause the memory to fail.

The goal behind the design of 4K SRAM II was to increase this operating temperature range to the full military specification range of -55°C to 125°C. This would require reduced subthreshold leakage on the wordline access transistors. One way to accomplish this was by placing a diode between the cells' pulldown EFETs at VSSA and the cell array's ground as shown by D1 in Figure 26. This raises all the cells' internal node voltages so that a negative gate to source voltage can now be used to properly shut off the wordline access transistors. Simulations with this circuit change indicated full functionality over the entire temperature range.

With just the addition of a diode per cell the whole chip would become much larger than 4K SRAM I, and in order to keep it at the same footprint at 4K SRAM I, two series 2/1μm DFETs were replaced by a single 2/2μm DFET in each cell leg as shown in Figure 26 by J4 and J5. (A 2/1μm *transistor size refers to a gate width of 2μm and a gate length of 1μm.)* A 2μm channel length transistor model was not immediately available for simulation purposes at the time 4K SRAM II was designed, so some alternative solutions were proposed. In the simulations, the square 2/2 device was simulated as a square 1/1 DFET. Based on prior experience in CMOS, it was believed that these two transistors' characteristics were a close enough match to use as pull-up, high resistance loads in the cell.

FET Data

Unfortunately, data obtained after 4K SRAM II fabrication shows greater variation in transistor characteristics due to channel length than was first assumed. In Figure 27 not only do we see a difference in the current carrying capability of the different channel length devices at $V_{gs} = 0$ volts, but we also see a positive shift in threshold voltage. So a DFET with a 1μm channel and a gate to source voltage of 0 volts would be ON hard, and a DFET with a 2 μm channel length may be just turning ON or may still be OFF.

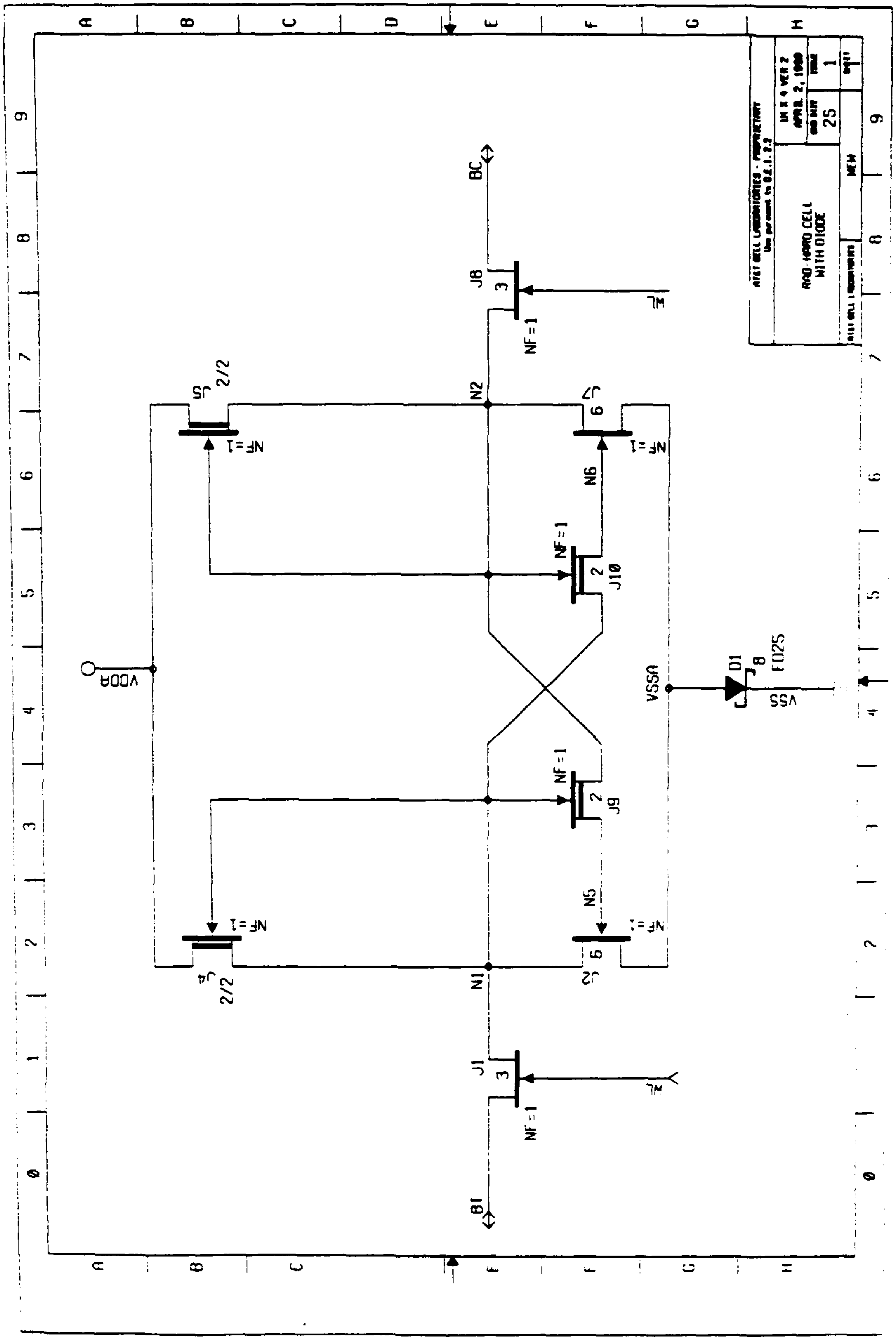
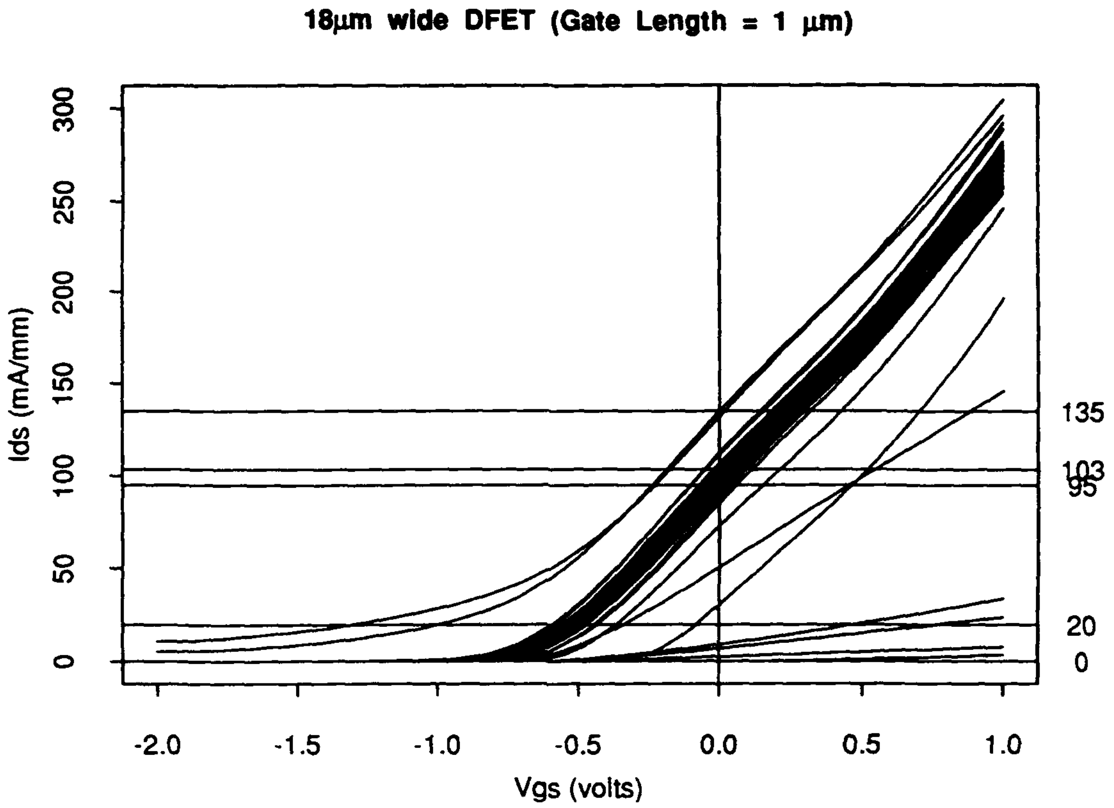

BC
BT
WL
WL
J1
J8
3
3
NF=1
NF=1
N1
N2
J4
2/2
J5
2/2
J2
6
J7
6
NF=1
NF=1
NF=1
NF=1
J9
2
NF=1
J10
2
NF=1
N5
N6
VDDA
VSSA
D1
8
FD25
VSS
RAD-HARD CELL
WITH DIODE
25
1
1
A
B
C
D
E
F
G
H
0
1
2
3
4
5
6
7
8
9

Figure 26 - Radiation Hardened Cell with Diode


18μm wide DFET (Gate Length = 1 μm)

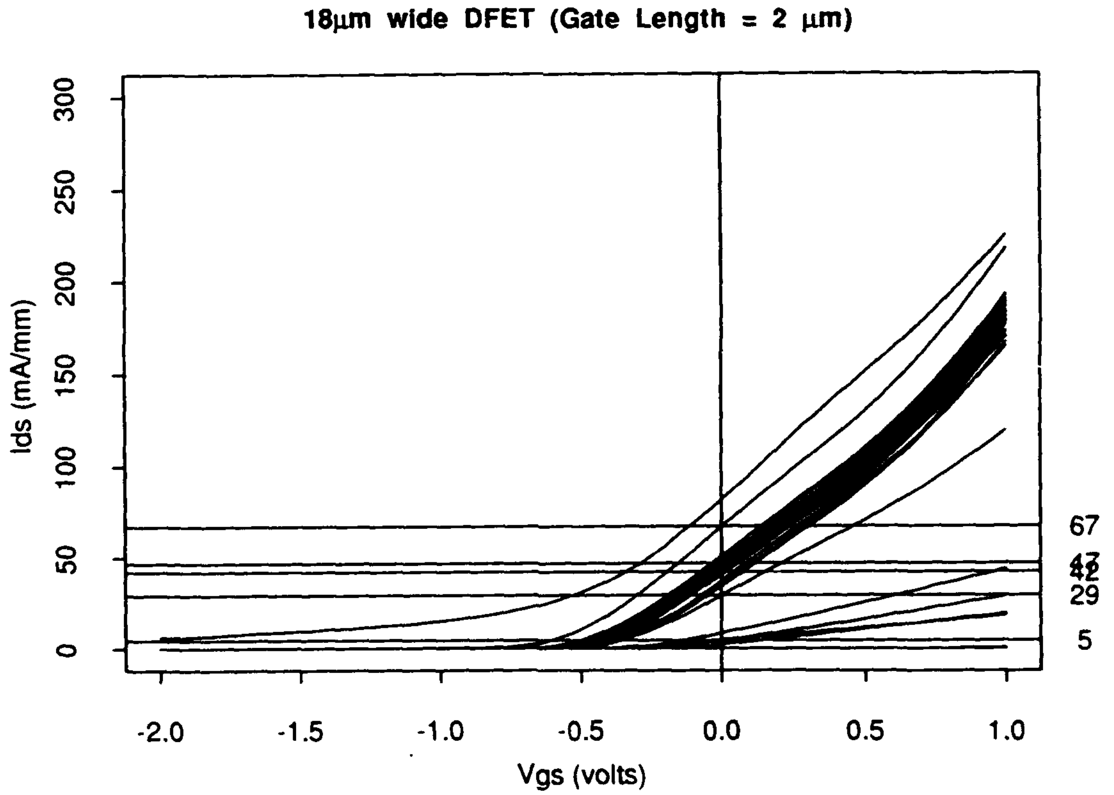

18μm wide DFET (Gate Length = 2 μm)

Figure 27 - Characteristics of 1μm and 2μm DFETs, showing 350mV Threshold Shift

When the memory cell array is full of very weak pull up DFETs, like what we can expect from these longer channel length transistors in 4K SRAM II, we can predict the performance of the memory chip. Since there is essentially no active pull up capability in the cell, a charge will only be held by the capacitance of the internal cell node. This capacitance is not very large, so the charge will dissipate after only a short time and the cell will lose its stored information. If the cell is ready very soon after a write, the data may be preserved. There will be no preferred state in this situation, so "hard, stuck at bits" will be difficult to find.

Testing and FMA

The test results from the Teradyne test system confirm this explanation of the non-functional 4K SRAM II memories. These results shown random bit failures where some bits will pass some tests and fail other tests. The bits do not always fail for just 0s or just 1s, so they can be said to have no preferred state. Each chip appears to have different bits bad for certain tests, and there are some tests for which all bits fail. This contrasts 4K SRAM I data where most of the bad bit failures fail all tests.

Physical Failure Mode Analysis (FMA) of these bit failures has uncovered no defects in the array which could cause failures such as the ones described, again contrary to what we observed in 4K SRAM I, where physical defects were found for cells failing all tests. Because this is a transistor performance problem on 4K SRAM II, it is unlikely that any physical defects exist in the area of failing cells.

No third iteration 4K SRAM is intended for this program. However, it is instructive to describe the lessons learned from 4K SRAM I and 4K SRAM II. In 4K SRAM I we had functional I/O sections, but a limited operating temperature range. The 4K SRAM II design addressed the temperature issue but has an unstable cell condition. To make a hypothetical 4K SRAM III operate as intended, three possible changes would be made. First, the two series 2/1 μm DFETs could be put back in the cell. Second, the 2/2 μm DFET's threshold and "ON" current could be adjusted. Or third, a different size DFET pull-up transistor could be used which more accurately resembles the two series 2/1 μm devices. The impact of going back to the two series DFETs has the obvious disadvantage of increased chip size but has the most promise based on what we have learned. The adjustment of the 2/2 μm DFET may be difficult to achieve without impacting other devices' performance. And using another size DFET would be an attractive option if a reliable model could be generated and simulated.

2.9 Laser Programming of GaAs Memories (R. T. Smith and F. H. Fischer)

To increase SRAM yield, each chip will have redundant sections which may be selected by laser programming. Experiments were conducted in June, 1987 to determine whether laser programming GaAs wafers posed any health and safety problems. The principal concern was that airborne particulates of inorganic arsenic bearing compounds might be generated by the interaction of the laser beam with the composite target structures on the GaAs wafers. Air samples close to the target area were collected while the Nd-doped YAG laser (1.064 μm wavelength) was programmed to shoot directly into the GaAs substrate at 5 times the normal operating power of 1μJ per pulse in a serpentine scan fashion for six hours at the rate of 20 shots per second. In spite of this, none of the air samples analyzed by the Environmental Engineering organization showed the presence of arsenic at or above the detection limit of 0.4μgram/cubic meter for the sample volume used. This is well below the OSHA standard of 5μgram/cubic meter. At a Safety Review, it was concluded that laser programming GaAs wafers should not pose any additional safety problems compared to normal laser operations.

The first PT-1 wafer used for laser programming had no passivating layer. This made it similar to unpassivated silicon wafers used in conventional laser programming of redundant memories. Unexpectedly, this wafer indicated that no useful processing window for laser energy exists for the break-link process without passivation. The gold metallization, whether BOTMET or TOPMET, horizontal or vertical, could not be reliably disconnected by the laser without significant shorting to the splash fence. Successful break-link processing requires a windowed passivation process to expose the target link metallization but provide a splash blanket over neighboring areas. This is illustrated for BOTMET in Figure 28. Results on wafers with this windowed passivation indicate a wide process window for laser pulse energy for horizontal link disconnect, whether BOTMET or TOPMET. The threshold energy is somewhat lower for BOTMET. Unfortunately, the process window for vertically oriented links is narrower and begins at roughly double the threshold energy (3µJ or more), resulting in sporadic excessive damage to neighboring areas. This orientation dependence has been observed to a lesser degree in aluminum and other link materials. Investigation showed that this orientation is due to asymmetry in the spatial profile of the focussed laser spot.

PT-2M wafers were routinely laser programmed for deliverables inventory and to provide models for radiation testing and reliability studies. Although the automated laser programming process was proved in on both Teradyne M118M and ESI 8000C laser systems, using repair menus generated off-line on the Teradyne J937 test system, the ESI equipment was used for the majority of the PT-2M models. Either system is capable of doing the job. Results on the best wafer so far, Number 32881, were as follows: Of the 274 functional chips (56% yield), 176 were initially functional, and 98 were successfully laser repaired from a potentially repairable population of 116. The repair rate was 84%, which is highly respectable in an off-line process which precludes the possibility of using spare replace spare techniques.

The final laser programming work focussed on modifying the existing process sequence in order to improve the laser link target structure and to simplify the associated wafer fabrication process. The previous process required two separate CAPS lithography and etch steps, and it produced wafers with a wide thickness variation in the dielectric which covers the link. This variation translated into a problem of inconsistent link burn quality. A modified process was tried on the wafers in lot 35850. The new process eliminates a deposition/lithography/etch step and yields a link structure with ~2000Å of overlying SiON. Targeting runs were made on a variety of chip sites on three different wafers from lot 35850 and were compared with wafers from previous lots. The link burns on the new link structure were more consistent, and they required less energy. Energy windows of 0.4µJ for horizontal links and 0.2µJ for vertical links were observed. An 8µm spot size and spot asymmetry compensation offsets were used on all samples in the comparison.

2.10 Gate Matrix CAD (Y. T. Oh)

An integrated set of gate matrix tools was developed for the physical implementation of GaAs IC circuits. Gate matrix is a symbolic layout style utilizing orderly structures where the gates of the devices are aligned in a single direction. The requirement of gate alignment in GaAs is particularly suitable for gate matrix design style. The symbolic approach isolates the layout from changing design rules as the technology evolves. The circuit design and layout can be done in parallel with the fine tuning of the technology, hence, shortening the development time for the implementation of GaAs circuits in the production line. An example of the gate matrix character symbolic is shown in Figure 29 together with its physical geometry.

The gate matrix design tools include symbolic editor, design-rule checker, symbolic-to-layout translator, gate-level extractor and layout-to-logic comparator. They are integrated in a single design environment called GASCAD residing on Sun workstations. This permits all the tools to be instantly available for operation on the layout through the use of menus. The integration of these tools has resulted in more power than from the sum of individual tools. Consequently, the complexity of the layout task has been simplified, and productivity increases.

The gate matrix design methodology includes many layers of verification to ensure error-free layout. The flow-chart of the methodology is shown in Figure 30. Starting with defined logic, in form of an LSL (Logic Simulation Language), the design flows into the gate matrix environment, GASCAD, where the layout is created in both symbolic form and geometric form named XYMASK. Before the symbolic is translated into XYMASK, a program, GASCHK checks for symbolic design rule violations. An electrical description of the layout in XYMASK is then extracted and converted into an LSL by the programs GOALIE2 and GASLSL. A program, LLC

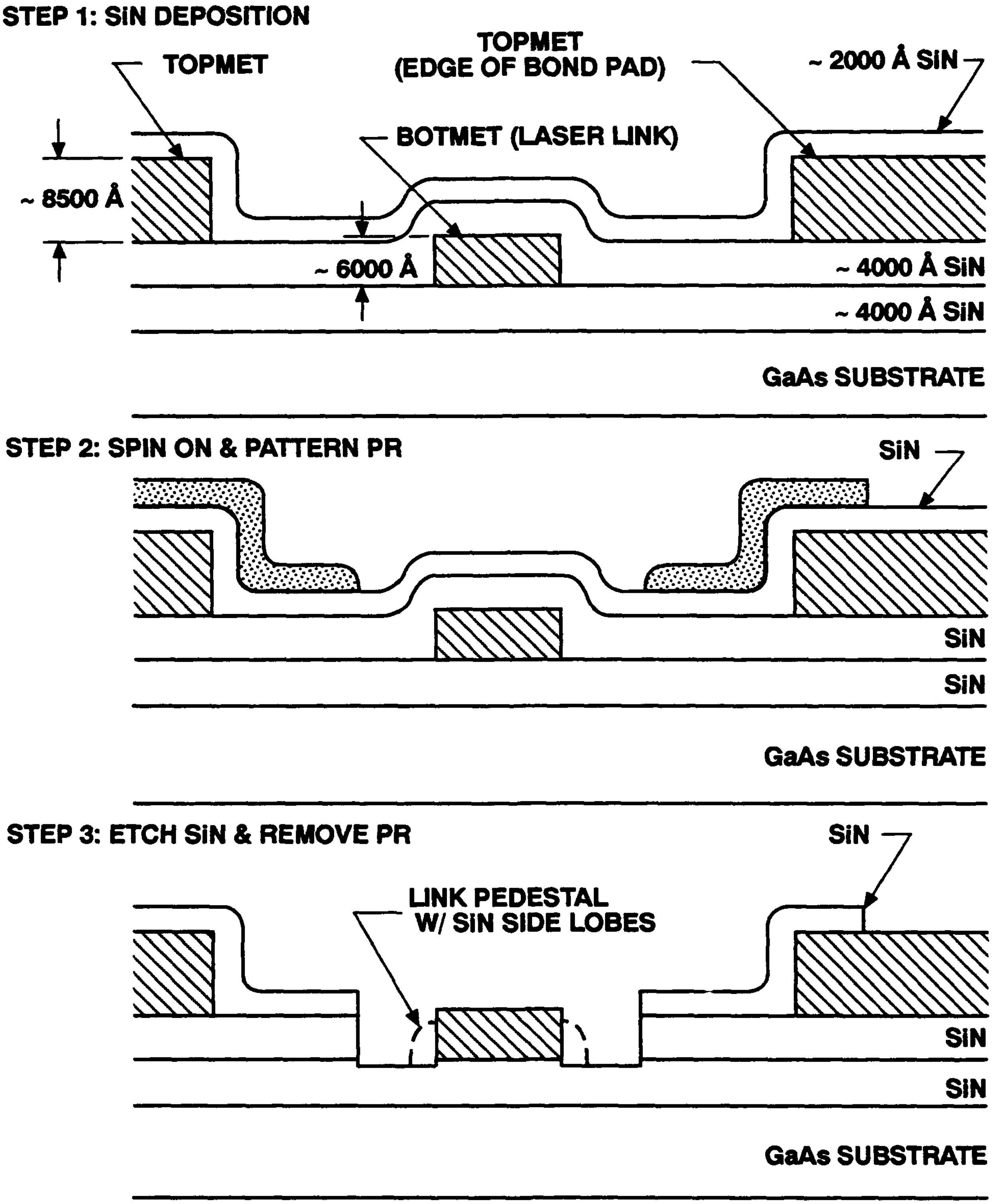
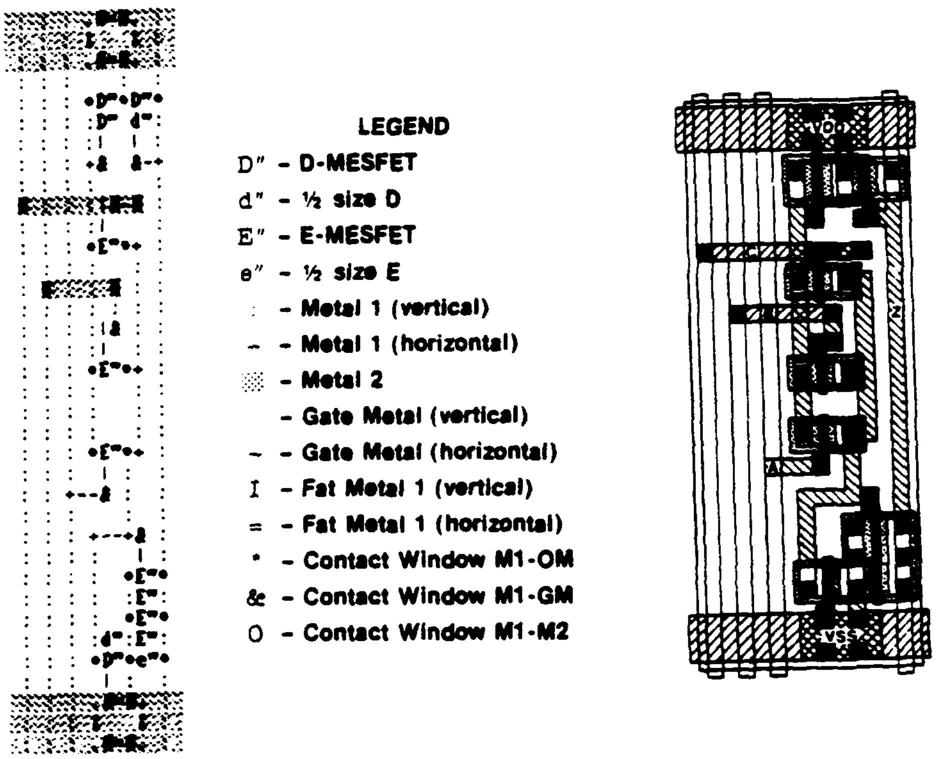

STEP 1: SiN DEPOSITION
TOPMET
TOPMET (EDGE OF BOND PAD)
~ 2000 Å SiN
BOTMET (LASER LINK)
~ 8500 Å
~ 6000 Å
~ 4000 Å SiN
~ 4000 Å SiN
GaAs SUBSTRATE
STEP 2: SPIN ON & PATTERN PR
SiN
SiN
SiN
GaAs SUBSTRATE
STEP 3: ETCH SiN & REMOVE PR
SiN
LINK PEDESTAL W/ SiN SIDE LOBES
SiN
SiN
GaAs SUBSTRATE

Figure 28 - Cross-section of Laser CAPs Process



LEGEND

D″ - D-MESFET

d″ - ½ size D

E″ - E-MESFET

e″ - ½ size E

: - Metal 1 (vertical)

- - Metal 1 (horizontal)

░ - Metal 2

- Gate Metal (vertical)

~ - Gate Metal (horizontal)

I - Fat Metal 1 (vertical)

= - Fat Metal 1 (horizontal)

• - Contact Window M1-OM

& - Contact Window M1-GM

O - Contact Window M1-M2

Figure 23 Gate Matrix Symbolic and Associated Physical Geometry

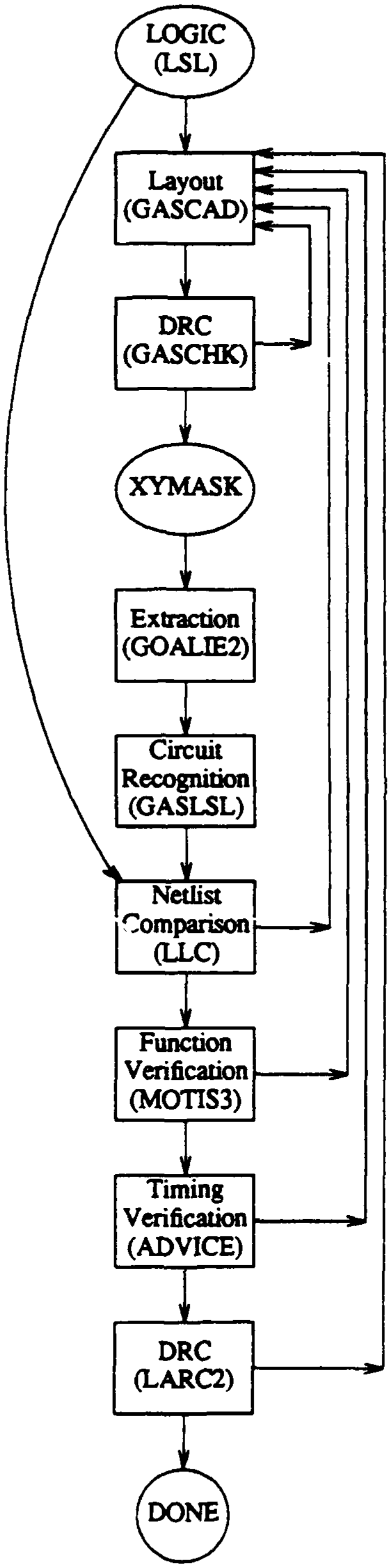

LOGIC
(LSL)
Layout
(GASCAD)
DRC
(GASCHK)
XYMASK
Extraction
(GOALIE2)
Circuit
Recognition
(GASLSL)
Netlist
Comparison
(LLC)
Function
Verification
(MOTIS3)
Timing
Verification
(ADVICE)
DRC
(LARC2)
DONE

Figure 30 - Gate Matrix Design Methodology

compares the original LSL with the LSL generated from the layout, and any discrepancies between the two LSLs are examined and corrected. When the logic is completely verified, the generated LSL is used for functional simulation using MOTIS3. The extracted transistor netlist and circuit parasitics are used in timing simulations with ADVICE. Finally, the entire geometry of the design undergoes design rule checking with the program, LARC2 before going to mask. The feedback loops are used until the layout is free of errors. With design rule checking, logic verification, functional and timing verification, the design should have no errors. Although the layout was created with frequent human interaction, the correct-by-verification principle used in the methodology insures right the first time design. The robustness of the methodology has been repeatedly demonstrated with the success of PT-1 and PT-2 logic circuits. This Gate Matrix CAD system was used both to design custom logic circuits and to design the standard cells and macrocells for the standard cell circuits.

2.11 PT-1 Logic Designs and Test Results (AT&T Logic) - (Y. K. Lo, W. A. Oswald, and E. K. Poon)

The PT-1 maskset contained our first small small logic circuits. PT-1 was the first step in an orderly sequence of increasing complex logic circuits leading up to the required 3000-5000 equivalent gate circuits. As both AT&T and Hughes were responsible for designing the required circuits, both companies design circuits for PT-1. AT&T's circuits included a full custom 6x6 multiplier, a standard cell 4-bit adder, and a cell array ring oscillator.

The 6x6 multiplier was designed 1) to obtain initial results on the design and fabrication capabilities of the GaAs technology for LSI circuits, 2) to prove-in the E/D SFFL family, and 3) to verify new Gate Matrix CAD tools which were tailored for GaAs IC design. The functionality of the multiplier is based on the Baugh-Wooley two's complement multiplication algorithm. The circuit was implemented with E/D SFFL logic family and designed with a full custom approach.

The multiplier was realized with 3072 transistors (465 gates). The longest delay path has 32 gates. To obtain optimal performance, the chip layout was hand-packed using the GaAs Gate Matrix CAD tools. The layout floorplan consists of 33 blocks. These blocks were carefully arranged to butt next to each other without using routing channels. This approach minimizes routing parasitics and reduces layout area. The layout was designed to fit into a 2.25mm^2 die area. A complete functional and timing verification was performed by GOALIE, MOTIS, and ADVICE tools. GOALIE was used to convert the layout from the geometrical data base back to a transistor level description that could be verified using MOTIS functional simulator and ADVICE circuit simulator. On-wafer 25°C test results show the chips are fully functional from 1.7 to 2.4 volts with a multiplication time of 7.0 ns, which is equivalent to a delay of 219 ps/gate at 0.92 mW/gate.

The 4-bit adder was an excellent vehicle for testing the standard cell placement and routing system, LTX2, as it relates to GaAs design. The adder is a conventional full adder with carry look ahead. The layout was constructed using the standard cell library developed at AT&T. One additional output was added to the circuit which (when fed back to the input) will cause the circuit to oscillate. The circuit contains 550 transistors (72 gates), and the longest delay path has 11 gates. The adder was successfully constructed using LTX2 and was verified using GOALIE, and ADVICE.

On-wafer 25°C test results show the chips are fully functional from 1.7 to 2.4 volts with an addition time of 3.12 ns, which is equivalent to a delay of 284 ps/gate. The static current could not be accurately reported because the adder shares the chip with other circuits.

The ring oscillator site consists of two ring oscillators, a 17-stage inverter ring oscillator and a 7-stage D-type flip-flop (with preset and clear) ring oscillator. Comcell is the basic structure of the cell array; it is capable of implementing an INRG gate and a NOR-3 gate. Six Comcells, arranged in a 3x2 matrix, are used to form an island. Nine islands are used in the chip. The resulting circuit has 514 transistors.

On-wafer 25°C test results from five good sites show a 0.2 ns variation for the oscillation frequencies. The highest observed oscillation frequency for the flip-flop oscillator is 7.4 ns, or 135 MHz. The average propagation delay is 530 ps/flip-flop. since the signal goes through three NOR-3 gates in the flip-flop, the delay for each NOR-3 gate is therefore 177 ps. For the inverter chain, the best observed oscillation frequency is 3.8 ns, or 268 MHz. The average propagation delay is 112 ps/inverter.

Hughes designed four circuits for the PT-1 test chip. Each was a *subcircuit* of the Casino Test Chip, the 3.7K gate standard cell circuit that was the first full scale logic chip designed under this contract. The Hughes PT-1 designs included: a 4-Bit Universal Shift Register, a 4-Bit Up/Down Counter, an 8-Bit Comparator, and a 16-to-1 Multiplexer. These ranged in complexity from 85 to 115 logic gates with the largest containing 682 transistors.

The ASIC design methodology used standard cells automatically placed in rows and routed using commercial layout design tools. The designs were performed on Apollo workstations hosting Mentor Graphics (schematic capture and logic simulation), SDA (place and route), ECAD (layout verification), and HSPICE (circuit simulation) software. All CAD databases were populated with GaAs SARGIC-HFET process design rules, simulation parameters, and standard cell symbolic and layout libraries. This effort helped validate the approach used to design the Casino Test Chip.

As shown in Table 11, four standard cell designs were found to be fully functional on the first wafer lot. The sequential circuits were functionally verified up to 80 Mbits/sec., and the combinational circuits were measured to have 4.5 nS total propagation delays. Average dynamic power dissipation contributed by both the chip's internal core and I/O circuitry varied between the four designs from a low of 90 mW to a high of 142 mW.

Table 11 - PT-1 Test Results (Wafer #1)

Circuit	Yield	Dynamic Power	Timing Data
PT-1MUX16TI	11/25	102 mW	Prop Delay = 4.5 ns ⇒ 222 MHz
PT-1COMP8B	11/25	90mW	Prop Delay = 4.5 ns ⇒ 222 MHz
PT-1USR	2/25	132 mW	Operates at > 40 MHz
PT-1COUNT4	1/25	142 mW	Operates at > 80 MHz

Table 12 shows the 1st set of DC functional yield data obtained from the first lot of wafers. The numbers represent high success in first time functionality on the first GaAs processing attempt.

Table 12 - DC Functional Yield

Wafer #	16:1 Multiplexer	8-Bit Comparator	4-Bit Counter	4Bit Univ. Shift Reg.
11214	11/25	11/25	1/25	2/25
11205	6/25	8/25	2/25	3/25
11212	18/25	7/25	1/25	1/25
11206	7/25	9/25	1/25	0/25
11208	4/25	11/25	0/25	1/25
11204	13/25	6/25	0/25	0/25
AVERAGES:	**39%**	**35%**	**3%**	**5%**

A total of 119 wafers were tested. A steady improvement in wafer yield was observed as more experience was gained in processing. In the final lots wafer lot yield of 10 sites (45.5%) was recorded for the 6x6 multiplier which has 3072 transistors. And wafer lot yield of 19.5 sites (88.6%) was recorded for the 8-bit comparator which has 412 transistors. Some of the functional chips were packaged in the TriQuint 44 pin package and delivered to DARPA. The performance of the packaged circuits was better than the wafer probing results because of a better testing environment. From these test results, the propagation delay through a gate was found to be 100-200 ps, which is faster than necessary to meet the minimal contract goals.

Besides the regular testing of wafers and packages, experiments on high speed testing were conducted. The 4-bit adder circuit has been tested successfully at 200 Mbps. Testing of packages over the high temperature region has also been done. Preliminary results indicated that the 4-bit adder circuit is fully functionally over the temperature range of 25-150°C.

2.12 PT-2 Logic Designs and Test Results (W. B. Leung, Y, K. Lo, W. A. Oswald, E. K. Poon, L. Ackner, C. E. Reid, and C. H. Tzinis)

The PT-2 Logic circuits were the second set of preliminary logic designs. They were divided between two masksets: PT-2L and PT-2M. The circuits, the source of the logic designs, and their gate counts are shown in Table 13. The four largest circuits went into PT-2L, and the two smaller test circuits went into PT-2M (which also contains testers for SRAM circuits).

Table 13 - PT-2 Logic Test Circuits

	Circuit	Logic Design*	Gate Count
PT-2L	ALU DEMO I	MDAC	2211
	Dual 8 x 8 Multiplier	ALC	1778
	Quad 4-Bit Adder	ALC	364
	Memory Tester	Mayo	1723
PT-2M	4-Bit Adder	ALC	96
	Programmable Multiplexer	ALC & RD	280

* MDAC = McDonnell Douglas, ALC = AT&T Bell Laboratories at Allentown-Cedar Crest, RD = AT&T Bell Laboratories at Reading.

The process tester PT-2L was implemented as a test vehicle for fairly large logic circuits with over 2K gate complexity. PT-2L was intended to expand on the results of PT-1, and to include more functions in each circuit. This enabled the designers to verify their CAD tools, the modeling of circuit behavior, the process control over a large die size, and the yield characteristics. With consideration of the optimal reticle size, the die size of PT-2L was chosen to be 5.1mm by 5.1mm. Four distinct chips, together with a process control monitor, were included in each reticle.

The ALU DEMO I was designed with the gate-matrix methodology. The logic design was done by McDonnell Douglas Corporation; it consisted of the ALU and the associated registers of a 32-bit microprocessor. Control signals and data path were included to facilitate the testing of the chip and the measurement of its characteristics. The dual 8 x 8 multiplier was an expansion of the 6 x 6 multiplier in PT-1. However, it was designed with the standard cell approach. Two multipliers were put into each die to increase the number of test circuits per wafer. This circuit provided a performance bench mark of the HFET processing and the SFFL logic family. The 8-bit multiplier has been fabricated in various processing technologies and logic families, and the results have been published in the past years. The quad 4-bit adder had the same logic function as the one in PT-1. However, it was designed in the cell array approach in PT-2L. Extra cell arrays were implemented to fill up all usable space, and it was used to try out the cell array CAD tools developed by Mayo Foundation. The memory tester was also designed with the gate matrix methodology. This chip was the portion of the original Casino Test Chip that was removed by Hughes when the Casino Test Chip was re-architected for use in Pilot Line III (see Section 3.15). It can test up to 8 byte-wide SRAMs with up to 64k address space. The programmable multiplexer performed parallel to serial conversion with serial output up to 2 Gb/s.

We tested 67 PT-2L wafers from 12 lots. Five of the tested lots produced working[2] devices and are summarized in Table 14. Processing information indicated that the EFET and DFET thresholds for the zero-yield lots were not within specifications, and this probably caused the poor wafer yield.

Table 14 - PT-2L Wafer Yield Summary for Logic Circuits

	Good Sites per Wafer			
Wafer #	8-Bit Multiplier	4-Bit Adder	Memory Tester	32-Bit ALU
31722	1	5	0	0
31723	2	7	0	0
31724	0	10	0	0
31871	7	11	0	6
31872	9	16	0	6
31873	16	14	0	8
31874	6	8	0	5
31876	0	2	0	1
31877	2	13	0	9
32231	1	2	0	0
32233-8	0	0	0	0
32401	1	0	0	0
32402	0	0	0	0
32403	5	6	0	0
32404	2	3	0	0
32406-8	0	0	0	0
32871	1	5	0	2
32872	5	5	0	7
32874	0	3	0	1
32875	0	2	0	1
32875	0	0	0	0

There are 30 test sites per device per wafer.

PT-2L lot 31870 required preconditioning before valid test data could be obtained. That is, each circuit had to be exercised with one or more sets of test vectors before data were actually taken. Only by doing this were the test results reproducible. Lot 31870 was the only PT-2L lot where this was required; other lots could be tested reproducibly without preconditioning, and preconditioning did not improve test results. At the time, we hypothesized that the FETs in lot 31870 had marginal characteristics, so that the temperature increase caused by preconditioning brought the FET characteristics closer to target and made testing more reproducible. Since no other PT-2L lots required preconditioning, we did not explore this phenomenon further at the time.

As will be discussed later, two other circuits required special treatment of their test vectors. The Standard Cell Casino Test Chip required the final test vector to turn off the internal logic. Otherwise, the temperature rise changed the circuit characteristics before it could be retested (Section 2.15). Also, the 32-Bit Multiplier required preconditioning in its early lots (Section 2.14). In the later lots, processing was improved so that small EFETs had the proper characteristics, and there was no longer a need for preconditioning.

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[2] Working means successfully passing all test vectors at 1 MHz at V_{DD} = 2.0V.

Tables 15-17 show test data for the PT-2L ALU, Quad 4-bit Adder, and Dual 8-bit Multiplier. The propagation delays are shorter than the program requirement by comfortable margins. The requirement is 200 MHz operation for 15-20 gate delays (5 ns propagation delay). We find 5.3 ns (189 MHz) for the ALU (33 gates plus input/output buffers), 2.3-3.3 ns (303-435 MHz) for the Adder (9 gates plus input/output buffers), and 7-10 ns (100-143 MHz) for the Multiplier (40 gates plus input/output buffers).

Table 15 - PT-2L 32-Bit ALU Wafer Test Results at 1 MHz

	Mean ± σ	
	LOT 31870	LOT 32870
Prop. Delay (ns)	NA	5.29 ± 1.07
Dyn. I_{DD} (A)	1.34 ± 0.19	1.57 ± 0.26
Min. V_{DD} (V)	1.94 ± 0.32	1.92 ± 0.16

Data were obtained from 4 wafers for lot 31870 and 4 wafers for lot 32870
NA: Not Available

Table 16 - PT-2L 4-Bit Adder Wafer Test Results at 1 MHz

	Mean ± σ		
	LOT 31720	LOT 31870	LOT 32870
Prop. Delay (ns)	3.34 ± 0.03	2.34 ± 0.06	2.95 ± 0.41
Dyn. I_{DD} (A)	411 ± 6.9	496 ± 67.5	736 ± 79.5
Min. V_{DD} (V)	1.59 ± 0.03	1.49 ± 0.03	1.60 ± 0.08

Data were obtained from 2 wafers for lot 31720 and 4 wafers for lot 31870 and 32870

Table 17 - PT-2L 8-Bit Multiplier Wafer Test Results at 1 MHz

	Mean ± σ		
	LOT 31720	LOT 31870	LOT 32870
Prop. Delay (ns)	10.28 ± 1.01	7.11 ± 0.67	7.92 ± 1.04
Dyn. I_{DD} (A)	1.04 ± 0.11	1.25 ± 0.19	1.71 ± 0.9
Min. V_{DD} (V)	1.82 ± 0.43	1.65 ± 0.09	1.93 ± 0.19

Data were obtained from 2 wafers for lot 31720 and 32870 and 4 wafers for lot 31870

Few of the tested devices conform to all I/O level requirements; the primary failure mode is high V_{ih}. There are two reasons for this. First, the input switch points were incorrectly simulated by the SargicS.8 model files used to design PT-2L; actual switch points are 0.2V higher than simulated. Second, during this period our DFETs had thresholds near -200 to -300mV instead of the -500mV design target. In combination, these two problems shift V_{ih} to unacceptable high levels. While PT-2L was being fabricated, we were already attacking these problems. We adjusted the MBE structure to bring the DFET threshold closer to target, and we tightened the growth specifications to reduce the DFET threshold variation. We also upgraded our models, ending up with SargicS.15. The improvement in simulation accuracy given by these models is discussed in Section 2.7.

Of the nine lots tested, there was no functional Memory Tester Chip. Failure mode analysis was performed using the Schlumberger IDS 5000 electron beam prober and the Advantest T3340 test system. We found the failure was a layout error in the B section of the clock/reset logic. There is identical clock/reset logic for section A. These clock and reset signals are used by two identical counters, A and B. A bug in the design rule checker allowed two metal runners butting at the corners to pass as a connection. At wafer fabrication, these two metal runners separated and became an open circuit. As a result, there was no clock signal to counter B, but the reset signal was present. The bug in the design rule checker was fixed and this problem should not occur again. Since this device was not a deliverable part to DARPA, a mask fix was not initiated.

In addition to testing the circuits on the PT-2L reticle, a brief investigation was made on the two PT-2M logic circuits. Both the 4-bit adder and the programmable multiplexer were found to be working on the one wafer which was probed.

Data for packaged devices are shown in Table 18. Some of these devices were delivered to DARPA. All of them worked over the temperature range of -55°C to 125°C. Again the propagation delays are shorter than the program requirement by comfortable margins. Likewise, all the circuits work at or below the required $V_{DD} \leq 2.0V$.

Table 18- PT-2L Package Test Results (25°C)

Circuit	Wafer #	# of Pkgs	Average Propagation Delay (ns)	Average Performance (MHz)	Average Dynamic Current (A 1 MHz)	Minimum V_{DD} (V)
32-Bit ALU	31872	3	NA	NA	1.15	1.59
	31873	4	NA	NA	1.40	1.59
	31874	3	NA	NA	1.30	1.60
	31877	4	5.5	180	1.39	1.88
4-Bit Adder	31872	4	3.8	260	0.49	1.39
	31873	4	3.6	280	0.64	1.47
	31877	5	2.3	440	0.66	1.65
8-Bit Mult.	31873	9	7.7	130	1.37	1.63
	31874	2	8.2	120	1.39	1.68
	31877	1	6.9	150	1.41	1.69
	32403	2	6.4	160	1.36	1.69

NA: Not Available

2.13 Custom ALU Circuit Design and Test Results (K. W. Teng, A. Hu, W. B. Leung, T. C. Poon, L. Ackner, and C. H. Tzinis)

The custom ALU is a test circuit with about 3500K gate complexity. The logic design of this circuit was supplied by McDonnell Douglas Microelectronics Center. It consists of a 32-bit ALU, two sets of 32 x 5 input registers, and a 32-bit output register. Pre-layout simulations showed that the maximum operating frequency of this chip was higher than 200 MHz. This circuit was intended to expand on the results of PT-1 and PT-2L, and to include better marginality as well as better circuit performance.

This ALU contains a 32-bit adder and a 32-bit logic unit. All logic operations are performed on 32-bit operands. Various enhancements were added to this custom circuit to ensure adequate circuit yield, high speed performance, low power consumption, and good reliability. These include the better optimization of noise margins with current technology, the implementation of faster as well as less process sensitive logic gate designs, and the suppression of the L DI/DT noise generated in the I/O buffers. In addition, with a divided routing/clock driver architecture, we were able to reduce the metal bus loading on the clock driver and to further enhance the circuit performance.

This ALU was designed with the gate-matrix technology. Layout of the circuit was then verified using the CAD tools such as GASCHK, GOALSL, LLC, and MOTIS3. Pre-layout and post-layout timing simulations were studied, including all critical path delay times. The pre-layout simulation results showed that this circuit could perform very well to meet DARPA's Statement of Work requirements: 200 MHz operation, assuming a pipelined chip design with 15-20 cascaded gate delay stages, with each gate driving a load of at least three similar gates.

The post-layout simulations included parasitics obtained from the whole chip layout. I/O registers, clock-drivers and the whole critical path were simulated to ensure that the maximum operating frequency of this chip will meet DARPA's performance requirement. The IR-drops on both VDD and V_{SS} power busses were analyzed using ADVICE, and were less than 75 mV. Simulations of 40 output buffers switching simultaneously at a frequency of 200 MHz were also performed to study the ground-bounce on the I/O buffer power rails, and the results were acceptable. A summary of important data of custom ALU is listed below.

Inputs	78
Outputs	34
V_{DD}/GND pins	68
Logic Gates	3571
Transistors	25,903
Estimated Power Dissipation (with all outputs open)	2.7 W

We started 19 6-wafer lots of custom ALUs. Several with particularly poor PCM[3] had zero circuit yield. Table 19 shows data for five lots that yielded working circuits.

Table 19 - Custom ALU Wafer Yield Summary

Lot Number	Functional Sites	Total Sites	Functional Yield	PCM Rating
33810	47	459	10%	8/144 = 6%
33970	11	255	4%	15/80 = 19%
34050	8	255	3%	11/80 = 14%
34340	1	204	0.5%	1/64 = 2%
34600	2	153	1%	1/48 = 2%

These circuits dissipate an average 2.2W (vs. 2.7W simulated at 2.0V), operate in the 1.8V-2.2V range, and are tested at controlled temperatures. One surprising outcome of the investigation was the presence of holes in the shmoo plot of any I/O parameter vs. V_{DD}. Its immediate impact is manifested by irreproducible I/O level measurement; therefore, we currently read the I/O levels directly from the shmoo plot of the I/O voltage vs. V_{DD}. A possible culprit was sidegating, and our new MBE structure that suppresses sidegating was expected to alleviate the problem in future circuits. Selected devices that were packaged for the December, 1989 and March, 1990 deliverables show that the primary failure mechanisms were low V_{oh} and marginal V_{il} and V_{ol} (Figure 31). These observations are similar to the 1K Cell Array results and are mainly due to buffer design; the marginal V_{ol} is due to FET turn on characteristics.

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[3] PCM yield is the fraction of PCM sites that simultaneously satisfy 100 < via chain resistance , 20,000 Ω, 40 < EFET I_{ds} < 70 mA/mm, 65 < DFET I_{ds} < 120 mA/mm.

2.14 Custom 32-Bit Multiplier Circuit Design and Test Results (L. R. Tate, R. J. Niescier, L. Ackner, and J. Scorzelli)

For the second full custom circuit, we chose a circuit which addresses a data processing bottleneck in high performance scientific workstations: namely, the floating point multiplier. The floating point multiplier used in the design of high performance floating point processors cannot be pipelined without loss of system performance for applications with dataset dependencies. Therefore, it has an inherent high gate depth and hence low I/O bandwidth. The I/O bandwidth allows the use of this gallium arsenide circuit to improve the performance of a practical system composed primarily of mainstream MOS and ECL integrated circuits.

The 32-bit IEEE Floating Point Multiplier accepts two 32-bit floating point basic single IEEE format operands and generates a 32-bit IEEE format product in less than 15 nanoseconds (67 MFLOPS). The 50,000 transistor chip may be used as a building block in floating point systems which support IEEE standard 754 or as a multiplier in signal processing systems. Referring to the architectural block diagram of Figure 32, note the flow-through architecture employed to minimize total latency and thereby allow full performance even in applications with dataset dependencies (registers are used only on the inputs and outputs). Booth recoding is employed to reduce the number of partial products and thereby reduce circuit complexity and power consumption. To obtain absolute maximum speed without sacrificing layout regularity, a binary tree of 4-2 adders is used to reduce the Booth recoded partial products. This results in a time optimum (proportional to Log n) architecture. Features which support IEEE standard 754 include IEEE basic single format operands and results, implementation of all four IEEE rounding modes, and exceptions processing in conformance with the standard. The exceptions processing for IEEE mode is fully described by the table in Figure 33. This table shows the flags and output data types that are generated as a function of the input operand data types. Seven status flags are provided (overflow, underflow, inexact, invalid operation, rounded up, not-a-number, and denormal operand). Support for IEEE gradual underflow (denormals) is provided when the multiplier is in "wrapped underflow" mode via a "wrapped underflow" datatype. A "Fast" mode where denormal results are set to zero is also provided for signal processing applications. The architecture employs separate multiplier, multiplicand, instruction, and mode input ports, each with an asynchronous enable for maximum flexibility. Three state output ports are provided for the product and flag registers.

A major challenge in the layout of this circuit was the development of a robust power distribution scheme. The power supply routing must be unobtrusive enough, so that its capacitance contribution is minimal, but large enough to adhere to the electromigration rules and to minimize ohmic drop to the center of the chip. Two large horizontal TOPMET V_{DD} and V_{SS} busses are at the top and bottom of the chip to reduce ohmic losses and distribute power from the pads easily. Thirty-two columns of 50μm V_{SS} and 20μm V_{DD} run vertically to supply the individual cells of the chip. V_{SS} is much wider than V_{DD} because the logic family can withstand a larger ohmic drop from the V_{DD} line than the V_{SS} line. The V_{DD} line is electromigration limited and the V_{SS} line is ohmic drop limited.

An electromigration and ohmic loss analysis was performed on the worst case column in the chip. The results show worst case losses of 36 mV on the ground buss and 90 mV on the V_{DD} buss. The ohmic loss analysis assumed an isolated worst case column with a worst case current flow and 0.04 ohms/square for TOPMET.. A sub-power network of six micron BOTMET lines is not included in the analysis, so the resultant losses are expected to be slightly better than predicted.

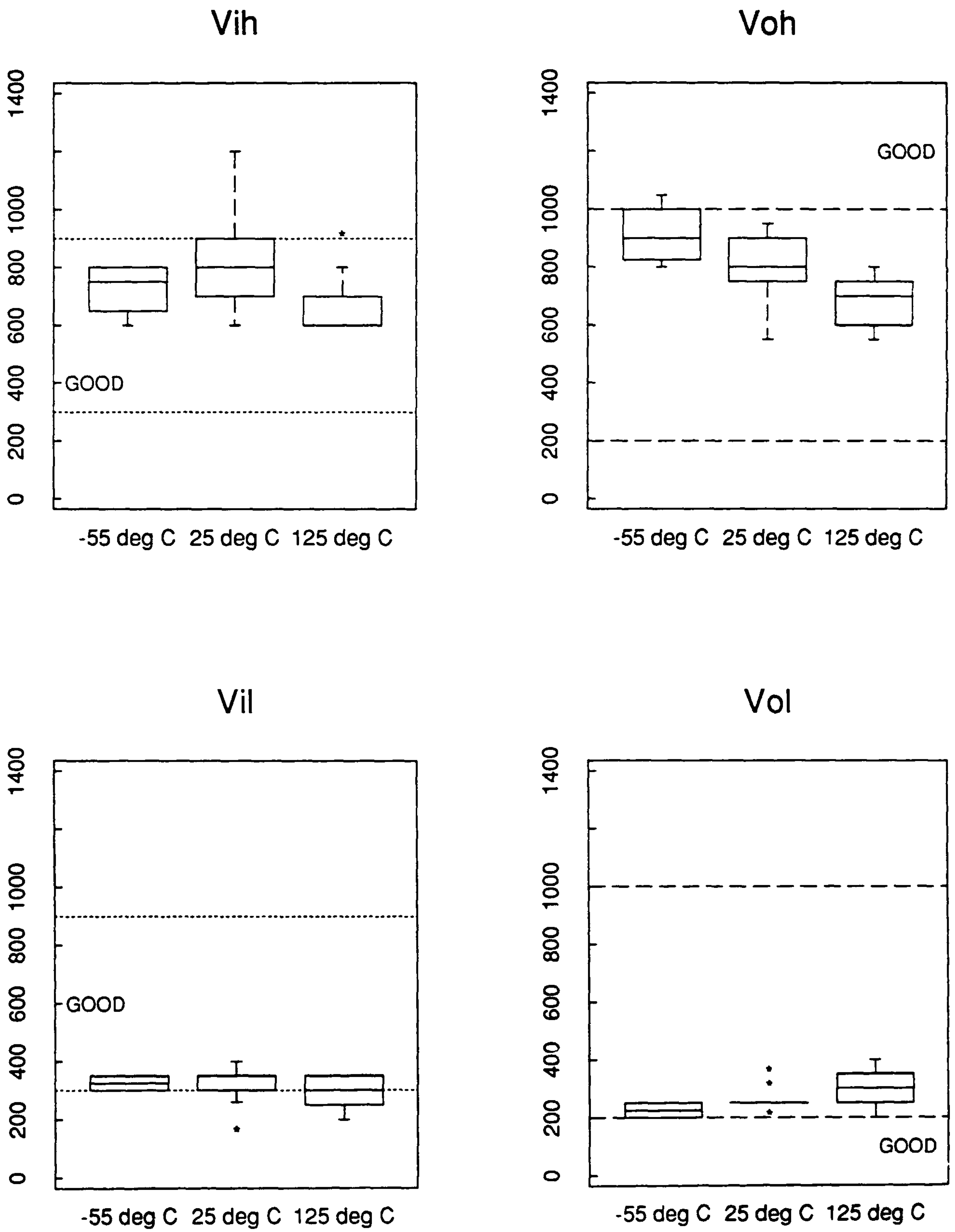

Figure 31 - Packaged Device I/O Levels for Custom ALU

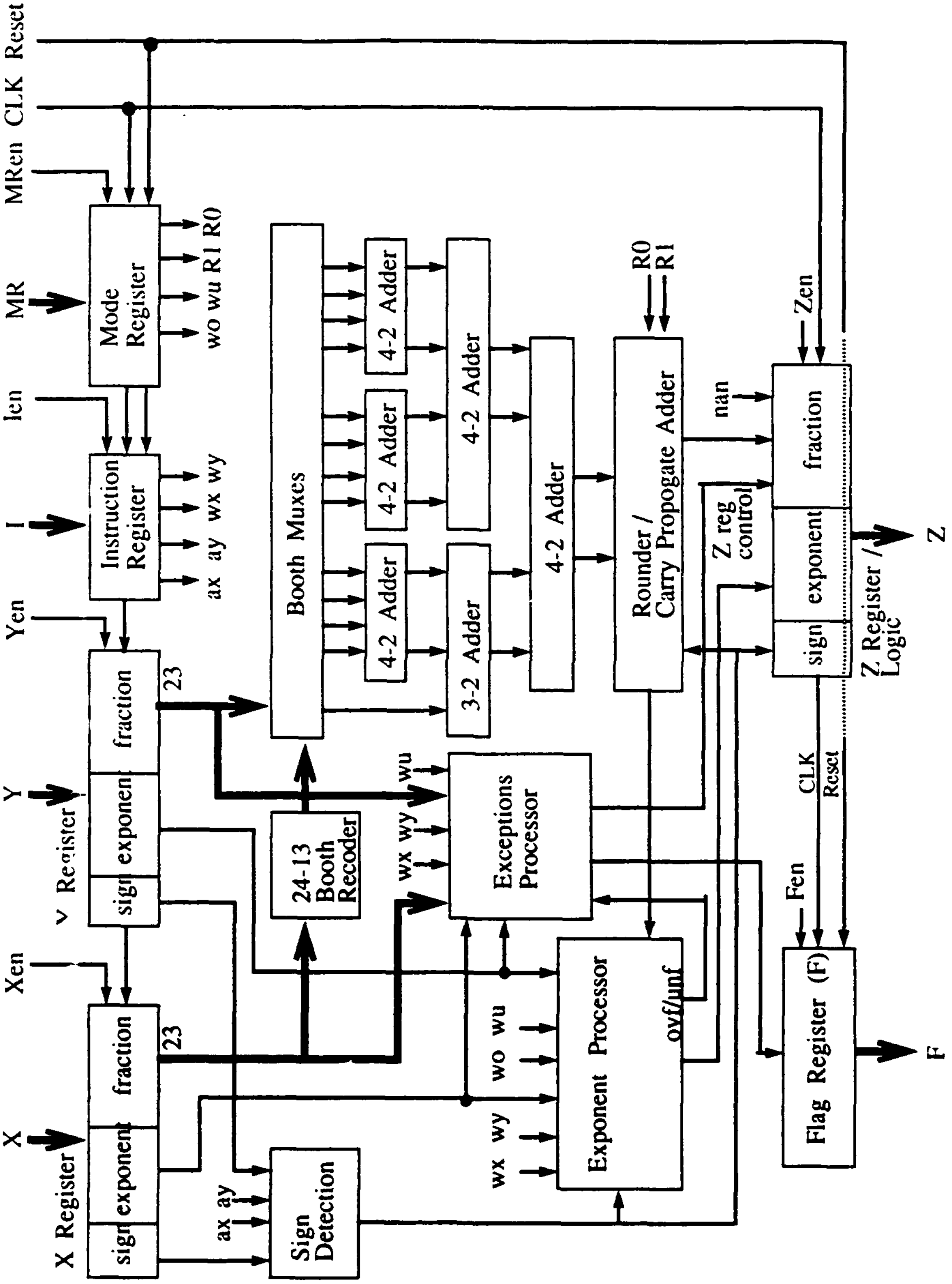
Reset
CLK
MRen
MR
Mode Register
wo wu R1 R0
Ien
I
Instruction Register
ax ay wx wy
Yen
Y
Y Register
sign
exponent
fraction
23
Xen
X
X Register
sign
exponent
fraction
23
Booth Muxes
24-13 Booth Recoder
4-2 Adder
4-2 Adder
4-2 Adder
4-2 Adder
4-2 Adder
3-2 Adder
4-2 Adder
R0
R1
Rounder / Carry Propogate Adder
Zen
nan
Z reg control
fraction
exponent
sign
Z Register / Logic
Z
wu
wx wy
Exceptions Processor
wo wu
wx wy
Exponent Processor
ovf/unf
ax ay
Sign Detection
CLK
Reset
Fen
Flag Register (F)
F

Figure 32- 32-Bit Floating Point Multiplier Block Diagram

X Operand

Y Operand

	ZERO	DNRM	WRAP	NRM	NaN_S	NaN_Q	INF
ZERO	none/0	DEN/0	none/0	none/0	INV,NaN/ NaN-Q	NaN/NaN-Q	INV,NaN/ NaN-Q
DNRM	DEN/0	INX,DEN/0	INX,DEN/0	INX,DEN/0	INV,NaN/ NaN-Q	NaN/NaN-Q	DEN/INF
WRAP	none/0	INX,DEN/0	INX,none/0	none/NRM, UNF/WRAP, none,UNF/0	INV,NaN/ NaN-Q	NaN/NaN-Q	none/INF
NRM	none/0	INX,DEN/0	none/NRM UNF/WRAP none,UNF/0	OVF/{WRAP, INF, NRM.MAX}, none/ NRM, UNF/WRAP	INV,NaN/ NaN-Q	NaN/NaN-Q	none/INF
NaN_S	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q	INV,NaN/ NaN-Q
NaN_Q	NaN/NaN-Q	NaN/NaN-Q	NaN/NaN-Q	NaN/NaN-Q	INV,NaN/ NaN-Q	NaN/NaN-Q	NaN/NaN-Q
INF	INV,NaN/ NaN-Q	DEN/INF	none/INF	none/INF	INV,NaN/ NaN-Q	NaN/NaN-Q	none/INF

The possible data types are zero (0), denormal (DNRM), wrapped underflow (WRAP), normalized (NRM), signalling not-a-number (NaN_S), quiet not-a-number (NaN_Q), and infinity (INF). The output flags are listed first, then a "/" (slash), and then the possible data types are listed - curly braces enclose the data field when more than one data type is possible. In some case multiple flag and data type combinations are possible. When no flags are generated the word "none" appears in the flag field.

Figure 33 - Table for Exceptions for IEEE Compatible Mode (WU bit set)

A first order simulation of the power dissipation showed a worst case power dissipation of 8 watts with the I/O drawing about 3 watts. The critical path consists of 78 separate gates and occurs under only a few special conditions. The worst case delay occurs when the exponent overflows due to the incrementer rounding into the 47th bit, changing it from a zero to a one. The critical path of the multiplier was extracted with capacitance from the layout and simulated over all model files. Because of the number of transistors and capacitors in the fully extracted critical path, the ADVICE file was too large for ADVICE to handler (over 7000 transistors). We broke the simulation into three smaller parts. The results of the simulation predict a worst case delay of about 13.5 nS, with a best or typical case being about 8.5 nS (109-173 ps/gate).

Output buffers were designed to satisfy the DARPA specifications over all simulation files. The primary design objectives were to provide solid logic low ($V_{ol} < 0.2V$) and logic high ($V_{oh} > 1.0V$) levels over temperature while keeping power consumption to a minimum. The simulations of Figure 34 show that for all combinations of high and low threshold voltages and for all combinations of frequency dependent output conductance, the logic lows are less than 0.2 volts. The worst case (#9) is low thresholds for both EFET and DFET at 125°C. The logic highs are all above 1.2 volts. The switch points range from 0.4V to 0.9V and are centered at about 0.65V. The final design has the following characteristics:

Inputs	80
Outputs	39
V_{DD}/GND pins	76
Logic Gates	~6500
Estimated Power Dissipation (worst case average dynamic power)	8.0W

We processed nine lots of 32-bit multipliers, five of which occurred after we changed to the "PP" etchant and re-established control of our EFETs (see Section 4.3). In our initial tests of devices manufactured before the new "PP" EFET tub etchant, we had difficulty achieving stable and repeatable results. The devices required initialization vectors: vectors had to be repeated several times before a successful strobe compare of the outputs with the expected results could be performed. Loosely functional devices manufactured after the "PP" EFET tub etchant process do not require any initializing vectors. We attribute this to the improved EFET scaling for small EFETs (3µm to 20µm wide) and subsequent improvement in SFFL logic gate noise margin performance brought about by the new EFET tub etch.

After achieving repeatable functional test performance at 24 nsec worst case multiply time on unit 38185-207, we improved the test fixtures by reducing resistance and inductance in the power and ground paths to the DUT board, and by installing chip capacitors and bypass capacitors on the DUT board. These changes improved the measured worst case performance from 24 nsec to 10.75 nsec in the HP82000 real time compare mode, and down to 10 nsec in the HP82000 data acquisition mode. Tester calibration ultimately brought real time compare performance at 25°C down to 10 nsec as well. This seemed to be the limit of our testing ability, not necessarily the limit of the 32-Bit Multiplier.

Table 20 shows the speed and power supply currents for three devices. Both speed and current are weak functions of temperature. In general, while devices performed well at 2.0V V_{DD}, we could not demonstrate consistent performance at 1.8V.

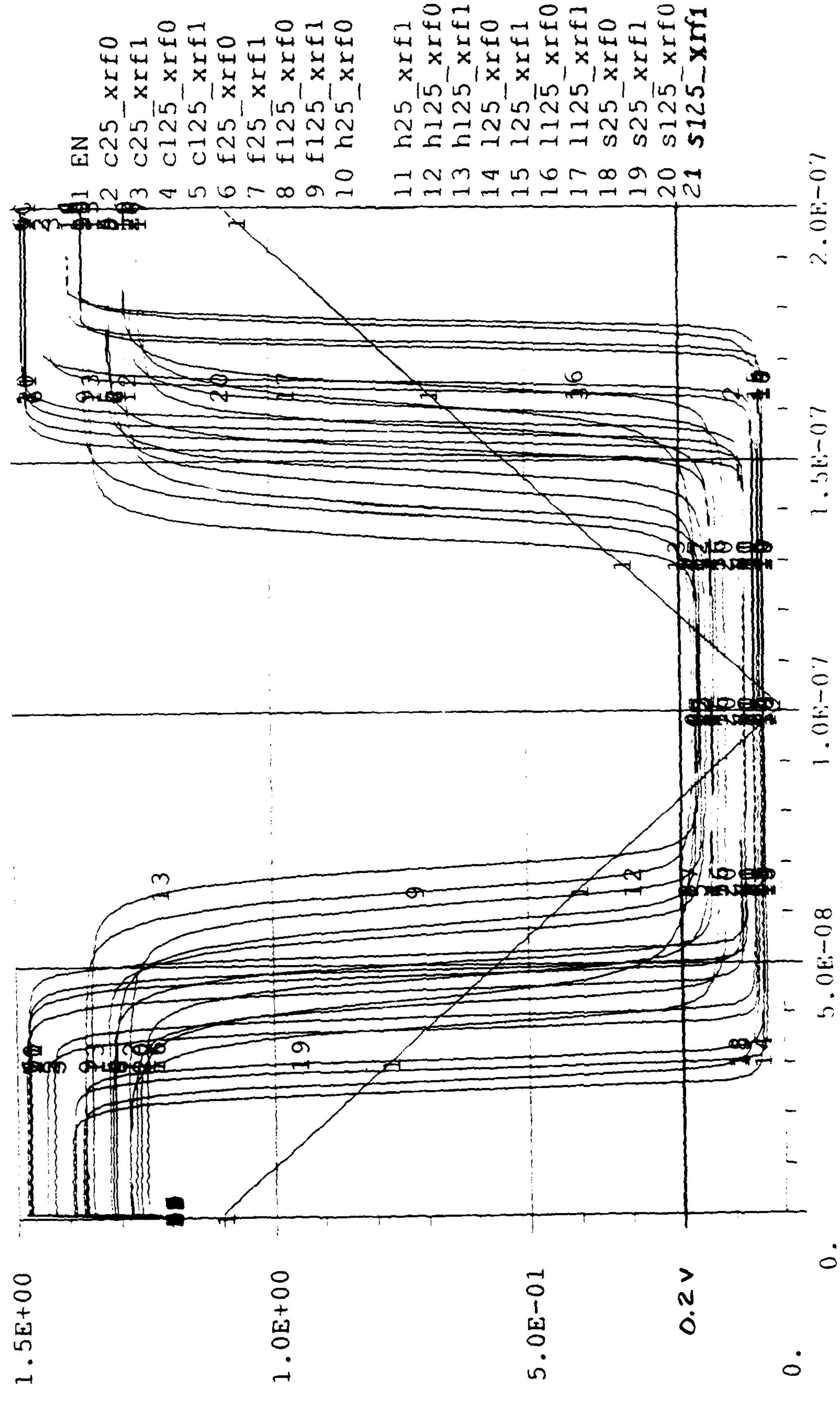

Figure 34 - Simulation of Output Buffer for 32-bit Floating Point Multiplier

Table 20 - Operating Multiply Times and I_{DD} Current

Wafer	Device	Temp (°C)	Minimum Clock Period at 2.0 volts (nanoseconds)	Dynamic I_{DD} at 2.0 volts (A)
38186	102	-55	10.75	3.4
38186	102	0	10.75	3.2
38186	102	25	10.25	3.1
38186	102	80	NA	3.2
38186	102	125	NA	3.2
38386	103	-55	10.75	3.4
38386	103	0	10.75	3.2
38386	103	25	10.25	3.3
38386	103	80	10.75	3.1
38386	103	125	NA	3.1
38185	201	-55	10.75	3.5
38185	201	0	10.75	3.4
38185	201	25	10.5	3.3
38185	201	80	10.75	3.2
38185	201	125	NA	3.3

The design frequency of operation was 75 MHz, or 1/75 MHz=13.3 nanoseconds. Most of the functional units seem to exceed this frequency of operation at any given set of operating conditions. In all cases, the circuits operated at less than the specified design of 4.0A. The per gate performance may be approximated as follows:

Average critical path gate delay = 10 nsec/70 gates
= 143 picoseconds/gate.

Total power consumption was 7 watts, of which 0.78 watts went to the output buffers. Since the circuit complexity in equivalent gates was approximately 6500 gates, the average power consumption per gate was (6.22 watts/6500 gates) 0.96 mW/gate. An estimate of the speed times power product is Speed • Power = 143 psec/gate • 0.96 mW = 140 fJ/gate.

The set of box plots in Figure 35 shows the I/O levels over operating conditions. V_{ih} appears to be consistent within our specifications, while V_{ol} consistently fails (except at low temperatures and power supply ranges).

Finally, the measured clock-to-output delay was 2.9 nanoseconds (one measurement was taken), which is less the specified value of 3.0 nanoseconds.

This multiplier was intended to demonstrate GaAs SARGIC-HFET capabilities in a computer application. Present silicon parts will operate around 100 MHz, the same as our GaAs multiplier, but they have 2 to 4 stages of pipeline. Consequently, the result of the multiplication is not available until 3 to 5 clock cycles after the input. This is satisfactory for a digital signal processing application where there is a steady stream of numbers to be multiplied, but it's not nearly as appealing in data processing applications with branched instructions where only a single multiplication may be desired. Then the GaAs multiplier, which operates at 100 MHz with no pipelined stages, is much more appealing than state-of-the-art silicon. Combined with a 200 MHz floating point ALU, it would be the basis of a floating point processor. In this program, we were able to demonstrate performance over the commercial temperature range (<80°C). With design refinements, the I/O voltages could be improved so that the multiplier would have full performance over the military temperature range of -55 to 125°C.

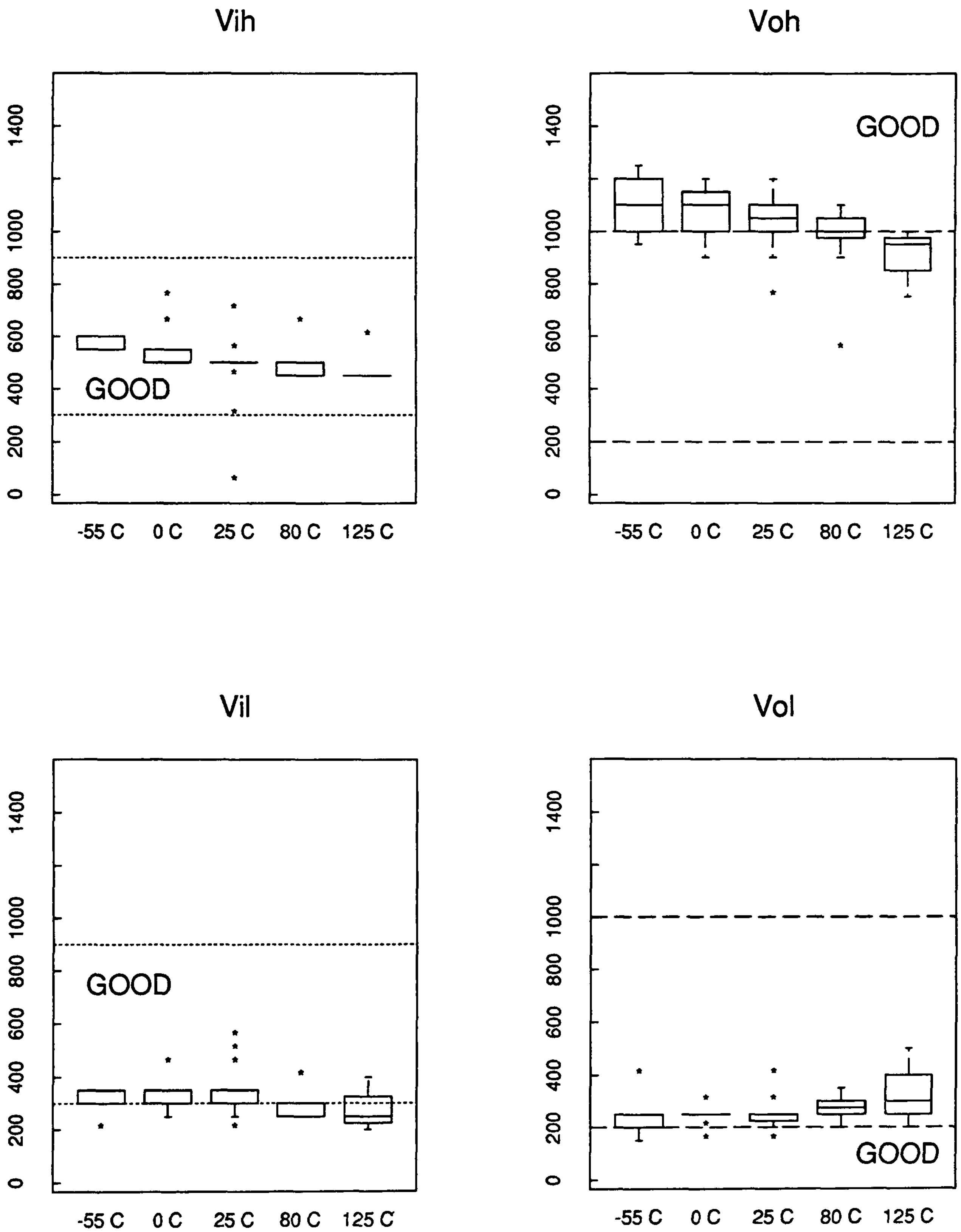

Figure 35 - Packaged Device I/O Levels for 32-Bit Multiplier

2.15 Standard Cell and Macrocell Libraries (A. I. Faris)

A standard cell library consisting of 37 cells was designed and laid out in the 2µm (lines and spaces) SARGIC-HFET process. The cells were incorporated into PT-1, and tests demonstrated full functionality on all cells. These cells were used in the Standard Cell Casino Test Chip.

The following is a list of the standard cell library. At present they comprise the DARPA Pilot Line III standard cell library.

1. INRB, Inverter*
2. NR2, 2 input NOR gate*
3. NR3, 3 input NOR gate*
4. NR4, 4 input NOR gate*
5. NR5, 5 input NOR gate*
6. ND2, 2 input NAND gate*
7. ND3, 3 input NAND gate
8. OAI22, 2/2 input OR/AND/INVERT gate*
9. OAI32, 3/2 input OR/AND/INVERT gate
10. OAI33, 3/3 input OR/AND/INVERT gate
11. OAI332, 3/3/2 input OR/AND/INVERT gate
12. XOR, 2 input Exclusive OR gate*
13. XNOR, 2 input Exclusive NOR gate
14. MUX21, 2 to 1 Multiplexer*
15. MUX41L, 4 to 1 Inverting Latched output Multiplexer
16. DECOD, 1 to 4 output Demultiplexer/Decode
17. SIGDRV, Non-Inverting Signal Driver
18. CKDRV, Non-Inverting Clock Driver
19. TBFIN, Non-Inverting Tri-state Buffer
20. FD1S2AX, Negative Edge Trig. D Flip Flop*
21. FD1S2DX, Negative Edge Trig. D Flip Flop with positive clear*
22. FD1S2NX, New Edge Trig. D Flip Flop with pos. clear and preset
23. FD1S2CX, Neg. Edge Trig. Master/Slave D Flip Flop with pos. clear and preset
24. FD1S5F, Neg. Level Trig. D Flip Flop with pos. clear and preset
25. BIN01, Non-Inverting Input Buffer
26. B075, Non-Inverting 75 OHM Output Buffer

*These cells are available in both buffered and unbuffered versions.

Then for the Transversal Filter Chip, a standard macrocell library consisting of 47 cells was designed and laid out in the 2µm (line and space) SARGIC-HFET process. The macrocell library is an enhancement of the original standard cell library. Many commonly used functions are laid out as a single macrocell. Compared to an implementation using the original standard cells, a macrocell implementation results in lower power consumption, smaller chip size, and faster chip speed. The macrocells all have the same height, thereby avoiding the layout problems that occur when cells have different heights.

The macrocell library was completely simulated using ADVICE and the SargicS.11 model parameters. The simulations were done at 25 and 125°C, using nominal, fast, and slow models. Also, a design manual was prepared and sent to Hughes to reside in HCAD. Presently all the cells have been rechecked for design rule violations and sent to Hughes. A list of these macrocells appears in Table 21.

Table 21 - Summary of HCAD Macrofunction Library

Cell Name	Cell Function
aoi333	and-or-invert
barsrb4	barrel shifter
bclab4	adder
bii01rlp	inverting input buffer
bii01tbp	inverting input buffer
bin01rlp	non-inv. input buffer
bin01tbp	non-inv. input buffer
bme	multiplier/encoder
bmfab4	booth multiplier
bmhab4	booth multiplier
bmmuxb4	booth multiplier
bo50rlp	non-inv. output buffer
bo50tbp	non-inv. output buffer
ckdrv_m	clock driver
clab4	adder
clcb4	carry lookahead
ctrdb4	down counter
ctrdpb4	down counter
ctrub4	up counter
ctrudb4	up/down counter
ctrudpb4	up/down counter
ctrupb4	up counter
daoi22	dual and-or-invert
daoi32	dual and-or-invert
daoi33	dual and-or-invert
decb4	decoder
dinrb	dual inverter
dmux	dual 2-1 multiplexor
dnr2	dual nor
dnr3	dual nor
dnr4	dual nor
dnr5	dual nor
dxnor	dual exclusive nor
dxor	dual exclusive nor
fadd	adder
fd1s2ax_m	flip-flop
fd1s2dx_m	flip-flop
fd1s2nx_m	flip-flop
fd15f_m	flip-flop
hadd	adder
regfb44	register file
sigdrv_m	driver
srmxpib4	shift register
srpipob4	shift register
srpisob4	shift register
srsipob4	shift register
tbfin_m	tri-state buffer

2.16 Standard Cell Casino Test Chip Design and Test Results (A. Lee, S. W. White, E. K. Gee and W. T. Kuo)

The Standard Cell Casino Test Chip (SC-CTC)[4] is a 3500-gate circuit designed by Hughes. The design is based on a scaled version of the Rockwell CTC in that the Memory Tester Macrocell was eliminated in order to meet the required gate count. The chip design was implemented in a standard cell layout style using CAD tools from Mentor and Cadence, and was completed in April, 1988.

The SC-CTC contains a number of functional units geared toward process/yield analysis. Included are a 16-bit Dual Datapath Macrocell containing counters, registers, and comparators for error detection. The design also includes a 15-stage Ring Oscillator with a divide-by-16 counter to provide for accurate gate delay measurement, an 8-bit 8x8 MUX/DEMUX (Switch Matrix), a Programmable Multiplexer Macrocell capable of performing a number of complex multiplexing operations, and a Straight-in/Straight-Out test circuit. Boundary scan circuitry is also included for testability. The design followed from the subcircuits that were successfully demonstrated in PT-1.

The following statistics summarize the major properties of the SC-CTC design.

Number of Input Pins:	98
Number of Output Pins:	74
Number of Power/Ground Pins:	69
Number of Logic Gates	3500
Number of Transistors:	24,266
Average Dynamic Power:	5.1 Watts

One of the high risk technical issues related to testing was the manufacturability of a 241-pin probe card for the SC-CTC. Micro-Probe, Inc. of San Diego was not only able to deliver the probe card on time but with excellent quality. Probe placement was very accurate despite the high pin count and tight pad spacing of the SC-CTC (241 pins, 4 mil pads on 5 mil centers). Test software development and final fixture debugging were completed after receiving the SC-CTC probe card and the first lot of wafers.

Four wafers from the first lot of SC-CTCs (Lot 308xx) were parametrically tested by AT&T and then delivered to Hughes for functional testing at the end of August 1988. Initial data from the Process Control Monitors (PCMs) showed relatively higher threshold voltages and lower transconductance than design targets. Test data demonstrated some working subcircuits, and average power consumption was measured to be 5.1 Watts.

Various sections of the SC-CTC were tested individually for functionality. The Ring Oscillator was measured with a high bandwidth oscilloscope to observe its waveform. Internal gate delays, as measured by oscillation frequency, varied between 125 and 234 pS. Yield on the Ring Oscillator structure was 36%, and rise and fall times were measured to be about 700 pS at the probe card level.

A second subcircuit called the Straight-In/Straight-Out buffer was also tested. This structure consists of two input receivers that fan out into six output drivers. Oscillations were seen when this section was tested.

Many experiments were performed to locate the source of the oscillations. Various loads were used on the outputs of the CTC as well as extra decoupling capacitors for the power supplies to reduce the amplitude of oscillation. There were two conditions that helped reduce the amplitude of oscillation:

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[4] The Government's Casino program was originally intended to provide a GaAs demonstration system for the Advanced On-Board Signal Processor (AOSP). The CTC was designed to test various AOSP concepts, especially chip-to-chip communication.

1. When some of the output pins were open circuited. (The more pins that were open circuited, the smaller the amplitude of oscillation.)
2. When current loads were connected at the outputs. (The smaller the current loads, the smaller the amplitude of oscillation.)

There was some evidence that the oscillations were caused by high transient load currents and the fact that the input receivers and the output drivers shared a common V_{DD} power bus at the chip level. Noise could be coupled back to the input receivers via the V_{DD} bus due to the fast edge rates of the GaAs circuit outputs. To confirm this, a YAG laser was used to separate the V_{DD} power bus between the input receivers and output drivers on the wafer. The oscillations were either smaller in amplitude or no longer present after separating the power bus. The undesirable oscillations were not detected during testing of the internal Ring Oscillator because all but one of the SC-CTC's outputs were open circuited at the time.

Another problem encountered in this initial lot was that the output logic levels of the SC-CTC chips had a spectrum of values between a logic LOW and a logic HIGH. Series resistors of 25 ohms were used in the probe card to properly load the SC-CTC's output drivers (25 ohms from resistors + 50 ohms from tester = 75 ohm load).

Between October 1988 and March 1989, Hughes completed extensive functional testing of 16 wafers from three more lots (317xx, 318xx, 322xx) containing a new MBE structure, ED7 (see Section 4.2). Though no fully functional SC-CTCs were found, all SC-CTC subcircuit designs were proven through analysis of data taken from these lots. Wafers processed with the new MBE structure demonstrated dramatically improved circuit operation and yield. Test results were provided to design and process engineers for further analysis and process enhancement.

The output logic levels from these lots were clearly discernible as either a HIGH or a LOW, unlike the devices from Lot 308xx. In addition, no parasitic oscillations of any frequency or magnitude were observable in these lots. There was also a strong correlation between the PCM data which showed correct threshold voltages and wafers with functional or partially functional subcircuits.

One problem that was encountered during test was that the error count was not repeatable. This came to be known as the "preconditioning" problem. When the test equipment ran the test vector file through the SC-CTC, the tester held the circuit's input state given by the last test vector in the file. The test vector in this case kept most of the internal logic of the SC-CTC in the ON state. This allowed the chip to warm up, changing the error count every time functional testing was repeated. To alleviate this problem, a new test vector was appended to the vector file that shut down most of the internal logic in the SC-CTC. This technique gave more repeatable test results.

Lot 317xx consisted of four wafers. There were some functional or partially functional subcircuits within the SC-CTC. This was a drastic improvement over the previous lot. One wafer contained two SC-CTCs with fully functional Boundary Scan subcircuits. The Boundary Scan subcircuit includes a 92-bit shift register containing approximately 1400 gates. In general, the less complex the subcircuit, the higher the yield.

Lot 318xx demonstrated the most encouraging testing results. Six SC-CTCs from this lot had many functional or partially functional subcircuits. One of the six devices had a total error count of only 3 of 1576 test vectors when three stuck output bits were masked out. The SC-CTCs from this lot were also tested at 40 MHz with similar functional yields.

While we never located a chip that was fully functional, all the subcircuits were functional on one chip or another. This led us to believe that we had correctly implemented the logic design and translated it to a correct mask layout. The lack of full functionality is not surprising since the standard cells used in this circuit were designed early in the program, before the FET characteristics had stablizied. By the time the wafers were fabricated, the FETs no longer matched the design model, and we found that the standard cells had low noise margins at high temperatures.

As mentioned earlier, much of the experience gained from testing the SC-CTC has been applied to other circuits including the TFC. Five of the major design issues identified during the SC-CTC testing are as follows:

1. Power supplies to the core and input receivers of a chip should be separated from the output driver power supply to prevent circuit oscillation.
2. Though the probe card manufacturer was able to build the tightly spaced SC-CTC card with excellent results, pad spacing should be relaxed.
3. Power/Ground pads should be placed frequently along output pads to prevent voltage sagging.
4. Larger Power/Ground pads should be used where supply currents are expected to be high. Multiple probes should be placed on these larger pads to minimize IR drops.
5. The output drivers should be designed to handle 50 ohm loads for testability utilizing current test equipment.

2.17 Standard Cell ALU Design and Test Results (W. A. Oswald, L. Ackner, C. H. Tzinis, and R. J. Niescier)

Using the experience gained constructing the PT-2L standard cell dual 8 x 8 multiplier, we started construction of the standard cell ALU as a means of testing the robust nature of the AT&T standard cell library and the associated tools. In logic as well as function, the standard cell ALU is the same as the earlier custom ALU. There are two design methods that could be used to accomplish the design task. We could construct the circuit using macro blocks (standard cells prewired creating higher functional blocks) or we can build the circuit using basic standard cells. The former would require LTX2 to place and route a few hundred cells, the latter a few thousand. By using the latter method we were able to test AT&T's cell library and LTX2's ability to place and route a large number of GaAs cells. Furthermore, to reduce design and test time as well as cost, the standard cell ALU uses the same I/O frame as the custom ALU eliminating the need for new probe cards.

The full chip (shown in Figure 36) contains 3571 gates and is 57 mm^2. There are three power planes, one for input, one for output, and one for internal circuitry. There are two ground planes, one for the I/O and one for the internal circuitry. The division of power and ground improves the noise immunity. Also, each row is divided in half by a center power bus which reduces electromigration.

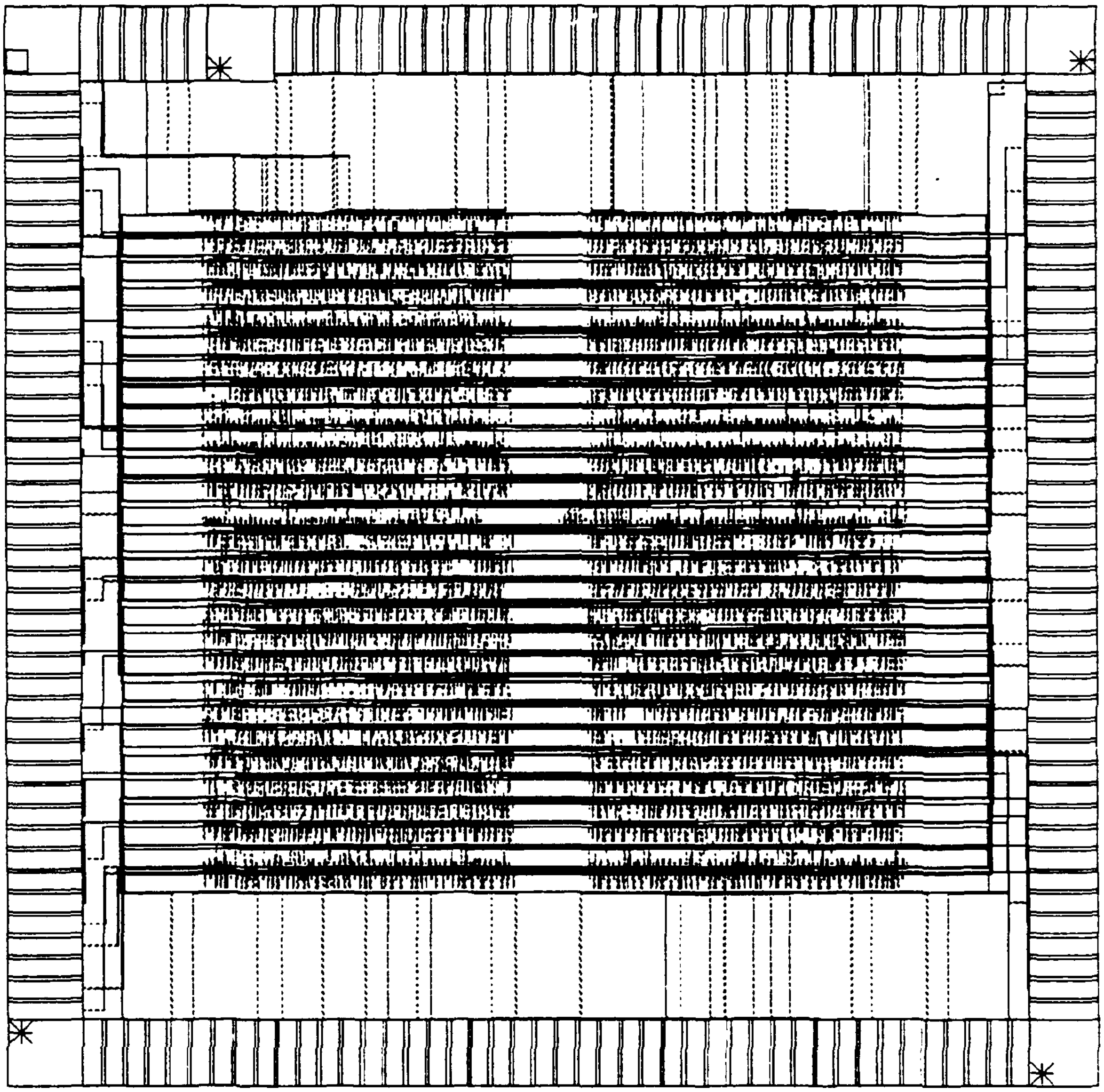


Figure 36 - Standard Cell ALU Chip Layout

Several conclusions can be drawn from the layout. First, the fact that the standard cell ALU fits in approximately the same area as the custom ALU is a tribute to the compact nature of the library. Second, the time frame for the design (from final logic to first place and route) was under 10 days excluding the learning phase of LTX2. Therefore, GaAs standard cell design is a viable method of layout when fast turnaround times are required. Third, our cell library contains enough gate families to build complex circuits. The main features of the standard cell ALU are:

Number of inputs:	79
Number of outputs:	35
Number of VDD/GND pins:	68
Number of Gates:	3571
Estimated Power Dissipation (all outputs open):	2.7 W

Six lots were fabricated, but only two produced functional circuits. Table 22 summarizes these data.

Table 22 - Standard Cell ALU Wafer Yield Summary

Lot Number	Functional Sites	Total Sites	Functional Yield	PCM Rating
33710	3	255	1%	27/101 = 27%
34060	5	306	2%	38/126 = 30%

Since the PCM ratings are relative high, the functional yield is disappointing. The devices from lot 33710 were marginal and operated in a very limited voltage area ($V_{DD} \cong 2.7V$); most of the devices of lot 34060 operated in nominal range. Three packages were tested and one of three devices satisfies all I/O requirements at room temperature and 100 MHz while another does so at -55°C and the same frequency.

It is instructive to compare the custom and standard cell design styles. Both designs used Enhancement Source Follow Logic (ESFL), a logic family using lower power than the standard SFFL. Both circuits used the same basic cells as building blocks for the ALUs. The main difference between the two is that for the custom design, the cells were hand-placed and routed to build the functional blocks. For the standard cell design, an automatic standard cell router placed the cells and routed the interconnects.

There were 96 wafers processed with the custom ALU, and 34 wafers processed with the standard cell ALU. As shown in Table 23, 32 custom ALU wafers had at least one fully functional device at 25°C; only 6 standard cell wafers had at least one functional die. Table 23 also shows the yield of functional die per wafer; only wafers with at least one functional die are included in this calculation. The yield difference between the two versions, although unexpected, can be attributed to processing, especially in the areas of interconnect. The main difference between the two designs is in the metal signal and power routing. The custom design has minimized its signal and power routes whereas the standard cell layout has similar power routes to the custom version, but a vastly different and much longer signal routing.

Table 23 - ALU Functional Yields

				Yield (%)	
	Wafers Processed	Wafers with at Least One Functional Die	Functional Die	Wafer	Die
Custom ALU	96	32	136	33.3	8.3
Standard Cell ALU	34	6	9	17.6	2.9

Because of the low number of functional standard cell ALUs, the comparison between the two versions will be made with the best working circuits from each. The selection of the best device was not done on the basis of I/O compliance, but rather overall device characteristics, including speed, power and operation over the temperature range. The simulation of the output buffer indicates that on average, both devices should have the same I/O characteristics.

Table 24 shows the differences in power, delay, and I/O characteristics between the custom and standard cell versions at 2.0 volts and 25°C.

Table 24 - ALU Performance

	Power (Watts)	Speed (MHz)	V_{IH} (Volts)	V_{OH} (Volts	V_{IL} (Volts)	V_{OL} (Volts)
Custom	2.26	167	0.70	0.85	0.35	0.25
Standard Cell	2.08	125	0.55	1.10	0.20	0.20
Specification	2.70	135	≤ 0.9	≥ 1.0	≥ 0.3	≤ 0.2

The performance (speed) advantage in the custom design is expected and can be attributed to the denser layout and to lower parasitic loading and fanout. The average power for the custom ALU is the same or slightly higher than the semi-custom ALU because all the gates are the same and the custom ALU can run at a faster clock speed.

We note that the standard cell ALU required much less design effort than the custom ALU. This is hard to quantify since 1) the standard cell design used cells created during the design of the custom ALU, and 2) the same team designed both circuits, so that the standard cell benefited from the prior custom design. Nevertheless, the custom design required 24 staff months, where the standard cell required only five. Given the similar performance of the two circuits and the robust shmoo plots seen for both circuits, the standard cell design style is very attractive.

2.18 Standard Cell Transversal Filter Design and Test Results (S. W. White, E. K. Gee, W. T. Kuo)

The Transversal Filter Circuit (TFC) contains 5200 gates on a die which is approximately 84 mm^2. It was the first circuit designed into DARPA Pilot Line III which exceeds the 5000 gate contractual requirement for complexity. The chip was designed solely using the Cadence based HCAD system also developed on this program. The circuit employs a standard cell layout methodology using AT&T's macrocell library. Predicted operating speed of the TFC is 160 MHz. The design was completed and masks were ordered during August 1989.

The TFC's architecture was chosen to benefit the next generation BSTS digital filter module, although its generic nature enables use on other programs. It serves as a finite impulse response filter for signal to noise ratio enhancement. The circuit includes 16 programmable 8-bit filter coefficients (taps) which reside in an on-chip register file. A pipelined multiply/accumulate processor forms the 24-bit filtered output data by operating on these coefficients and an infrared detector array sourced 16-bit input data stream. Because multi-pixel arrays (up to 4096 pixels) are accommodated, pixel data is stored temporarily in external memory when it is not indexed. As such, a complete memory interface was designed into the circuit which assumes that pipelined GaAs SRAMs are to be utilized. This interface is compatible with the 4K SRAMs under development at AT&T for this program. Finally, a 17-stage ring oscillator circuit is included on the design to provide for accurate gate delay measurement and characterization.

The following are key statistics of the TFC:

Number of input pins:	43
Number of output pins:	62
Number of power/ground pins:	68
Number of gates:	5200
Number of transistors:	41,546
Average dynamic power:	5.1 Watts

Six lots of Transversal Filter wafers were processed, and three passed PCM screening. Table 30 shows some of the key characteristics associated with the test wafers. During this time period, the MBE structure changed from ED10 to ED11 so that the FET characteristics would more closely match the design models (see Section 4.2). Also, three wafers were purchased from Picogiga. These wafers were supposed to match the ED11 layer structure, but they actually produced lower EFET and DFET currents than ED11.

Three functionality metrics are provided in the table. The first is the number of fully functional devices found at some supply voltage at 1 MHz. The next column labelled "Mean # Working Vectors" is the average number of test vectors passed by a die on the given wafer at V_{DD}=2.0 V. (There are a total of 3326 test vectors.) The column labelled "Mean # Working Bits" refers to the average number of output bits passing all test vectors for a die on the given wafer at V_{DD} = 2.0 V. (There are a total of 61 output bits.) Finally, the average drain current (I_{DD}) measured at the supply voltage of 2.0 V for each device on a given wafer is provided. These data are not available for lot 3388x as this test had not yet been implemented into the test program at the time those wafers were tested.

Table 30 - Wafer Characteristics (All Lots)

Wafer	MBE Structure	Functional Devices	Mean # Working Vectors	Mean # Working Bits	Mean I_{DD} (A)
33881	ED10	0	7	3	–
33882	ED10	1	156	11	-
33883	ED10	0	5	1	-
33884	ED10	1	203	14	-
33885	ED10	0	115	17	-
33886	ED10	0	18	3	–
34141	ED10	1	250	11	3.19
34143	ED10	0	99	13	2.76
34144	ED10	0	459	5	2.53
34145	ED10	0	306	6	2.42
34146	ED10	0	52	9	3.80
34801	ED11	0	39	9	3.99
34802	ED11	0	43	4	4.19
34803	ED11	0	0	0	4.36
34804	Picogiga	6	833	29	2.62
34805	Picogiga	1	250	32	2.70
34806	Picogiga	2	543	17	3.58

These functionality metrics can be examined from two different viewpoints. First, the best wafers are those with over 100 mean working vectors and/or over 10 mean working bits. All the functional devices came from wafers in this category. Empirically, we find that the PCM data for these wafers gives I_{dss} (EFET, V_{gs} = 0.5V) between 30 and 66 mA/mm and I_{dss} (DFET, V_{gs} = 0V) between 54 and 81 mA/mm. This is lower than the DFET current obtained from ED11. In other words, because the TFC was designed with the SargicS.11 models, it is not expected to work well with ED11 MBE material, which gives currents that are too high in comparison with SargicS.11. This is consistent with the results we obtained with the two ALUs.

The second viewpoint is that there are significant testing problems with circuits that draw high currents. Due to resistive losses, there is difficulty supplying adequate voltages to the circuits and their interiors when currents are high. This means that high current devices like those on the ED11 wafers are hard to test and may test as failures simply because insufficient current could be supplied.

Table 31 below provides characterization data for the best parts found in lot 34800. This includes all devices with fewer than 5 bad bits when tested at 1 MHz. Devices are identified as (X, Y, Z) where X represents the last digit in the wafer number, Y represents the row, and Z represents the column. Fully functional devices at 1 MHz and 40 MHz are indicated by a check mark, while partially functional devices are listed by the number of failing bits. The minimum supply voltage (V_{DD}) at which each part operates is listed. In all cases but one (see *), these devices operated from this minimum V_{DD} value up to at least 2.2V (the upper end of the specification value). All I/O voltage levels are listed (V_{OL}, V_{OH}, V_{IL}, and V_{IH}) as well as the total drain current with outputs terminated to 50 Ω. Finally, the derived gate delay for each stage of the on-chip ring oscillator circuit is given. These values can be compared to the specification and simulation values shown at the bottom of the table.

Table 31 - Best Die Characteristics (Lot 3480x)

Device	Fully Func. @ 1 MHz	Fully Func. @ 40 MHz	Min. V_{DD} (V)	Max. V_{OL} (V)	Min. V_{OH} (V)	Max. V_{IL} (V)	Min. V_{IH} (V)	I_{DD} (A)	Ring Osc. Gate Delay (ps)
(4,5,3)	√	√	1.70	0.024	1.357	0.501	0.844	2.94	220
(4,5,4)	√	√	1.65	0.029	1.355	0.498	0.842	2.98	216
(6,4,1)	√	√	1.60	0.080	1.396	0.459	0.820	3.34	211
(4,3,4)	√	√	1.80 *	0.026	1.375	0.527	0.826	3.00	220
(4,4,3)	√	√	1.95	0.034	1.355	0.550	0.892	2.98	239
(6,2,1)	√	√	1.80	0.057	1.278	0.632	1.050	3.15	220
(5,4,1)	√	1 bit	2.25	0.016	1.339	0.545	1.118	2.82	257
(4,2,4)	√	>10 bits	2.10	0.024	1.325	0.500	0.847	2.84	230
(4,3,3)	√	>10 bits	1.65	0.040	1.372	0.537	0.845	3.03	225
(5,6,1)	1 bit	1 bit	1.95	0.008	1.096	0.568	1.001	2.47	312
(6,5,1)	1 bit	1 bit	1.65	0.064	1.280	0.472	0.840	3.38	220
(5,2,2)	1 bit	>10 bits	1.85	0.016	1.333	0.564	0.878	2.91	239
(1,6,1)	2 bits	2 bits	2.25	0.177	1.221	0.406	1.033	3.30	248
(4,4,4)	3 bits	3 bits	1.70	0.033	1.375	0.456	0.862	3.00	stuck high
Specified			≤1.80	≤0.200	>1.000	>0.300	<0.900		
Simulated								3.19	189

It can be seen that the top three devices shown in Table 31 meet all specifications and are fully functional at 40 MHz. Overall, the devices shown above are significantly more robust than the best devices from the other two lots. Most of the devices shown above performed identically at 1 MHz and 40 MHz. This was not the case on the other two lots. Finally, these devices exhibit no pattern dependency. Unlike these later devices, all of the better circuits from the first two tested lots passed the test program only when the vector sets were arranged in a particular order (what we termed to be pattern dependency). This last improvement may be due to the reduce side-gating characteristics for this most recent lot. Ring oscillator gate delay averaged 235 ps. This is slightly faster than the previous two lots but still approximately 25% slower than predicted. Note that only one device from an ED11 wafer is listed in the above table as it was the only one with fewer than 5 bad bits.

Total yield over all three tested lots is 12/527 (2.3%). Yield on wafers 34804-34806 is significantly better at 9/93 (9.6%) while best wafer yield is 6/31 (19.4%). Note that for all of these yield figures, a part is considered to be good if it passes all test vectors at some V_{DD} value at 1 MHz. These latter yield figures are encouraging given that the original program goal was to achieve 10% yield on deliverable circuits of this complexity.

Shmoo plots display V_{IH} vs. V_{DD} operation were generated for a number of the best parts from lot 3480x. Figure 37 shows a plot for the device from wafer 34804, row 5, column 3.

2.19 1K Cell Array Design and Test Results (B. Randall, W. Satre, C. H. Tzinis, L. Ackner, J. Scorzelli, and R. J. Niescier)

Our initial cell arrays were the PT-2M 4-bit adder and the PT-2L quad 4-bit adder. Before designing the 5000 gate Cell Array Casino Test Chip, we decided to build a 1K cell array. This circuit is intended to fully exercise the CAD tools and the basic cells, which will also be used in the Cell Array Casino Test Chip.

The 1K cell array has 1024 basic cells, 80 I/O buffers, and 48 power pads. Each basic cell can be personalized into an inverter, 2-input NOR gate, 3-input NOR gate, or 4-input NOR gate. Each personalization also has a high-drive option for signals having high fan-out or routing capacitance. The SFFL logic family was selected because it was implemented successfully in PT-1. Provisions were made to the basic cell, the I/O buffer, routing channels, and reference coordinates so that they were compatible with the MagicCAD system at Mayo Foundation.

The logic design was supplied by Mayo Foundation. It consists of a dual data path with counters, registers, multiplexers, comparators, and a 6 x 6 multiplier. The total gate count is about 750, which corresponds to 73% utilization of the cell array. This design emphasizes testability, and many control signals are included so that each functional block can be tested. Also several of them can be connected together to determine the performance in a system environment.

The following design steps were performed to ensure a correct implementation of the circuit. Logic simulation, test vector generation, design data capture, place and route, layout verification, capacitive load extraction, post-layout timing verification, generation of a GDSII tape, and generation of a SPICE netlist were completed by Mayo with the MagiCAD system. Functional simulation of design, IR drop simulation, power bus noise simulation, merging of routing layers and floor plan, final DRC check, transistor netlist extraction, netlist comparison, and functional verification were performed by AT&T. The layout is shown in Figure 38. Some important data are listed below.

Inputs:	38
Outputs:	26
Additional Buffers:	16
Logic Gates:	738
Estimated Power:	2.3 W

We processed ten lots of 1K Cell Arrays, and four lots produced functional sites. In total, 296 functional sites were identified. Lots 33730 and 34030 were characterized in detail. Testing for functionality at the wafer level was done on the Advantest T3340, whereas the packaged circuits were tested from -55°C to 125°C up to 200 MHz on the HP 82000. The wafer test results for lot 33730 and 34030 are summarized in Table 27. As described above, the PCM rating reflects how many sites out of the total number tested (16 per wafer) simultaneously fulfills EFET and FET currents, and via resistance requirements.

WAFER 34804, ROW 5, COLUMN 3

```
2.000V     !. . . . . **.********************************************************
1.950V     !.         ***********************************************************
1.900V     !.        ************************************************************
1.850V     !.        ************************************************************
1.800V     !.         ***********************************************************
1.750V     +. . . . . ***********************************************************
1.700V     !.         ***********************************************************
1.650V     !.         ***********************************************************
1.600V     !.         ** ********************************************************
1.550V     !.         ** ********************************************************
1.500V    >+. . . . . ***********************************************************
1.450V     !.         ** ********************************************************
1.400V     !.         ** ********************************************************
1.350V     !.         ** ********************************************************
1.300V     !.         ***********************************************************
1.250V     +. . . . . ***********************************************************
1.200V     !.         .**********************************************************
1.150V     !.         ***********************************************************
1.100V     !.         ***********************************************************
1.050V     !.         ***********************************************************
1.000V     +. . . . . ***********************************************************
950.0MV    !.         ** *******************************************************
900.0MV    !.         *         .         .         .         .         .
850.0MV    !.         .         .         .         .         .         .
800.0MV    !.         .         .         .         .         .         .
750.0MV    +. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .
700.0MV    !.         .         .         .         .         .         .
 (Vih)      +---------+---------+---------+---------+---------+---------+--------
         1.500V    1.700V    1.900V    2.100V    2.300V    2.500V    2.700V
                                             (Vdd)
```

‘*’ = Pass, ‘ ’ = Fail

Figure 37 - Transversal Filter Chip Shmoo Plot for V_{DD} vs. V_{IH}

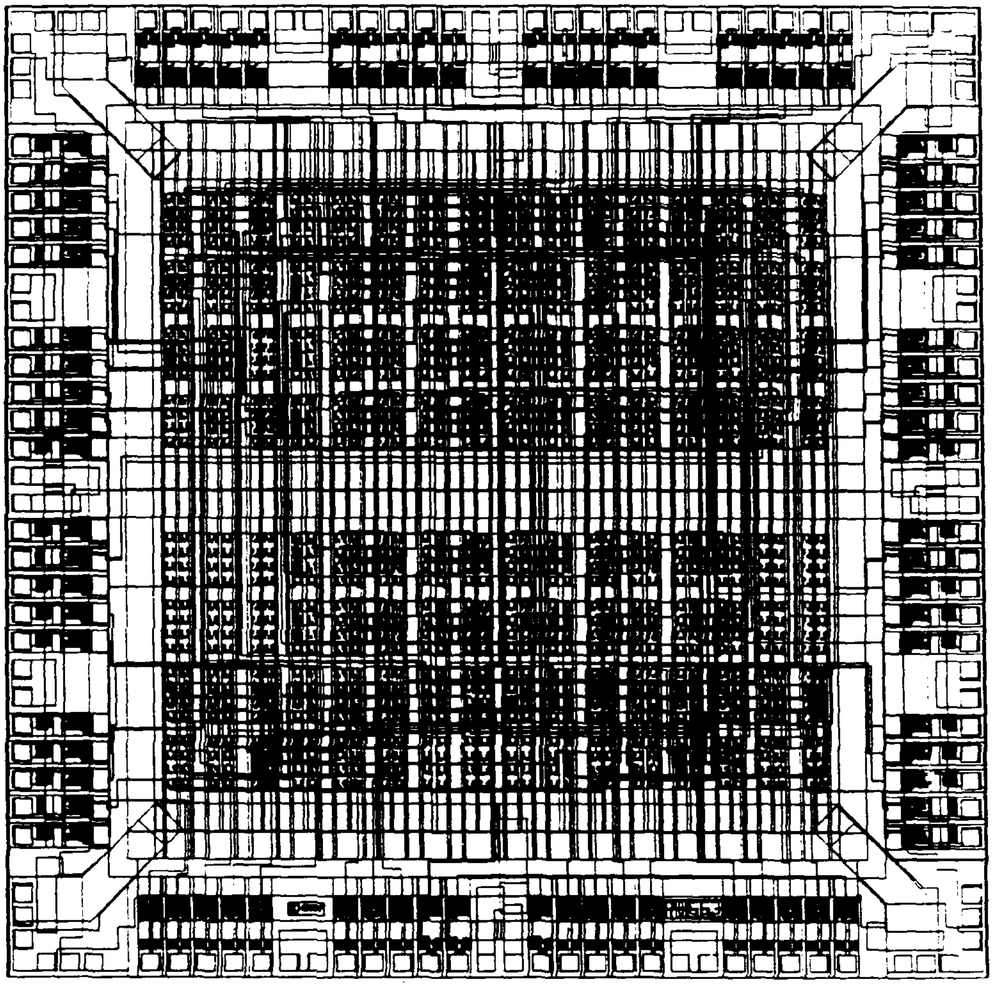


Figure 38 - Layout of 1K Cell Array Circuit

Table 27 - 1K Cell Array Wafer Yield Summary

Lot Number	Functional Sites	Total Sites	Functional Yield	PCM Rating
33730	135	498	27%	54/96 = 56%
34030	40	415	10%	3/80 = 4%

Not all functional sites satisfy the I/O requirements. The primary failure mechanism is high V_{IH}, which was expected, as the 1K Cell Array was designed with SargicS.11, a model that makes a 250 mV error in predicting the input switchpoint (see Section 3.3). However, data analysis revealed much higher V_{IH} than expected, prompting detailed investigation. We found holes in the shmoo plots which invalidated our search algorithm for testing. We used an improved search algorithm when we tested packaged devices. Figure 39 shows the I/O levels of 28 packaged devices in a boxplot format for -55, 25, and 125°C; each box contains the data for all three voltages -1.8, 2.0, and 2.2V. Next to the 25°C package data, the respective wafer probe data demonstrate the discrepancy in V_{IH}. The horizontal lines represent the specification levels, and it is apparent that the main failure mechanisms are V_{IL} and V_{OH} at 125°C and marginal V_{OL}. Simulations with SargicS.15 predict the collapse of VOL at 125°C, while the marginal V_{OL} is understood in terms of FET leakage around threshold voltage area (soft turn on). Figure 40 demonstrates the reduction of V_{OH} at 125°C as simulated by SargicS.15. The boxplots represent actual package data from Figure 39. Dotted lines show SargicS.15 models for this output buffer at 25°C (high, center, and low models: 25h, 25c, and 25l). Dashed lines show the three models at 125°C (125h, 125c, and 125l). The correlation with the measured results is apparent.

2.20 Cell Array Casino Test Chip Design and Test Results (S. W. White, L. R. Fisher, W. A. Oswald, J. Scorzelli, and C. H. Tzinis)

The Cell Array Casino Test Chip (CA-CTC) is the full-size cell array design for this program. The design of the CA-CTC was a joint effort involving design teams at both AT&T and Hughes. AT&T's responsibilities included designing the cell array floorplan and library, while Hughes used HCAD to personalize the Casino Test Chip function onto the array. Both teams performed independent logic and layout verification to ensure an error-free design. Good communication between the two design teams was accomplished through regular conference calls, face to face meetings, and electronic mail.

The CA-CTC is functionally equivalent to the Standard Cell Casino Test Chip previously developed by Hughes for the AT&T Pilot Line (Section 2.16). As such, it contains the same functional circuitry including a Datapath, Switch Matrix, Programmable Multiplexer, Boundary Scan Register, and Ring Oscillator. Mentor formatted logic schematics from the older standard cell design were used as a baseline for the cell array implementation. These schematics were updated to reflect the cells available in the newly developed cell array library. This library contains most of the cells in the standard cell library but their implementations differ somewhat; the E-family of SFFL is used and dual-gate FET structures have been eliminated from all cell types.

In order to make optimal use of HCAD's capabilities, the updated Mentor CA-CTC schematics were translated into Cadence format rather than simply translating the netlist. Additional HCAD cell representations were created for logic, circuit, and fault simulation as well as timing analysis, layout, and verification. With a complete cell array library hosted with HCAD, the design was verified using the SILOS logic and fault simulator. The standard cell CTC's simulation vectors were used following a translation into the HCAD compatible STL format. Because AT&T required a netlist representation to perform logic and layout verification, an LSL netlister was written and is now a permanent feature of HCAD. The CA-CTC design was subsequently run through this tool to create a netlist compatible with AT&T's computer-aided design environment.

Mentor's GateStation software, a key component of the HCAD system, was used to place and route the CA-CTC. Descriptions of the floorplan and cell layout personalizations were generated

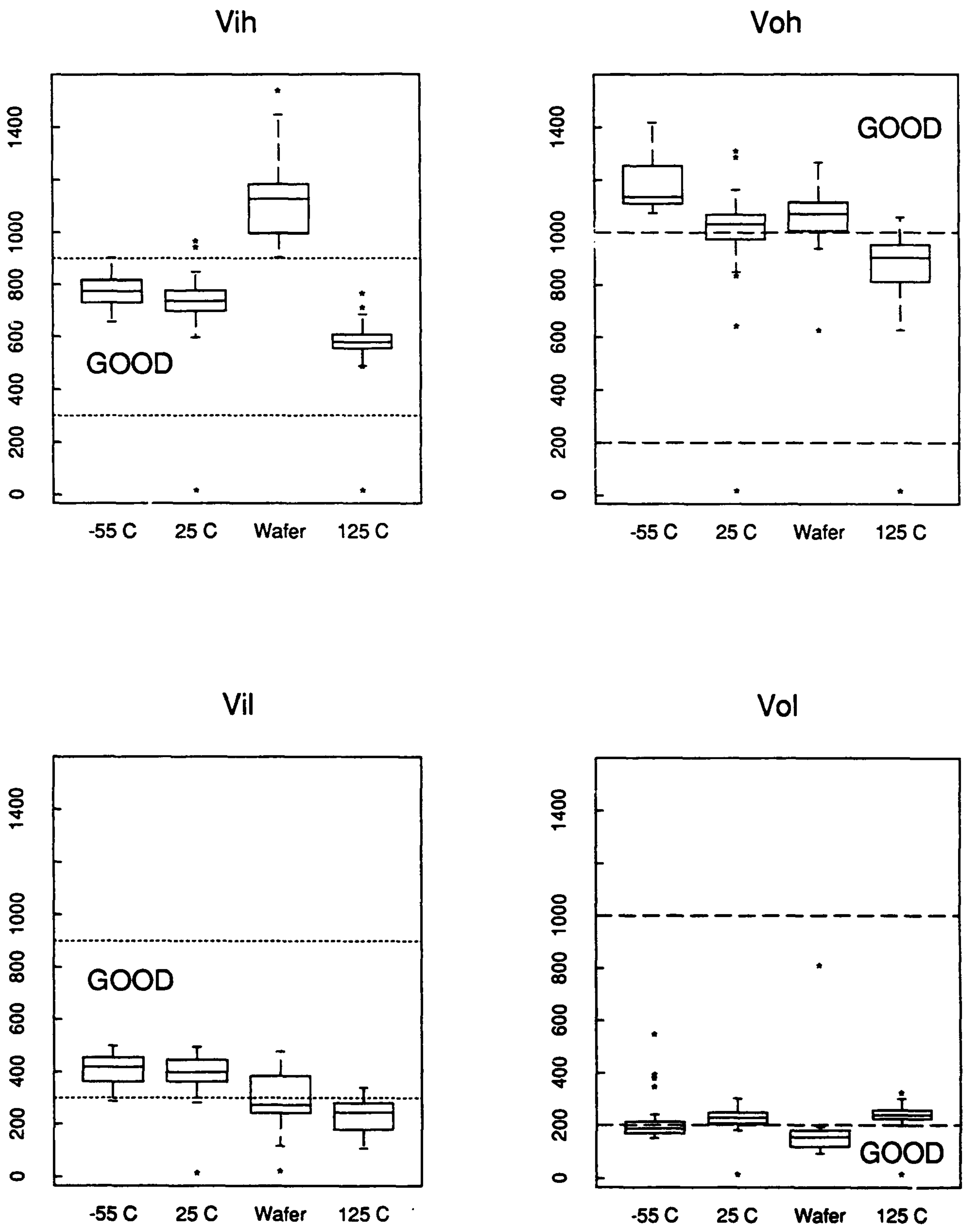


Figure 39 - Wafer and Packaged Device I/O Levels for 1K Cell Array

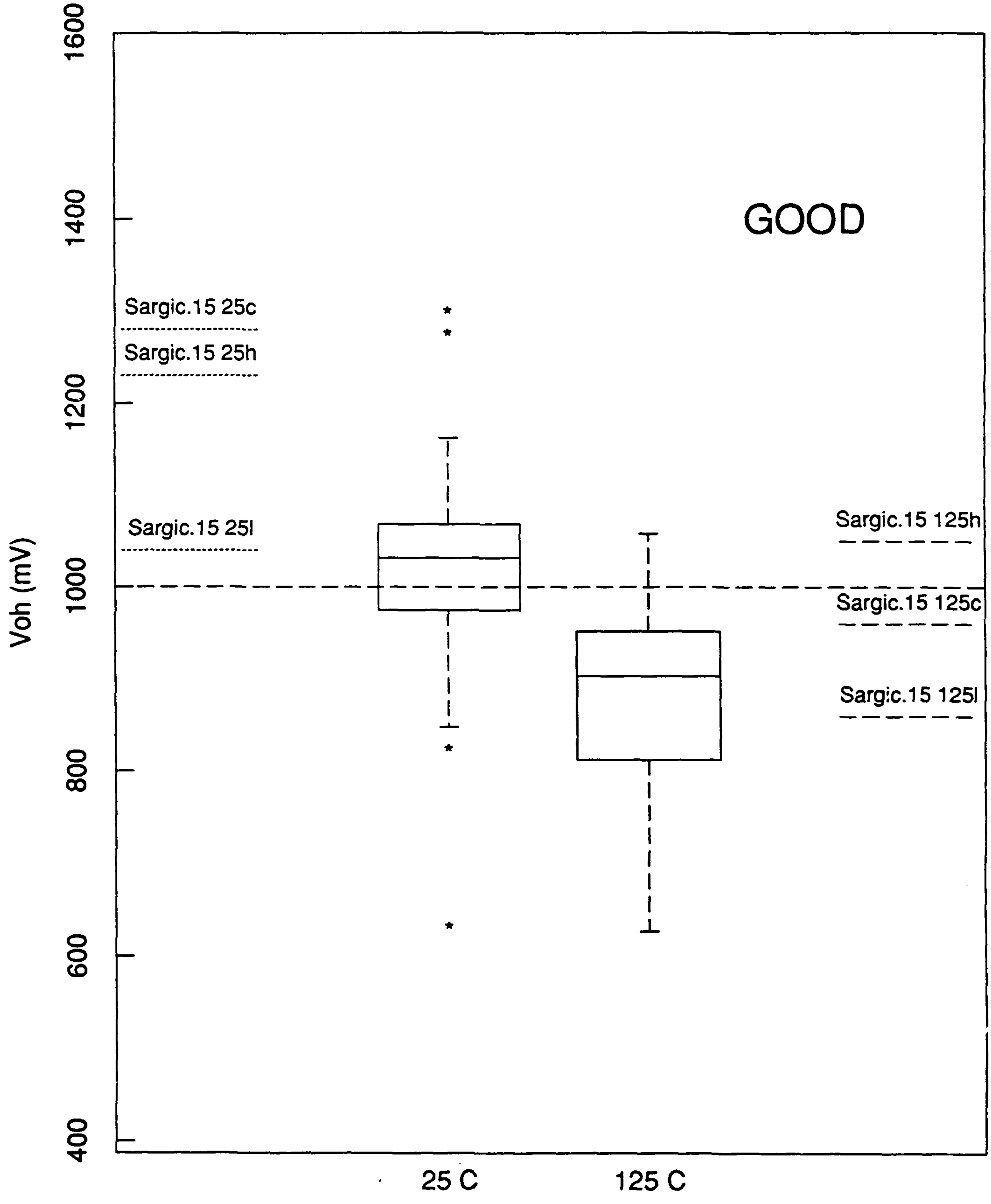


Figure 40 - Comparison of Simulated and Measured V_{OH} for 1K Cell Array

for GateStation in the form of text files. A number of test layouts were run but all resulted in many unrouted nets. After examination of these test cases, changes to the floorplan were recommended and later implemented at AT&T. GateStation is a row oriented, channel based router and thus works best with a floorplan of this style. The original floorplan was in a cell island style which explains why the router encountered such difficulty. The changes made to the floorplan reallocated the array's routing resource which greatly enhanced its compatibility with the router. Future routes on the enhanced floorplan were completed automatically with no unrouted nets.

Increased routing efficiency also was obtained by rotating the floorplan 90 degrees as represented within GateStation. This provided pin locations in the vertical plane that the router preferred. In the final GateStation session, the CA-CTC's I/O and Ring Oscillator cells were manually assigned to positions in the array by adding site locations in the schematics. All remaining cells were automatically placed and all nets automatically routed. Array utilization is quite high, exceeding 82%. The Hightower number is 55.

After HCAD successfully completed a fully auto-routed personalization, a timing analysis using the TA simulator was run to evaluate the effect of parasitics on the circuit's performance. TA identified the slowest paths within the design which prompted the addition of net weights into the schematic followed by a final iteration of the place and route process. Critical path nets were subsequently examined in the interactive routing environment and some were manually rerouted to minimize their lengths. Clock nets were given similar attention to eliminate the possibility of skew problems. By utilizing the net weights and HCAD's gate array interactive routing capability, the CA-CTC's critical path performance was improved by approximately 20%. The circuit's simulated performance is 199 MHz for a critical path that is 18 gates long. An ADVICE circuit simulation performed at AT&T predicted 204 MHz (272 ps/gate). Figure 41 is a diagram of the critical path.

Layout verification at Hughes consisted of design rule checking and two levels of layout vs. schematic checking (macrocell and device level). The final verified version of the CA-CTC layout was sent to AT&T for further independent verification using their own tools.

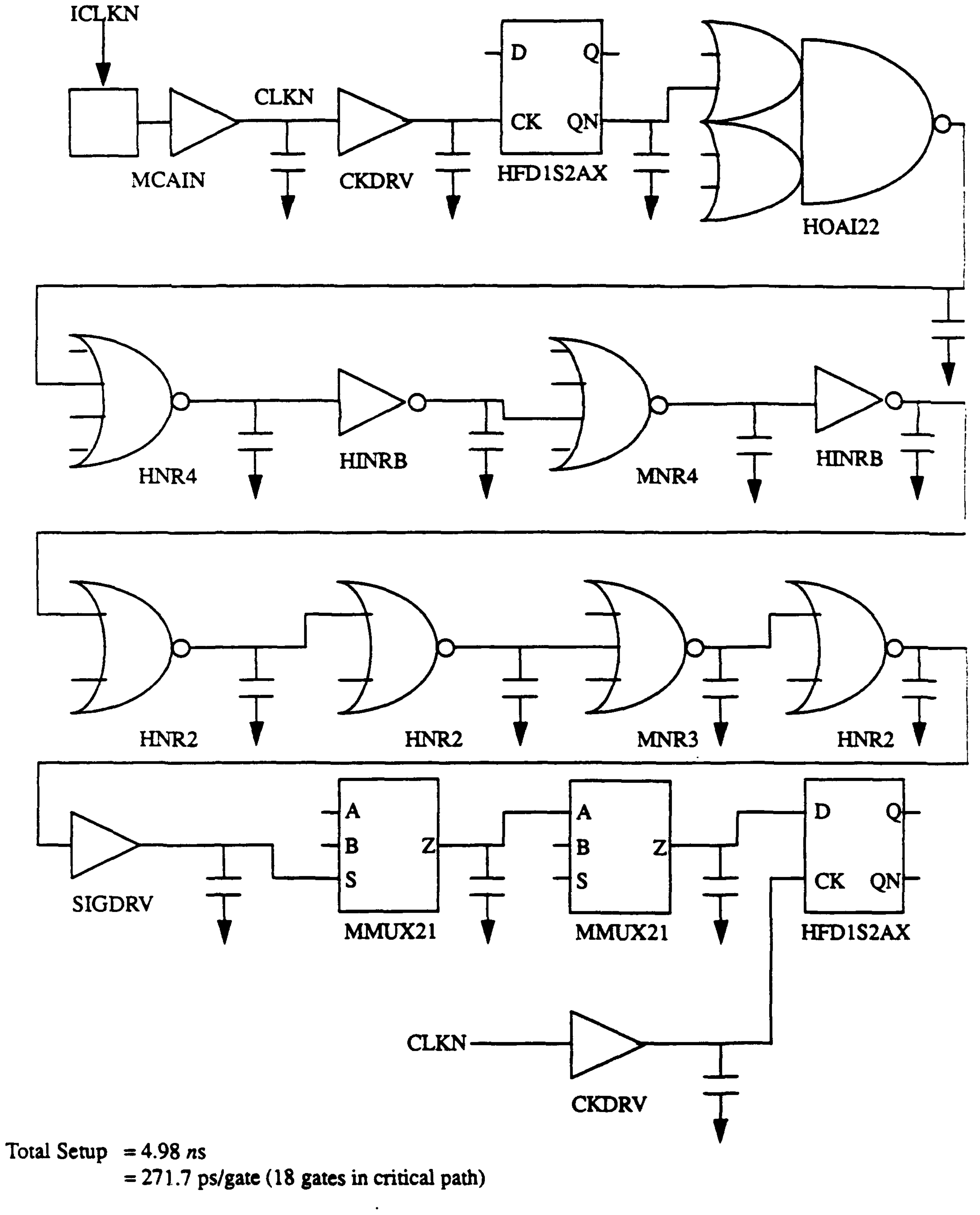
The final device size is 138 mm^2. During the final stages of design, we decided to cut the power bus between the input and output bonding pads. The Standard Cell Casino Test Chip (on which the CA-CTC is based) was impossible to test due to power bus oscillation. The separated power bus will only help during wafer test. Once packaged, all V_{DD} and V_{SS} are tied together.

The key features of this circuit are:

Number of Inputs:	98
Number of Outputs:	74
Number of VDD/GND pins:	80
Number of Logic Gates:	4126
Estimated Average Dynamic Pins:	4.8W

We fabricated 14 lots of CA-CTCs, four of them after we converted to the PP etchant and regained control of our EFETs (see Section 4.3). The CA-CTC is the largest circuit we fabricated. Accordingly, the yield of this circuit has been the lowest of all our circuits. We identified only one working chip at the wafer level and there are no fully functional packages. It is disappointing, but not surprising, that there were no fully functional chips in the four lots that used the PP etchant. Comparing the power buss and interconnect geometry and the chip size to the point defect yields described in Section 3.4, we would expect no more than a 2% yield. With 17 sites per wafer and 8 wafers that were PCM good, we would have predicted no more than 3 good chips.

Although no fully working devices were available for detailed characterization, we measured I/O levels for the vector blocks that pass.. We would expect fully functional devices to have the same I/O characteristics. A few devices satisfied all I/O level requirements through the entire 1.8 to


ICLKN
CLKN
D
Q
CK
QN
MCAIN
CKDRV
HFD1S2AX
HOAI22
HNR4
HINRB
MNR4
HINRB
HNR2
HNR2
MNR3
HNR2
A
B
S
Z
A
B
S
Z
D
Q
CK
QN
SIGDRV
MMUX21
MMUX21
HFD1S2AX
CLKN
CKDRV

Total Setup = 4.98 *ns*
= 271.7 ps/gate (18 gates in critical path)

Figure 41 - Critical Path of Cell Array Casino Test Chip

2.2V voltage range during wafer probe at 25°C. The maximum operating frequency recorded was 83.3 MHz, which is limited by the wafer probe card. Figure 42 is a shmoo plot showing the operational characteristics of a good device; the asterisk means pass. Figure 43 summarizes the I/O voltage levels of (11) packages. The main failure mechanism is high V_{OL}, especially at 125°C; detailed test set optimization and failure analysis with packaged 32-Bit Multipliers has shown that high V_{OL} is not intrinsically characteristic of the device, but is mainly due to test conditions; i.e., optimization of vector transistors. Limited 32-Bit Multiplier data at 25°C wafer probe showed that the V_{OL} level is below 100 mV in the entire 1.8 to 2.2V range.

Dynamic I_{DD}, shown in Figure 44, runs approximately 0.5A higher than the simulated 2.55A at all temperatures.

2.21 Supercomputer Test Chip Design and Test Results (P. J. Robertson, R. J. Niescier, L. R. Tate, C. H. Tzinis, and S. F. Nygren)

Because of its high-speed, low power characteristics, the GaAs SARGIC-HFET technology used in Pilot Line III has many potential applications. The main objective of Pilot Line III is to produce 4K SRAMs and 5000-gate logic circuits that operate at 200 MHz over -55 to +125°C. Logic circuits for supercomputers are another application of this technology. In this case, the circuits are held at a tightly-controlled temperature when they are operating, so these circuits can be optimized for performance at a single temperature rather than compromised by having to operate over a wide temperature range.

To demonstrate this capability, we used the SargicS.15 models to design a supercomputer test chip with ten subcircuits containing free-running and clocked ring oscillators and an 8-bit counter. To minimize power, we chose a DCFL logic family. This contrasts with the SFFL family that is used in other Pilot Line circuits to provide operation over the -55 to 125°C temperature range. The subcircuits have fan-ins up to 4, fan-outs up to 4, and wiring loads up to 3mm.

The resulting chip is 8.1 mm square. There are 312 bonding pads, 101.6µm x 63.5µm, spaced 101.6µm from center to center). Each subcircuit appears twice on the chip, once of the left half, and once on the right half. A standard process control module (PCM) is embedded within the chip; its contact pads are in addition to the 312 around the edge. Figure 45 shows the chip layout.

Table 28 summarizes the subcircuits available in this chip. Nine of the subcircuits are ring oscillators. There are variations with different fan-ins, different fan-outs, and different loads (lengths of wire). Some can be operated in either pulse or ring oscillator modes. Others have logic stages between latches or have feedback that goes off-chip. The tenth circuit is a custom designed 8-bit up-counter that was designed for maximum performance compact layout.

Except for the dielectric, we fabricated this chip using standard Pilot Line III SARGIC-HFET technology. Each of the six lots contained two ED10 MBE wafers, two ED11 MBE wafers, and two Picogiga wafers in order to maximize our chances for success. The Picogiga wafers were supposed to replicate the ED11 layer structure. (At this point in our process development, we thought ED11 would be correct, but we did not yet have sufficient data to qualify it as our standard process; Picogiga wafers were included because they had been successful with other Pilot Line III circuits). Four of the lots were processed with the standard SiON dielectric. As an experiment, the other two lots used SiO_2 in an attempt to produce faster circuits. The SiO_2 deposition was "best effort," as there is no such standard process.

Table 29 gives the yields for these lots. Of the 36 wafer starts, 33 were mechanically good (92%). As expected, the ED11 and Picogiga wafers performed equivalently, where the ED10 wafers were inferior. Unlike the Picogiga wafers used with the TFC (Section 2.18), these wafers were good approximations of the ED11 MBE layers.

```
*** SPEED vs VDD SHMOO PLOT ***
RATE
(MHz)
100|                                         |
 90|                                         |
 80|      ***  ******************************|
 70|   **************************************|
 60|*****************************************|
 50|*****************************************|
 40|*****************************************|
 30|*****************************************|
 20|*****************************************|
 10|*****************************************|
   1.5         1.8     2.0     2.2         2.5
                       VDD

MAX FREQ AT 2V IS: 83.3333333333 MHz
```

Figure 42 - Cell Array Casino Test Chip Shmoo Plot for V_{DD} vs. Speed

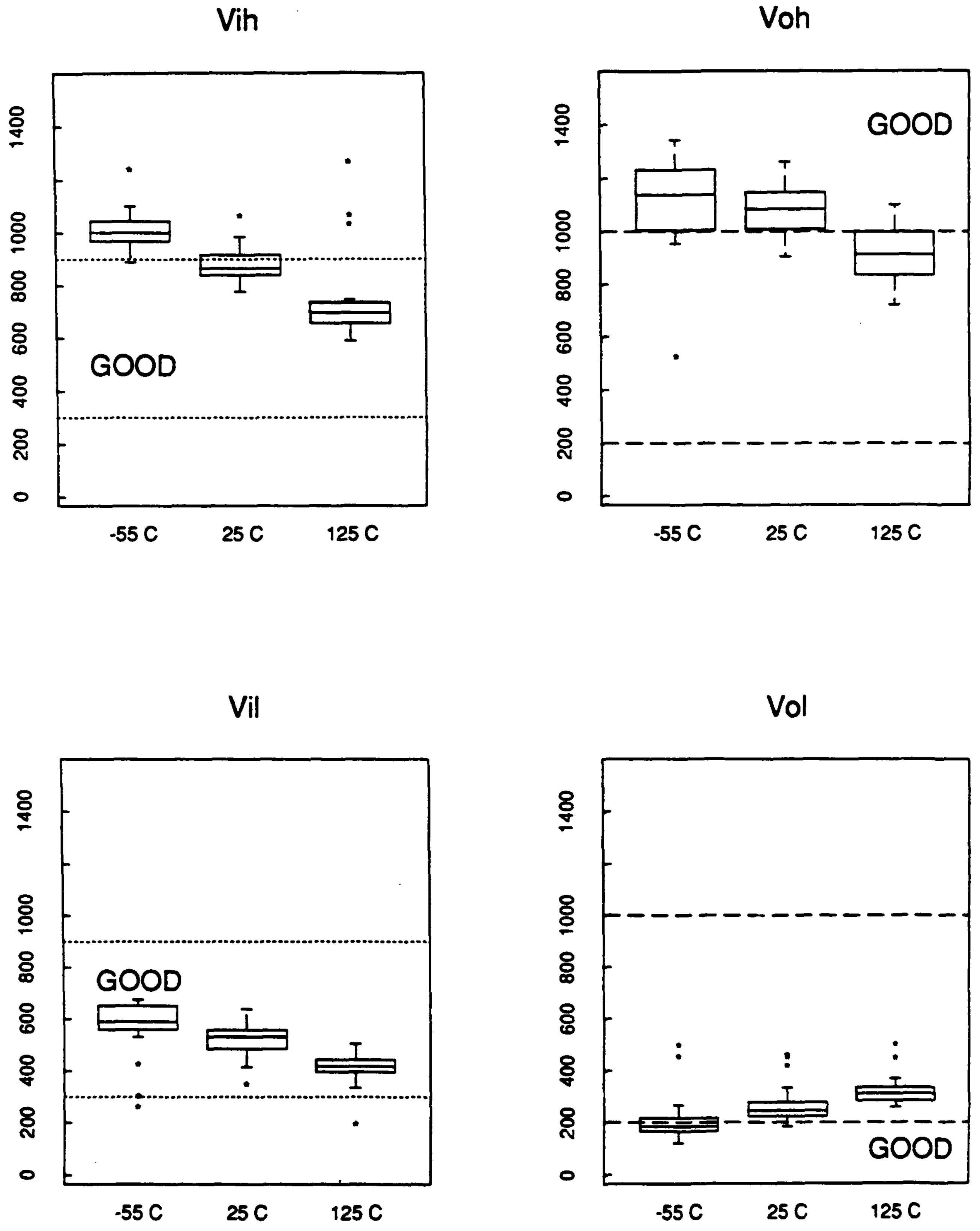


Figure 43 - Packaged Device I/O Levels for Cell Array Casino Test Chip

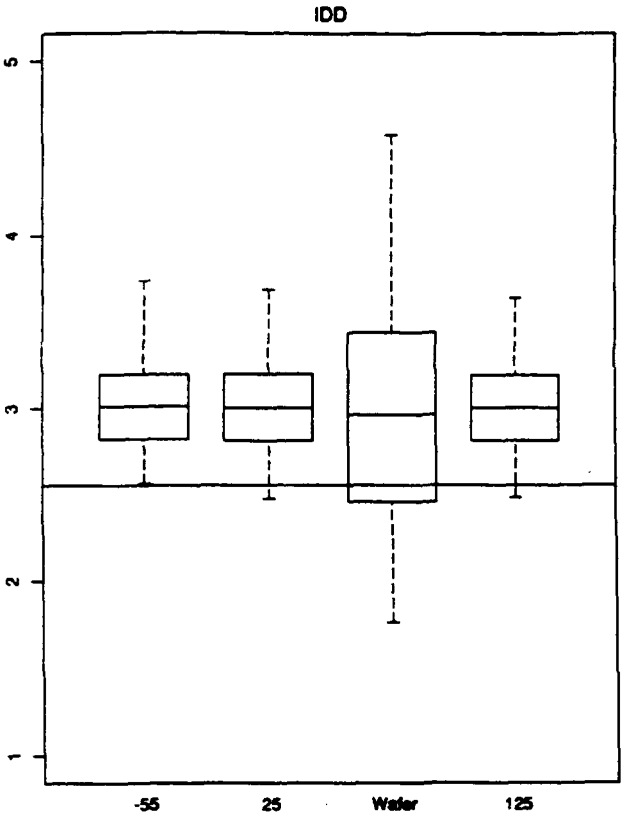


Figure 44 - Cell Array Casino Test Chip Power Supply Current

Circuit Placement

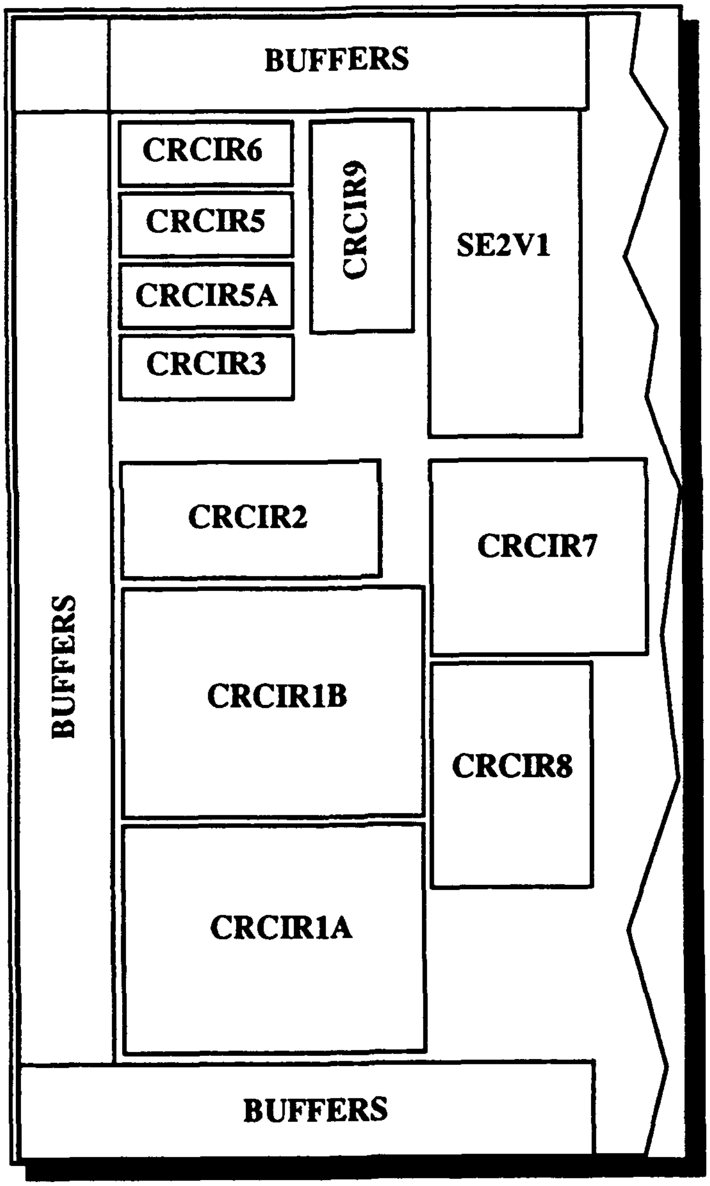

BUFFERS
CRCIR6
CRCIR5
CRCIR5A
CRCIR3
CRCIR9
SE2V1
CRCIR2
CRCIR7
BUFFERS
CRCIR1B
CRCIR8
CRCIR1A
BUFFERS

Figure 45 - Supercomputer Test Chip Subcircuit Layout

Table 28 — SUPERCOMPUTER TEST CHIP SUBCIRCUITS

Subcircuit	Function	Portion	No. Gates	No. Gate Delays	Stages	Metal	Fan-in	Fan-out	Wire
1A	Ring Oscillators (Top Metal)	1a_1	225	27	11	TMT	1	4	1mm
		1a_2		27	11	TMT	1	4	3mm
		1a_3		27	11	TMT	1	4	5mm
		1a_4		29	13	TMT	1	4	1mm
1B	Ring Oscillators (Bottom Metal)	1b_1	255	27	11	BMT	1	4	1mm
		1b_2		27	11	BMT	1	4	3mm
		1b_3		27	11	BMT	1	4	5mm
		1b_4		29	13	BMT	1	4	1mm
2	Ring Oscillators (Feedback Off Chip)	2_1	129	29	11	BMT	1	4	1mm
		2_2		31	13	BMT	1	4	1mm
		2_3		33	z	output			
3	Ring Oscillator (2 levels of logic between master and slave latches)	3	28	9	Latch Delay				5mm
5	Ring Oscillators (2 levels of logic between level-triggered latches) (Path between latches goes (off chip)	5_1	24	11	Latch + AOI Delay				5mm
		5_2		12	" " "				5mm
5A	Like 5, but wiring load is interdigitated fingers of TOPMET	5a_1	24	11	Latch + AOI Delay				5mm
		5a_2		12	" " "				5mm
6	Ring Oscillator (Multiple levels of logic between master and slave latches)	6	34	9	Latch Delay				
7	Ring Oscillators	7_1	179	27	11	BMT	1	4	1mm
		7_2		27	11	BMT	1	3	1mm
		7_3		27	11	BMT	1	2	1mm
		7_4		27	11	BMT	1	1	1mm
8	Ring Oscillators	8_1	150	27	11	BMT	4	1	1mm
		8_2		27	11	BMT	3	1	1mm
		8_3		27	11	BMT	2	1	1mm
		8_4		27	11	BMT	1	1	1mm
9	8-bit up Counter	9	125						

Table 29 - Supercomputer Test Chip Yields

	PCM Yield	**Functional Yield**
ED10	30% 3 out of 10 wafers	3.2% 20 sites out of 7 wafers
ED11	45% 5 out of 11 wafers	11.3% 112 sites out of 11 wafers
Picogiga	25% 3 out of 12 wafers	13.3% 132 sites out of 11 wafers

NOTES:

1. A PCM-good wafer has at least 6 out of 16 PCM sites satisfying:

   $40 < I_{ds}$ (EFET) < 70 mA/mm
   $65 < I_{ds}$ (DFET) < 120 mA/mm
   $2000 <$ Via chain resistance $< 20{,}000$ ohms

2. A functional-good site has all 10 subcircuits working on at least one of the two halves of the site.

Two lots were chosen for detailed analysis: 35190 (SiON) and 34960 (SiO_2). The SiON wafers have an average gate delay (NOR gate) of 193 ps and an average power dissipation of 0.8 mW/gate, so that the average power-delay product is 158 fJ. As expected, the SiO_2 wafers are faster. They have an average gate delay of 161 ps with an average power of 1.14 mW/gate, so that the resulting power-delay product is 183 fJ.

Figure 46 shows power-delay product for two wafers, one with each dielectric. For convenience, a dashed line shows 150 fJ. As mentioned above, the SiO_2 devices are faster than SiON, but they have a slightly higher power-delay product.

Figure 47 relates gate delay to fan-in and fan-out, and Figure 48 relates gate delay to wire length. The values average 3 ps/fan-in, 10 ps/fan-out, 28 ps/mm for first level metal (BOTMET), and 25 ps/mm for second level metal (TOPMET).

Finally, Figure 49 shows noise margins. Two different output buffers were designed and implemented: a 60Ω, parallel-terminated buffer and a 60Ω, series-terminated buffer. The series-terminated buffer gives somewhat higher noise margins. Its output voltage high (bs_voh) is about 1.13V; output voltage low (bs_vol) is about 0V; noise margin high (bs_nmh) is about 0.7V; and noise margin low (bs_nml) is about 0.3V. For the parallel-terminated buffer, the values are bp_voh ≅ 0.65V, bp_vol ≅ 0.03V, bp_nmh ≅ 0.23V, and bp_nml ≅ 0.28V.

Delay vs. Power

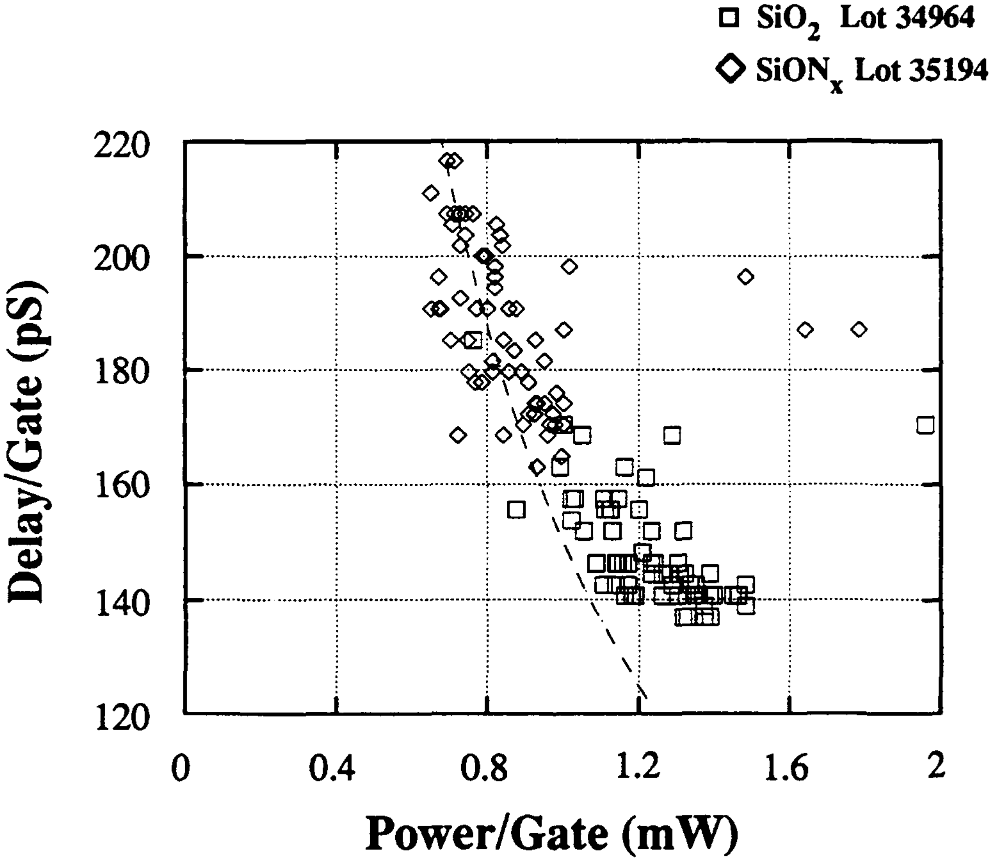
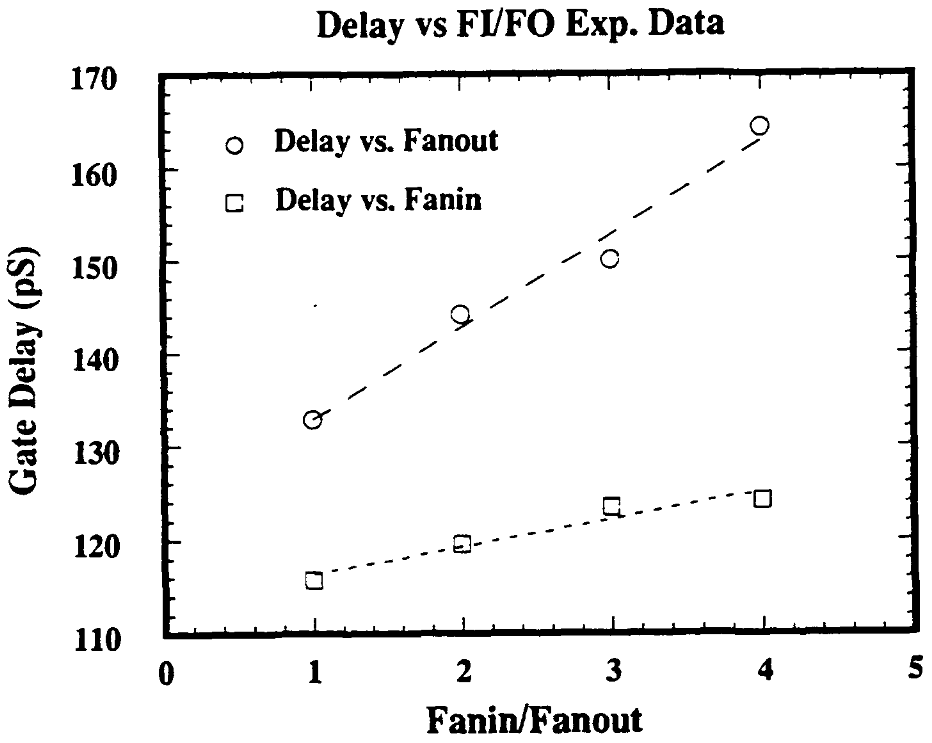


Figure 46 - Supercomputer Test Chip Delay-Power Product.
The dashed line is 150fJ.

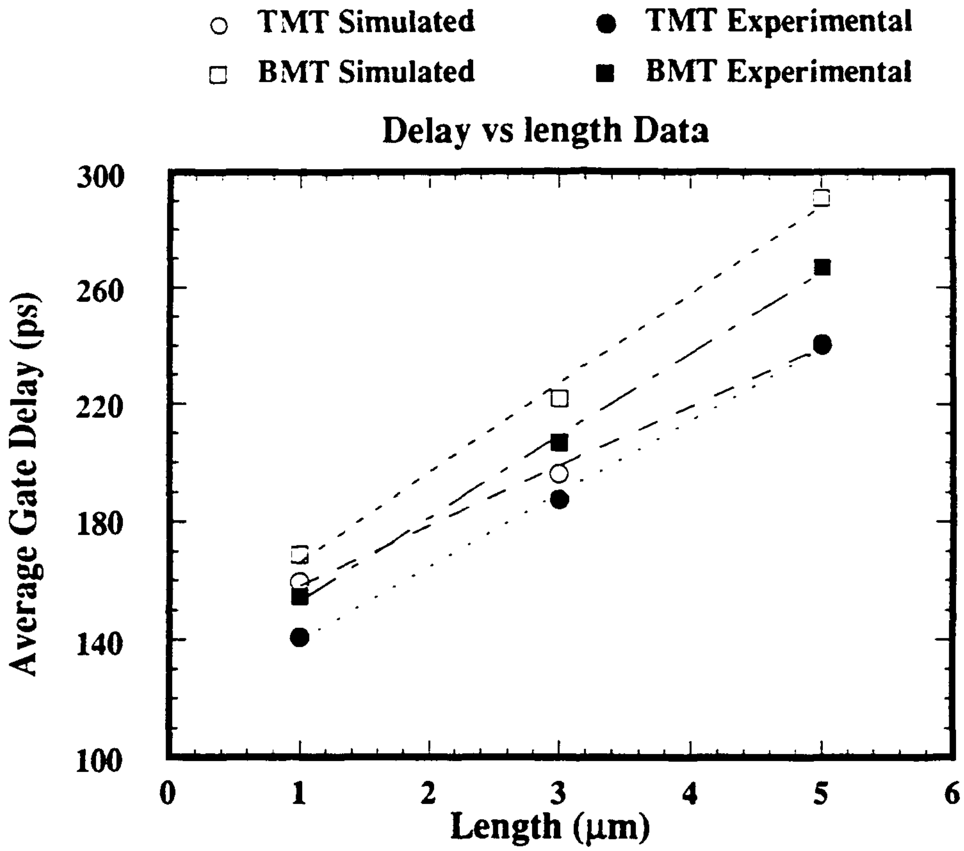
Delay Vs. Fanin/Fanout



*from Experimental Data

Figure 47 - Supercomputer Test Chip Delay Compared to Fanin and Fanout

Delay Vs. Wire Length



Data comes from simulation of circuits 1A and 1B and real data.

Figure 48 - Supercomputer Test Chip Delay Compared to Wire Length

I/O Noise Margins

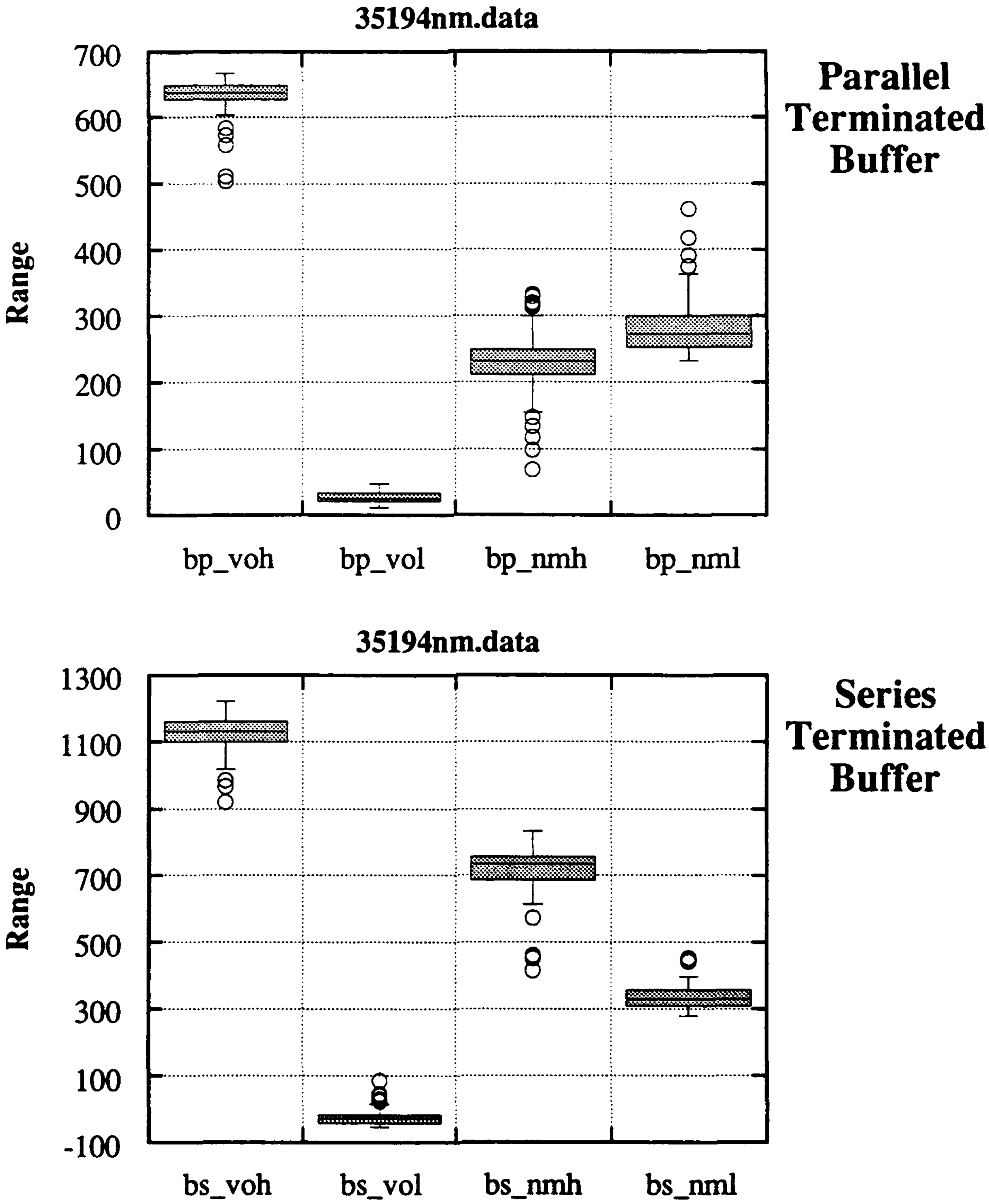


Figure 49 - Supercomputer Test Chip Noise Margins

2.22 Comparing PCM and Circuit Yield (C. H. Tzinis and W. R. Ortner)

Data analysis of PT-1 memory and especially PT-2M memory proved instrumental in model validation and in establishing correlation between PCM parameter and circuit test yields. Figure 50 demonstrates that for high circuit yield, the FET characteristics (EFET and DFET thresholds and currents) should be in a threshold window close to the one predicted by the model. In addition, empirical analysis shows that maximum yield occurs when the threshold and corresponding current follow a linear relationship (approximately constant gm) both for EFET and DFETs. Based on this analysis, criteria were established for screening wafers prior to circuit testing; these criteria are summarized in Table 30.

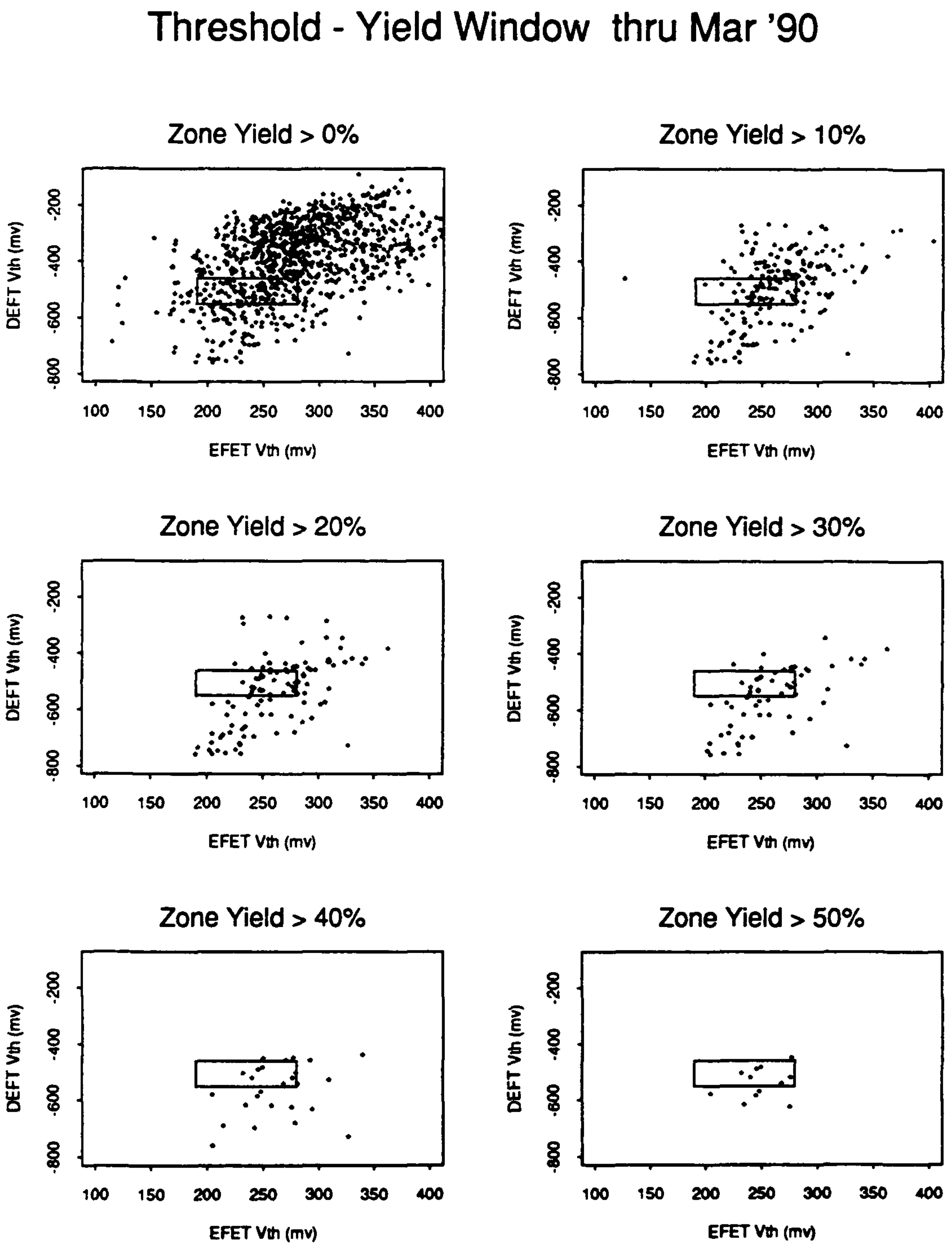
Table 30 - PCM Criteria

Parameter	Range	Units
EFET I_{ds}	$40 \leq I_{ds}$ (EFET) ≤ 70	mA/mm
DFET I_{ds}	$65 \leq I_{ds}$ (DFET) ≤ 120	mA/mm
Via Resistance	$1 \leq R_{via} \leq 20$	kΩ/4000 vias

Figure 51 shows the average PT-2M circuit yield per wafer as a function of the number of good PCM sites for a wafer; the number on top of the bar denotes the sample size for the distribution. There is a strong tendency for good PT-2M circuit yields to come from wafers with high PCM yields. On the other hand, we do not see such a correlation for logic circuits (Custom ALU, Standard Cell ALU, TFC, 1K Cell Array); apparently the need for good FET characterization is being masked by some other yield limiter.

For the Supercomputer Test Chip, Figure 52 shows the relationship between the number of good PCM sites on a wafer and the number of primary circuit sites in which all ten subcircuits are functional. The primary circuit yield increases dramatically when there are more than five good PCM sites per wafer.

In Figure 53, we show how gate delay and functional yield of Supercomputer Test Chips relate to the ratio of I_{dss} (EFET) to I_{dss} (DFET). The dashed lines show the upper and lower limits of the E/D ratio used in the SargicS.15 model. The solid curves show the computer generated local average for each value of E/D ratio. The data show that SargicS.15 correctly models these two characteristics for this circuit. The best yield and the fastest devices are obtained when the measured FET characteristics are within the target design window.



Threshold - Yield Window thru Mar '90

Zone Yield > 0%

Zone Yield > 10%

Zone Yield > 20%

Zone Yield > 30%

Zone Yield > 40%

Zone Yield > 50%

Boxed Area is sargic.11 Model Vth's Used to Design PT-2M

Figure 50 - Process Window Defined by PT-2M Yield

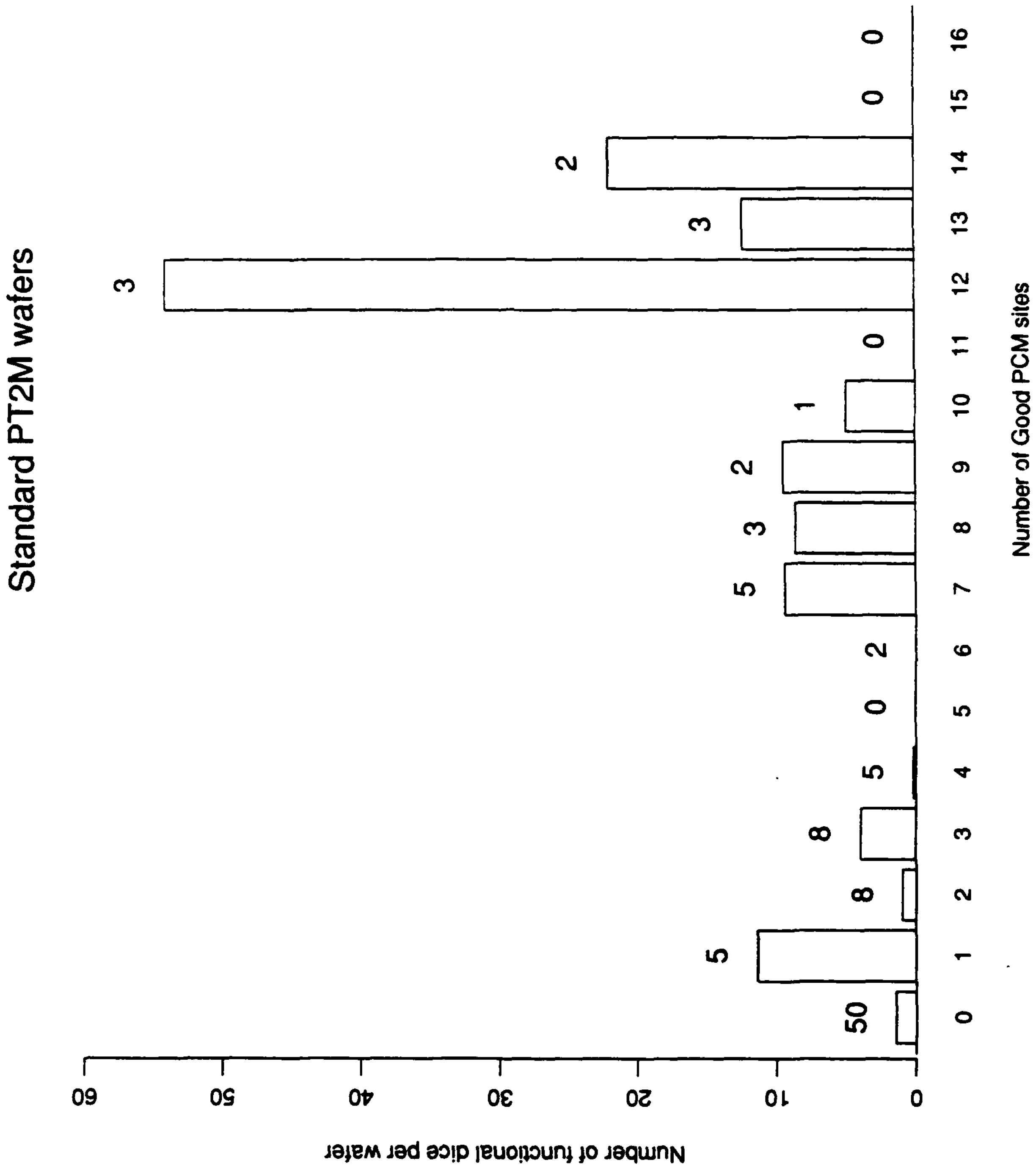


Figure 51 - PT-2M Memory Yield Compared to PCM Yield

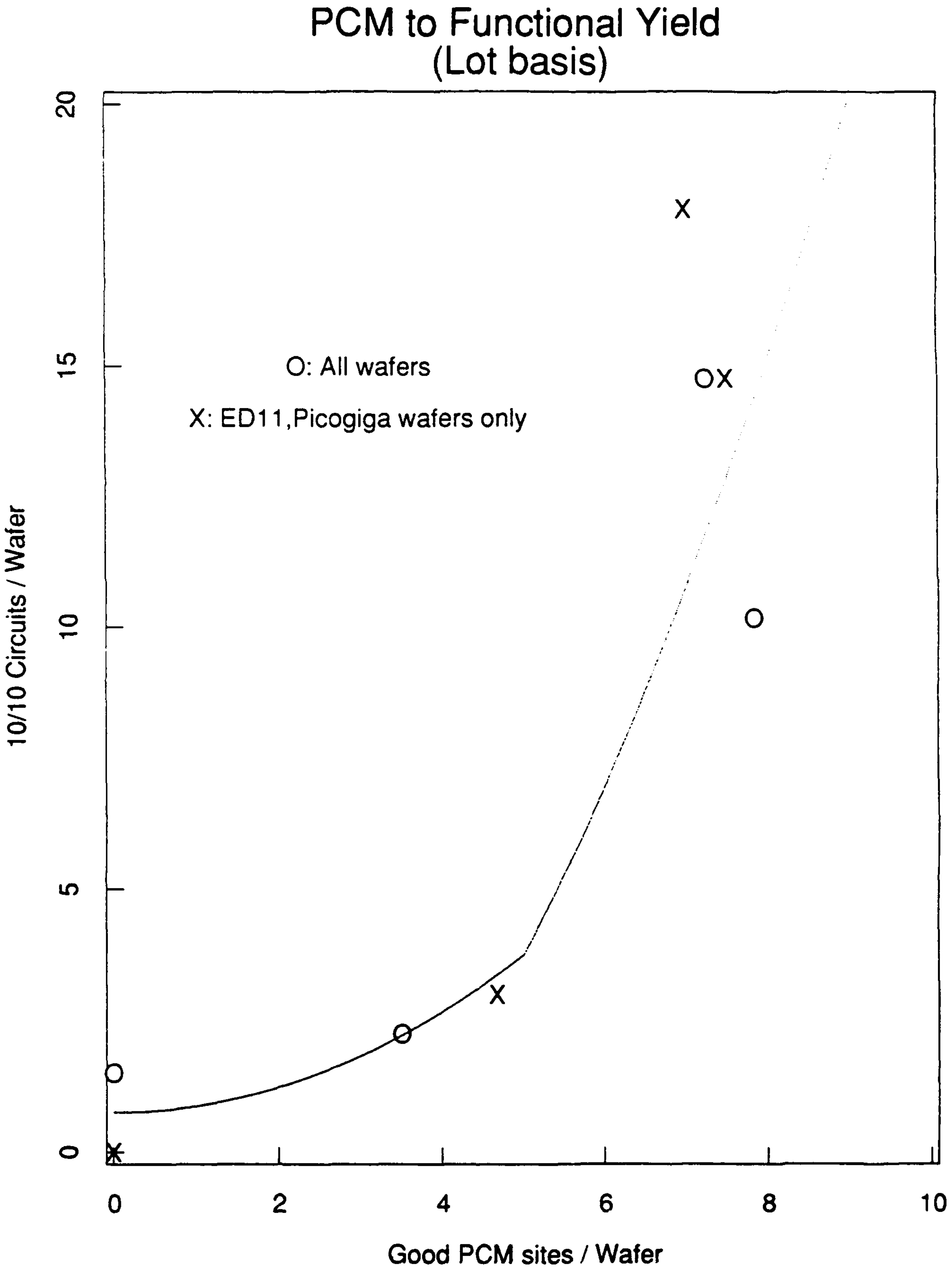
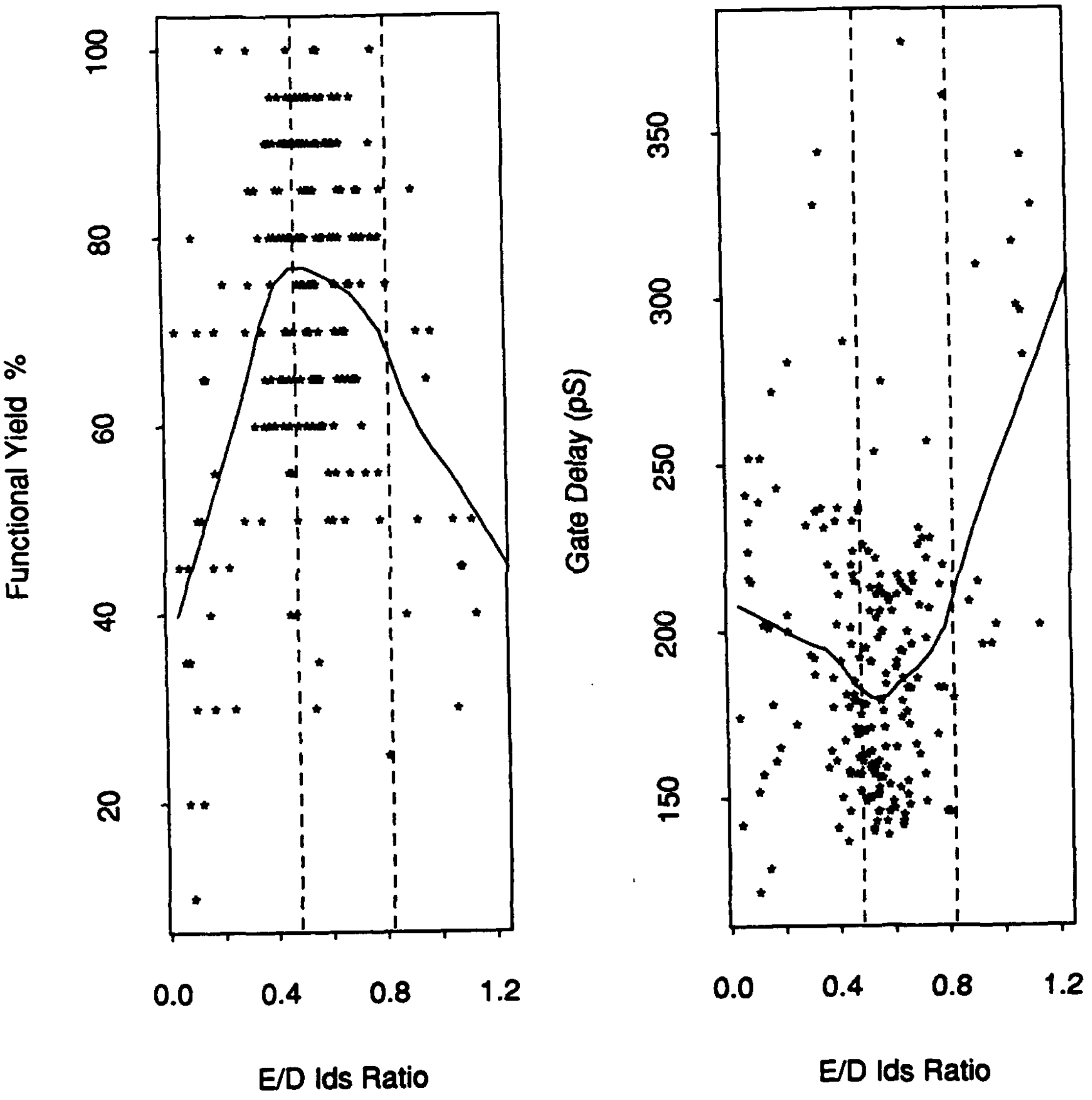


Figure 52- Primary Circuit Functional Yield Related to PCM Yield (Supercomputer Test Chip)



Dashed lines are the upper and lower SargicS.15 Model limits

Figure 53 - Supercomputer Test Chip Yield and Performance Related to EFET to DFET Current Ratios

3.0 PILOT PRODUCTION AND PROCESS DEVELOPMENT

3.1 Pilot Line Throughput, Interval, and Yield (S. M. Parker, S. S. Patel, and J. H. Duchynski)

The Pilot Line III program required the use of 3" GaAs wafers. At the beginning of this program, we moved into our new 10,000 sq. ft., Class 1/10 clean room. Except for some of the early PT-0 wafers (which were 2"), all wafers were 3". By the end of the sixth month of the program, almost all of the processing steps were being performed in the 3" clean room. The cumulative Pilot Line III wafer starts and completions for the entire program are shown in Figure 54. A total of 1877 wafers were started in the fab line, and 1344 wafers reached completion and were PCM tested. Most starts were made in the basic SARGIC-HFET process. Starts were also made in the advanced SARGIC technology for the APT-1 and APT-2 codes. Table 31 summarizes the starts and completions by code for the entire contract period.

Table 31 - Pilot Line Activity

Code Name	Wafers Started	Wafers Completed
PT-0	109	102
PT-1	598	357
Standard Cell Casino Test Chip	68	50
PT-2L	198	113
APT-1	49	37
PT-2M	244	186
Custom ALU	116	98
1K Cell Array	58	47
APT-2	29	17
Standard Cell ALU	42	34
Transversal Filter Chip	42	30
4K SRAM	108	90
Supercomputer Test Chip	36	33
Cell Array Casino Test Chip	78	65
32-Bit Multiplier	54	42
4K SRAM II	48	43
	1877	1344

Additional wafers were started in the Pilot Line for other AT&T projects. By end of November, 1991, total cumulative starts across all technologies were above 6000 wafers, and more than 4000 wafers were completed through PCM testing. The Pilot Line has a capacity of about 100 wafers per week, operating three shifts a day, five days a week. This could be increased to 300 wafers/week by adding equipment for which space is provided and appropriate additional staff. At present, roughly half the wafer starts are SARGIC-HFETs, and half are recessed-gate technologies. The SARGIC wafers include EFET/DFET wafers as were used in this program, and also DFET-only and EFET-only structures.

The computed fabrication interval for the Pilot Line codes over the length of the program is shown in Figure 55. This interval represents the sum of the average intervals of the individual process steps which are active each month. In Figure 55, the average computed interval is reported for each semiannual technical reporting period. Months in which there was a low level of activity in the line resulted in meaningless interval calculations, and those months were excluded from the averages. The training of second shift operating shop personnel began in January, 1989. The benefits of adding the second shift capacity can be seen in the reduction of the interval to approximately 35 working days in the following months. The lowest computed fabrication interval was attained during the processing of the final 16 lots in the spring of 1991, when the interval fell to 28 working days.

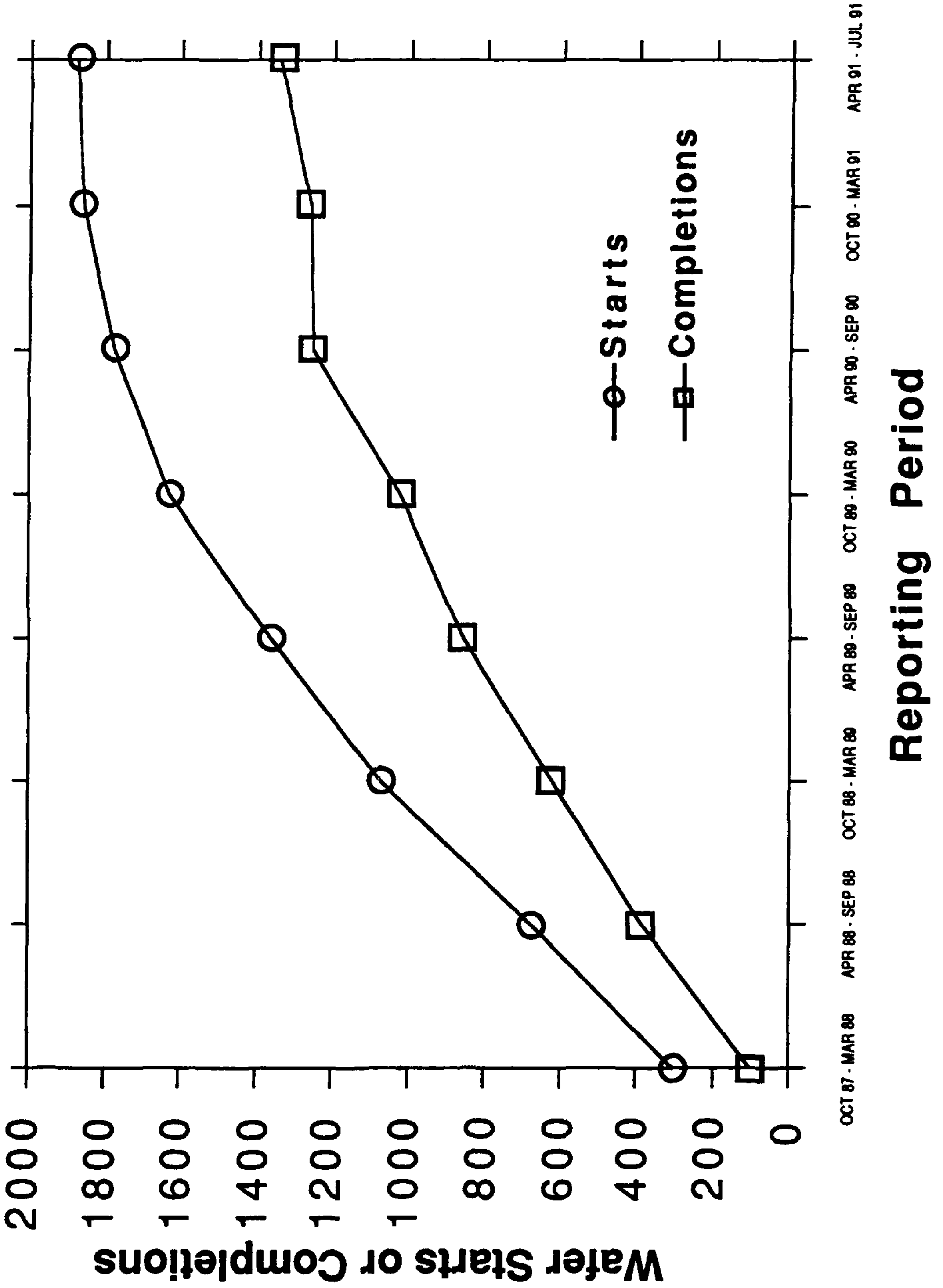


Figure 54 - Pilot Line III Wafer Fab Cumulative Starts and Completions
(Pilot Line Codes Only)

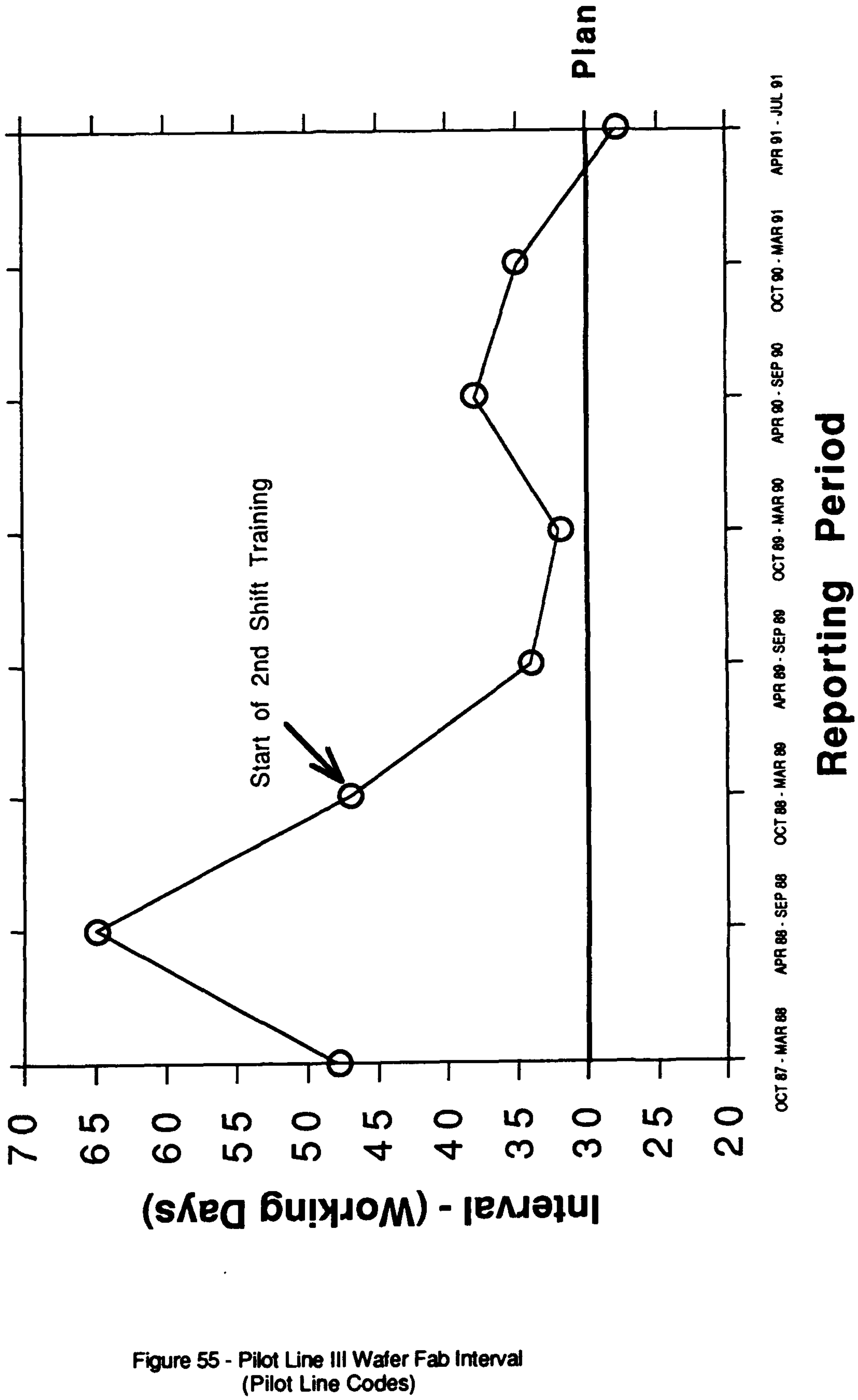


Figure 55 - Pilot Line III Wafer Fab Interval
(Pilot Line Codes)

Figure 56 shows the wafer fabrication yield for the Pilot Line codes during the course of the contract. This is a mechanical yield which compares the number of wafers which successfully complete each active processing zone to the number of wafers originally started at each of those processing zones. In Figure 56, the average wafer fabrication yield is reported for each semiannual technical reporting period. The average yield ranged from 70% in mid-1989 when a number of lots were scrapped during a prove-in of a new MBE structure (ED11) to 97% in the spring of 1991 during the processing of the final 16 lots.

3.2 Molecular Beam Epitaxy (H. H. Vuong, C. L. Reynolds, C. W. Ebert, E. L. Yachera, and J. M. Parsey)

The AlGaAs/GaAs heterostructures needed for SARGIC-HFETs are grown by Molecular Beam Epitaxy (MBE). During the initial part of the program, out efforts concentrated on adjusting the MBE layer thicknesses and doping to achieve the target FET characteristics. As a parallel effort that is still continuing, we developed improved growth and measurement techniques to enhance the quality of the layers and the manufacturability of the process.

Structure Design and Continuous Feedback from Device Results

Device results such as threshold voltage and transconductance can be calculated from material parameters such as thickness and doping levels. An AT&T device simulator program called SIGMA was used to design the MBE heterostructures required to produce the device results needed.

Several versions of the structure were used. The first three versions, ED1 to ED3, were experimental wafers used to define the number and composition of layers for the generic heterostructure used subsequently. Version ED4 was the first true production structure. The threshold voltages obtained from these wafers were found to be too positive with respect to the design targets, so a small number of experimental wafers, called ED5 and ED6, were grown to attempt to center the threshold voltages. These resulted in the structure called ED7.

Prior to the ED7 design, however, a correlation study of over fifty wafers was made, where the measured threshold voltages were compared with the values calculated from the measured material parameters. It was found that, when an empirical constant offset voltage was included, the calculated results fitted the measured ones well. This offset was used in the design of ED7. The threshold voltages obtained from the ED7 wafers were close to the design window. However, sidegating was recognized to be a serious problem for our circuits; in our wafers this was caused by the impurities at the interface between the MBE layer and the substrate. Furthermore, the empirical offset used with SIGMA was due to the presence of the same interface impurities.

A few ED8 experimental wafers were grown to study the use of ozone substrate-cleaning in reducing the sidegating by reducing the interface impurities. Meanwhile, ED9 was formed by increasing the thickness of the top layer protective cap. In a parallel effort, ED10 was designed into the old process (without ozone-cleaning) to center the threshold voltage while work on the ozone-cleaning was carried out.

Using SIGMA, ED10 was designed to center the threshold voltages of both the EFET and DFET within the acceptable ranges. The attempt was successful for the EFET but did not shift the DFET threshold voltage by a large enough amount. It was probably because the DFET threshold voltage was much more sensitive than the EFET's to the interface impurity effect which was not modeled at the time. A final redesign, which took the heterostructure from the ED10 version to ED11, incorporated both the ozone-cleaning as well as a small thickness change to center the DFET threshold voltage. This achieved its goal, within the variation of the device results. A schematic of the ED11 cross-section is shown in Figure 57.

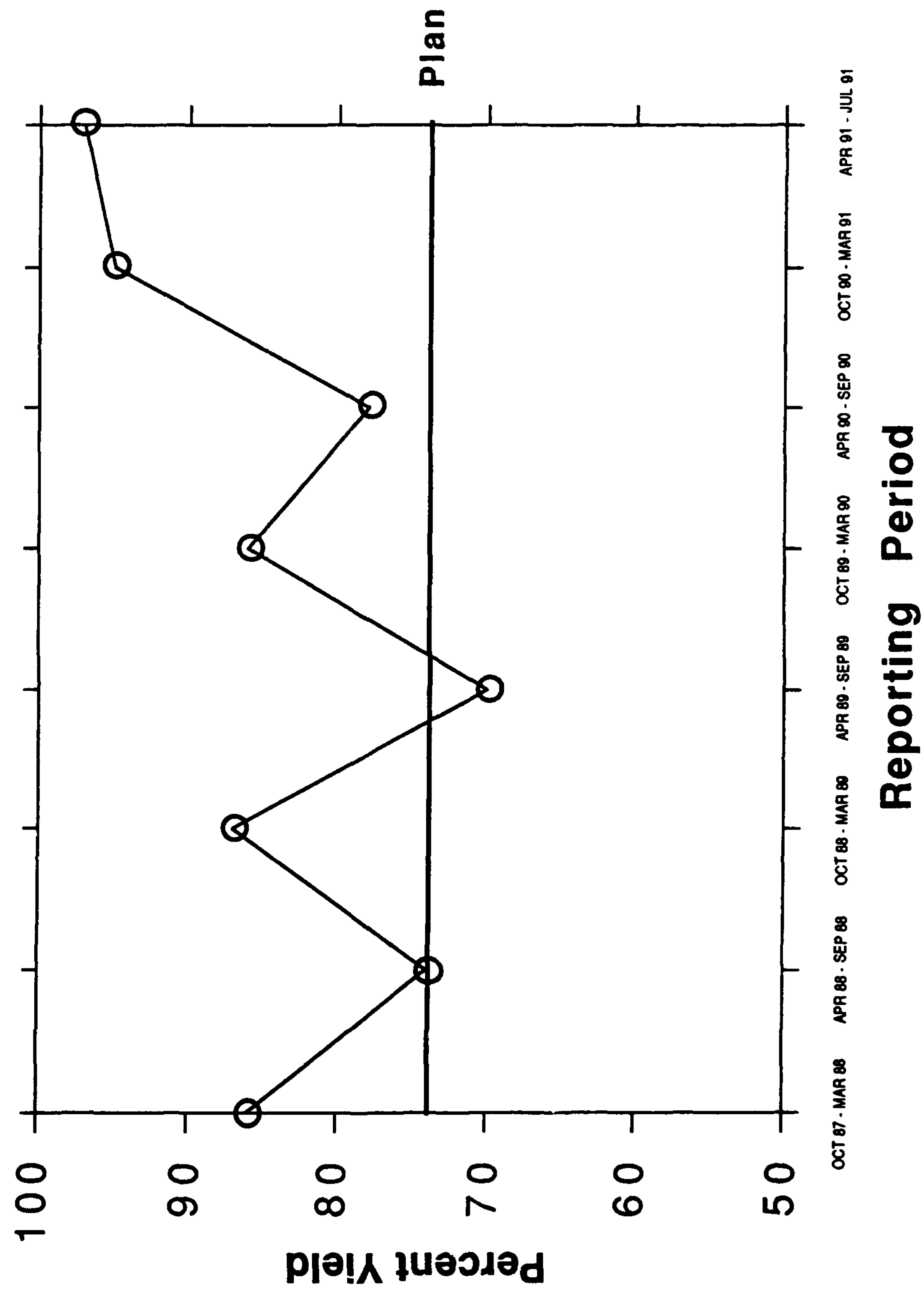


Figure 56 - Pilot Line III Wafer Fab Mechanical Yield
(Pilot Line Codes)

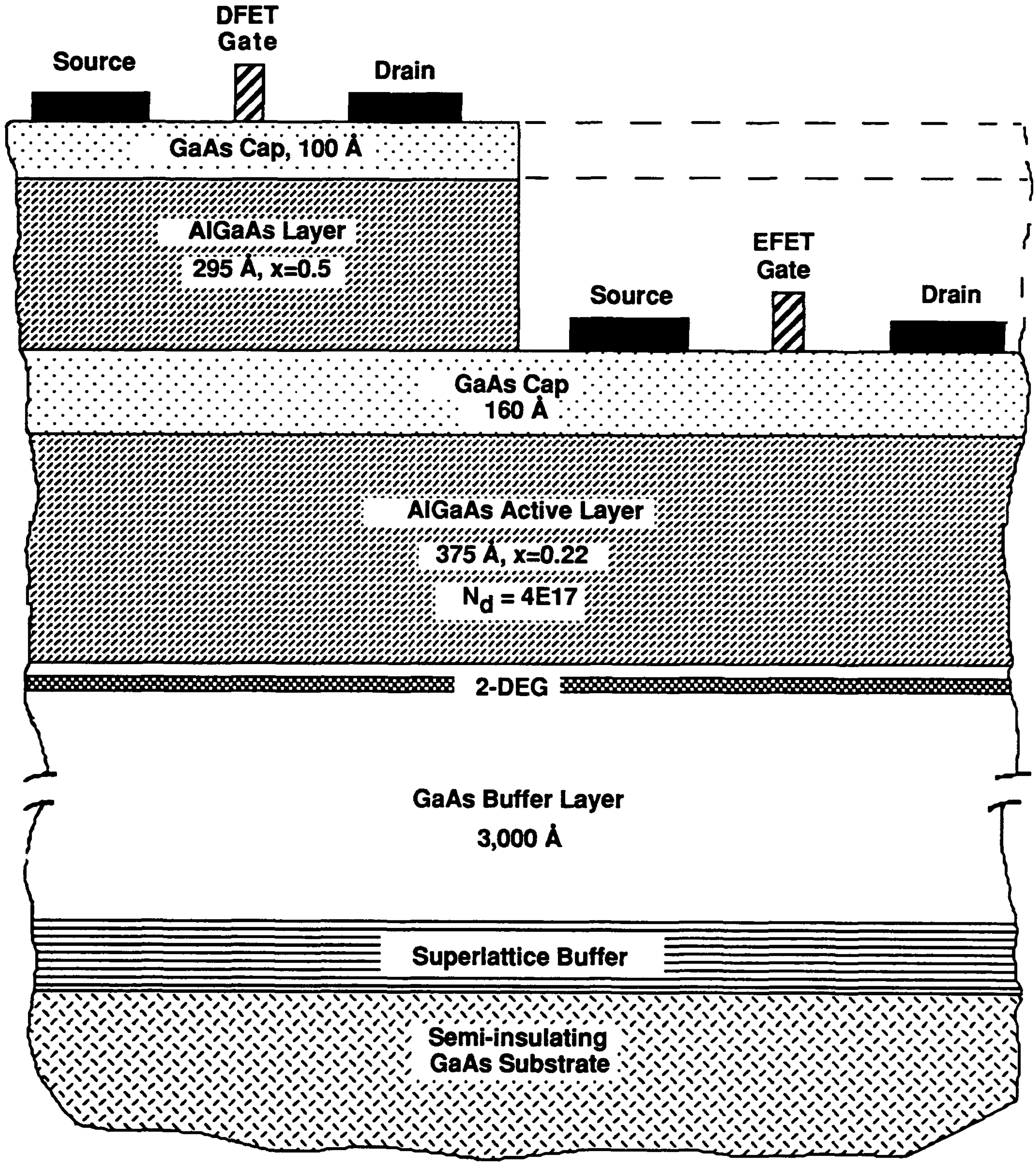

DFET Gate
Source
Drain
GaAs Cap, 100 Å
AlGaAs Layer
295 Å, x=0.5
EFET Gate
Source
Drain
GaAs Cap
160 Å
AlGaAs Active Layer
375 Å, x=0.22
N_d = 4E17
2-DEG
GaAs Buffer Layer
3,000 Å
Superlattice Buffer
Semi-insulating
GaAs Substrate

Figure 57 - ED11 MBE Structure Showing Location of DFET and EFET Electrodes

Wafer Characterization and Shipping Specifications

At the start of this program, only two characterization techniques were routinely carried out: measuring the defect densities, and measuring the mobility and free carrier concentration by the Hall technique. The former is non-destructive, and can be done on each wafer. The latter involves cleaving and testing one wafer from each batch of wafers. By analyzing the processed wafer device results, it was determined that heterostructure wafers used for the Pilot Line need to exceed a minimum mobility to produce good devices. This was included in the shipping specifications which the wafers have to pass before being processed.

Two other important parameters of the grown wafers are the thickness and composition of each of the heterostructure layers. The most accurate method of obtaining the thickness is Transmission Electron Microscopy (TEM). Unfortunately, TEM is very time consuming and cannot be done for each batch of wafers. Therefore, we made an extensive correlation of thickness measurements by TEM and by Rutherford Back Scattering (RBS) techniques. Once the correlation factors were obtained, the shipping specifications for thickness were set for the RBS technique, which can measure one wafer per batch. The window of acceptance for the thickness was set as narrowly as the accuracy of RBS allows (±20Å on each layer). In addition, RBS also measures the fractional composition of the layer with an accuracy of ±0.02. Therefore, shipping specifications for the composition were also set up with this window of acceptance.

In the last two years, we have added a contactless measurement of the sheet resistivity using the eddy current method. This is a non-destructive technique which can be used at several points on each device wafer to measure both the average and uniformity of the wafer's resistivity. The uniformity is defined as the percentage ratio of the standard deviation of the sheet resistivity across the wafer to the average sheet resistivity. By correlating this data with the final device results, the acceptable ranges of average sheet resistivity of the as-grown wafer as well as the uniformity were obtained. These were made part of the shipping specifications.

In addition to the device wafers, tester wafers are also grown. One is the doping calibration wafer grown at the start of each batch of device wafers. The doping level, which cannot be directly obtained on the heterostructure wafers, is measured on this test wafer using the Polaron capacitance-voltage technique. The doping level control is kept to ±5% at present. This represents the limit of accuracy of the Polaron method.

Table 32 summarizes the shipping specifications for the ED11 structure.

Table 32 - Shipping specifications for ED11

Parameter	Minimum	Maximum	Method of Measurement
d1+d2+d3 thickness	535Å	605Å	RBS
d3 thickness	155Å	195Å	RBS
d4 thickness	330Å	370Å	RBS
d0 A1 composition x	0.47	0.51	RBS
d2 A1 composition x	0.47	0.51	RBS
d4 A1 composition x	0.16	0.20	RBS
Doping	5.7E17 cm^{-3}	6.3E17 cm^{-3}	Polaron
77K Hall mobility	40,000		Hall
77K Hall sheet density	0.8E12	1.4E12	Hall
Defect Density	0	$250/cm^2$	SurfScan
Eddy Current resistivity	1000	1400	Eddy Current mapping
Eddy Current uniformity	0%	5%	Eddy Current mapping

The layers of the heterostructure are labelled from the surface down as d1, d2, d3, d4.

RBS, Hall, and Polaron measurements are done on calibration wafers from each growth day. SurfScan and eddy current mapping are done on each device wafer. Each wafer must also pass visual inspection, i.e. be free of scratches, chips, and haze as viewed under oblique light.

Finally, each week each machine grows a thick heterostructure tester wafer. This can be analyzed using the SEM and CL technique to ensure that the uniformity of the thickness and composition across the wafer are acceptable. This is part of the general quality assurance for each machine, which allows us to ship wafers from that machine.

Machine and Growth Procedure Improvements

Several hardware improvements were made to the MBE machines to improve the manufacturability of MBE layers. Equally important were the manufacturing practices developed both to enhance the growth itself, and to improve its implementation by teams of operators. It should be noted that all the results described here were obtained from wafers which were grown by operators and not engineers.

With the addition of the RHEED measurement (Reflection High Energy Electron Diffraction), MBE growth can be controlled within a monolayer for the thin layers whose growth time can be monitored by RHEED. The RHEED technique also enables the growth rate to be consistent, to within a monolayer, from one MBE machine to another, and from one source reload time period to another. This is of crucial help in maintaining consistent production. Recently, we have started to use a computer to automate the RHEED calibration procedure, both to achieve greater accuracy in the measurement itself, and also to account for transient effect so we can grow thick layers more accurately.

Early in establishing MBE production, the source furnaces were changed from the then standard sizes to larger sizes. This increased the machine uptime between source reloads from 20 (working) days to 40-50 days and led to a doubling of the thruput.

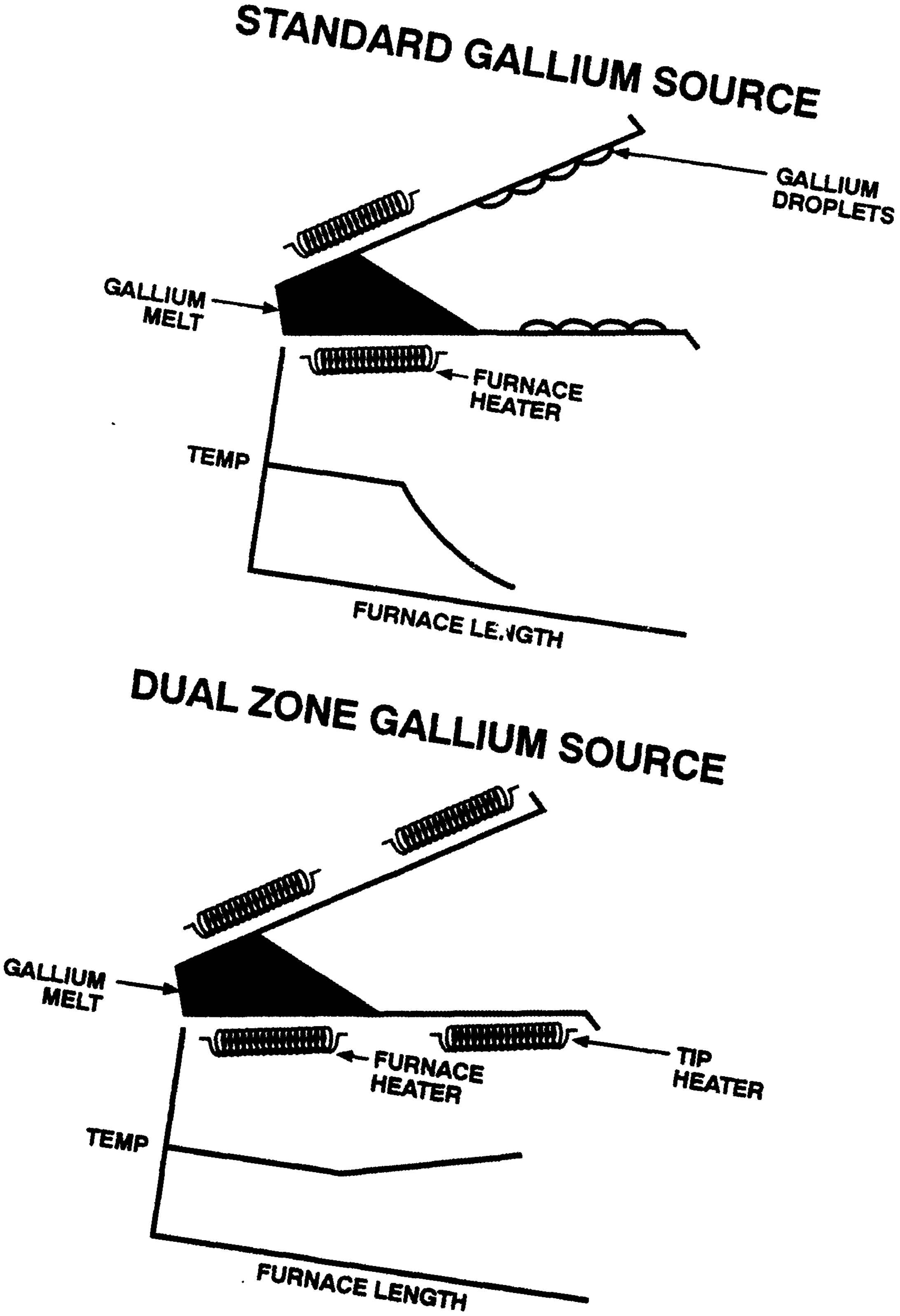
In the last year, the source furnaces for the Ga metal were upgraded, under change control, from a single heater element to dual-zone heating. The dual-zone design (Figure 58) greatly reduces the formation of Ga droplets which are the cause of the oval defects peculiar to MBE growth. At present, all three MBE machines have the dual-zone furnaces installed. As a consequence of this and of greater wafer handling care, the wafers defect densities have dropped by half on each of the production structures, for which we have adequate statistics. This is shown in Table 33.

Table 33 - MBE Defect Density in cm^{-2}

Tencor SurfScan 4500, defects in size range 0.8 to 10.24µm^2

		Defect Density with Standard Furnace		Defect Density with Dual Zone Furnace		
Epi Type	Epi Thickness	$\bar{x} \pm \sigma$	N	$\bar{x} \pm \sigma$	N	Best
MESFET 1	0.7µm	153 ± 37	20	75 ± 37	20	
MESFET 2	1.7µm	286 ± 10	20	120 ± 65	20	37
HFET ED11	0.7µm	164 ± 42	90	84 ± 39	90	10

In addition, the within-wafer uniformity of sheet resistivity as measured by the eddy current technique has also improved significantly, probably due to the removal of the Ga droplets which deformed the edges of the round furnace orifice. See Table 34.



STANDARD GALLIUM SOURCE

GALLIUM DROPLETS
GALLIUM MELT
FURNACE HEATER
TEMP
FURNACE LENGTH

DUAL ZONE GALLIUM SOURCE

GALLIUM MELT
FURNACE HEATER
TIP HEATER
TEMP
FURNACE LENGTH

Figure 58 - Gallium source designs for MBE. The dual temperature zone source substantially reduces wafer defect densities.

Table 34 - Sheet Resistivity Uniformity (from 55 measurements per wafer)

Epi Type	Standard Furnace Uniformity	Dual Zone Furnace Uniformity
MESFET 1	1.36% ± .1	0.84% ± .6
MESFET 2	0.83% ± .1	0.52% ± .1
HFET ED11	1.57% ± .4	1.20% ± .4

Battery backup has been added to all the MBE machines following a general failure due to an interruption of a power supply. This has proved effective on several occasions. Second sources for the substrates and solid sources have also been found. Finally, a second source for the epitaxial wafers themselves is also being qualified to ensure a completely stable wafer production.

Extensive work has been carried out to assess the minimum time needed to turn around the MBE machine after a source reload. This was a total of two weeks, and this procedure has become established for our operation, although under continuous revision for improvements suggested by the MBE quality team. The team was formed in 1989 and consists of all the engineers and operators involved with the MBE process. As a team, we concentrate most on the process control of the MBE machines, the wafer parameters, as well as the characterization procedures.

MBE Quality Metrics and Throughput

The MBE quality team set up three metrics which act as the main gauges for the state of MBE production. The first metric is shipment-against-plan, which is the ratio of qualified wafers shipped to the number of wafers requested. Since January 1990, the cumulative shipment-against-plan is 99.93%.

The second metric is wafer yield, which is the ratio of qualified wafers to the number of wafers grown (not including calibration set-up wafers). On average, the yield for all wafers is approximately 80%. For the heterostructure of the type used in the Pilot Line, the yield is 92% for the 559 wafers produced in 1991. For wafers which do not qualify, the reasons are recorded, and a monthly loss analysis indicates the areas which need to be improved.

The final metric is MBE machine downtime. This is the percentage of time the MBE machine is incapable of producing device-quality wafers, and therefore includes the calibration procedure time necessary after a source reload. This is one of the major concerns about the manufacturability of the MBE technique: since an ultra-high vacuum environment is required for MBE, restoring the vacuum after opening the machine to atmosphere is not a rapid procedure. Our calculated minimum downtime is 20% with the present machine configuration, assuming no machine failure so that the machine is open only for source reload. Our actual average downtime in 1991 is 22%, quite close to this minimum.

The thruput of the three single-wafer MBE machines presently in use averages 75 qualified wafers per week.

3.3 Baseline Technology (A. G. Baca, C. L. Reynolds, Y-C Shih, H-H Vuong, A. D. Brotman, R. H. Burton, and S. F. Nygren)

The baseline technology for this program is an EFET/DFET process using heterostructure FETs. Figure 54 schematically shows the cross-section of typical devices. The FET channel uses a two dimensional electron gas (2DEG). The DFET is on the gallium arsenide surface of the completed wafer, while the EFET is in an etched tub that is approximately 400Å deep. Refractory WSi gates are deposited in a self-aligned process. Besides the gate, there are three metal layers: Au-Ge ohmic contacts, Au bottom metal, and Au top metal. Bottom metal is separated from the GaAs by SiON dielectric. We call this technology SARGIC-HFET, for Self-Aligned Refractory Gate

Integrated Circuit - Heterostructure Field Effect Transistor. Complete details of the design and layout rules are in Appendix A.

Initial Development

At the beginning of the program, we had to demonstrate that our basic device structure could be fabricated in our Pilot Line. The first steps included the development of material-selective etches for defining enhancement and depletion mode transistors, a tungsten-silicide refractory-gate technology, an implant/anneal process which preserves two-dimensional electron gas integrity while allowing low source resistances, and a low-stress silicon oxynitride for insulation between metal layers and for final device passivation. This was initially done using design rules calling for 3.5µm lines and spaces.

Then, to achieve the stated circuit design speeds, a reduction in design rules from 3.5µm lines and spaces with 2.0µm vias to 2.0µm lines and spaces with 1.5µm vias was achieved using liftoff with reentrant angle photoresist and evaporated gold. The via and interconnect process was successfully tested using PT-X. The 2.0µm design rule process with two levels of interconnect was evaluated for the first time on PT-1. Several via testers were used to test the effect of extra morphology expected from the extra level of interconnects in the two-level metal process. Preliminary indications were that the via process is adequate for reasonable yields on PT-1 and PT-2, but that further improvements would be required for circuits of 5K gate complexity.

In addition, a planar isolation process based on ion implantation of oxygen was implemented. This achieves lower and more reproducible isolation currents than the mesa isolation method, and it survives the high temperature anneal. The planar process is important because it places fewer constraints on the photolithography and is expected to promote high yield. The EFET formation process window was improved by means of a stronger HF solution and longer etch time in order to reduce the induction time observed in the AlGaAs etch.

In the last part of the initial process development, the reproducibility of the pre-gate AlGaAs removal etch was improved by automating the etch. Before introduction of the automated process, etching was inconsistent near the center of the wafer (though consistent near the outside), as monitored by the E-D step height. After introduction of the automated etch, the E-D step height uniformity improved, as did V_{th} uniformity.

Via yield was improved for testers with morphology. Failure Mode Analysis indicated that WSi adhesion problems were responsible for initial low yields on the via1-via2 tester. Improving the oxide removal prior to gate deposition resulted in better adhesion of WSi and a factor of three improvement in the via1-via2 yield.

Particulates on WSi gates were observed by SEM and TEM measurements after furnace annealing. The particulates were identified by Auger microanalysis as GaAs and were not visible by routine optical inspection. The GaAs particles resulted from a temperature gradient between the cold and hot zones of the furnace, allowing some of the wafers to sublime GaAs when the As flow was shut off. A solution to the problem required elimination of the temperature gradient.

Gatelength control was monitored by means of a split cross bridge and is shown in Figure 59. Optical lithography with a monochromatic light source and a reflective (WSi) substrate places stringent requirements on photoresist thickness in order to minimize linewidth variation due to diffraction effects. Control of the process has been improved primarily by reducing the thickness variation of the photoresist for gate lithography.

Sidegate susceptibility of the SARGIC-HFET devices has been characterized, and process modifications are being investigated to reduce its impact. Figure 60 shows the effect of sidegate voltage on I_{dss} with a 2µm sidegate spacing. Recent work has shown that by extending the implant isolation through the superlattice buffer, sidegating is reduced to a considerable extent, as shown in Figure 61.

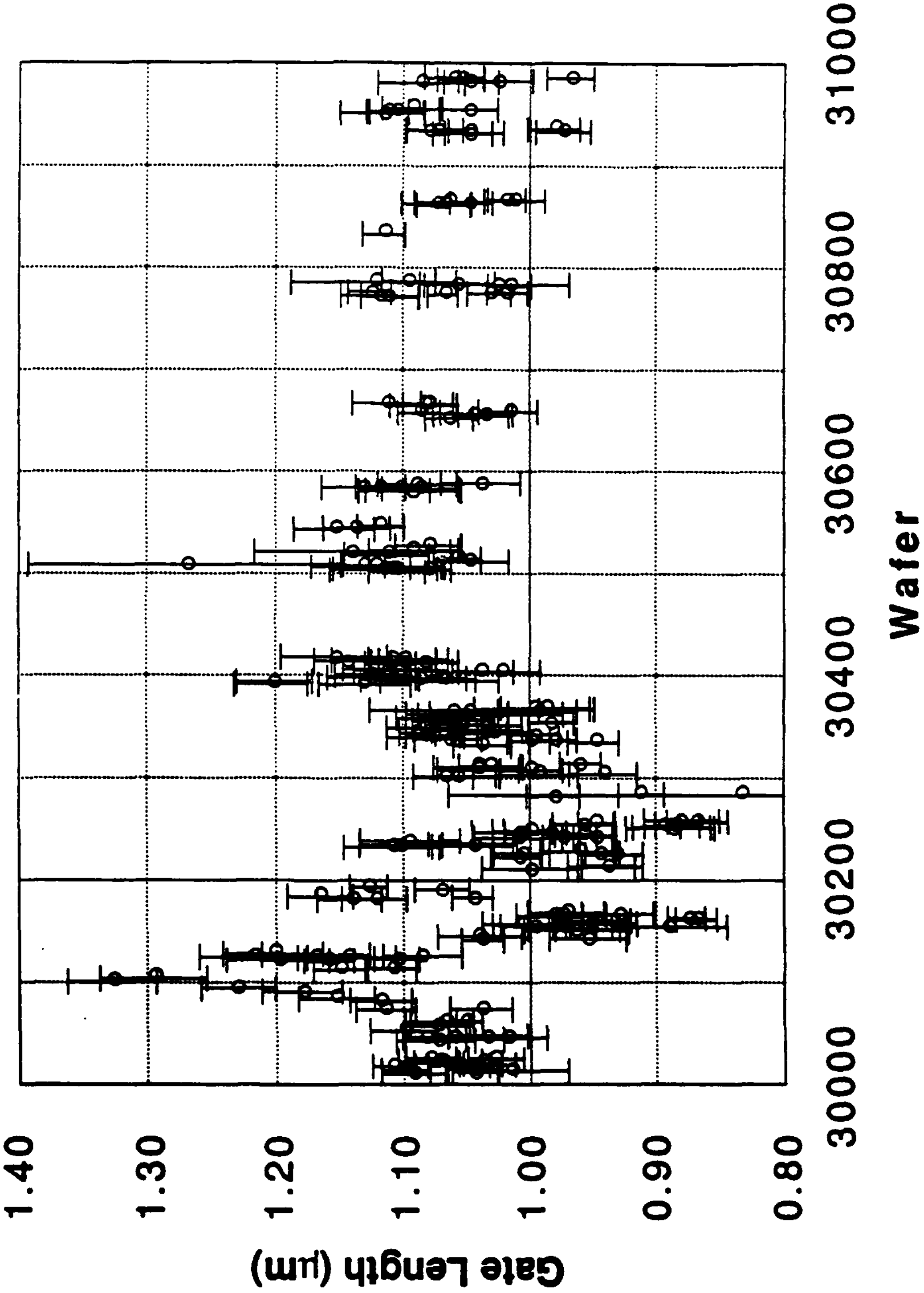


Figure 59 - Gatelength Process History

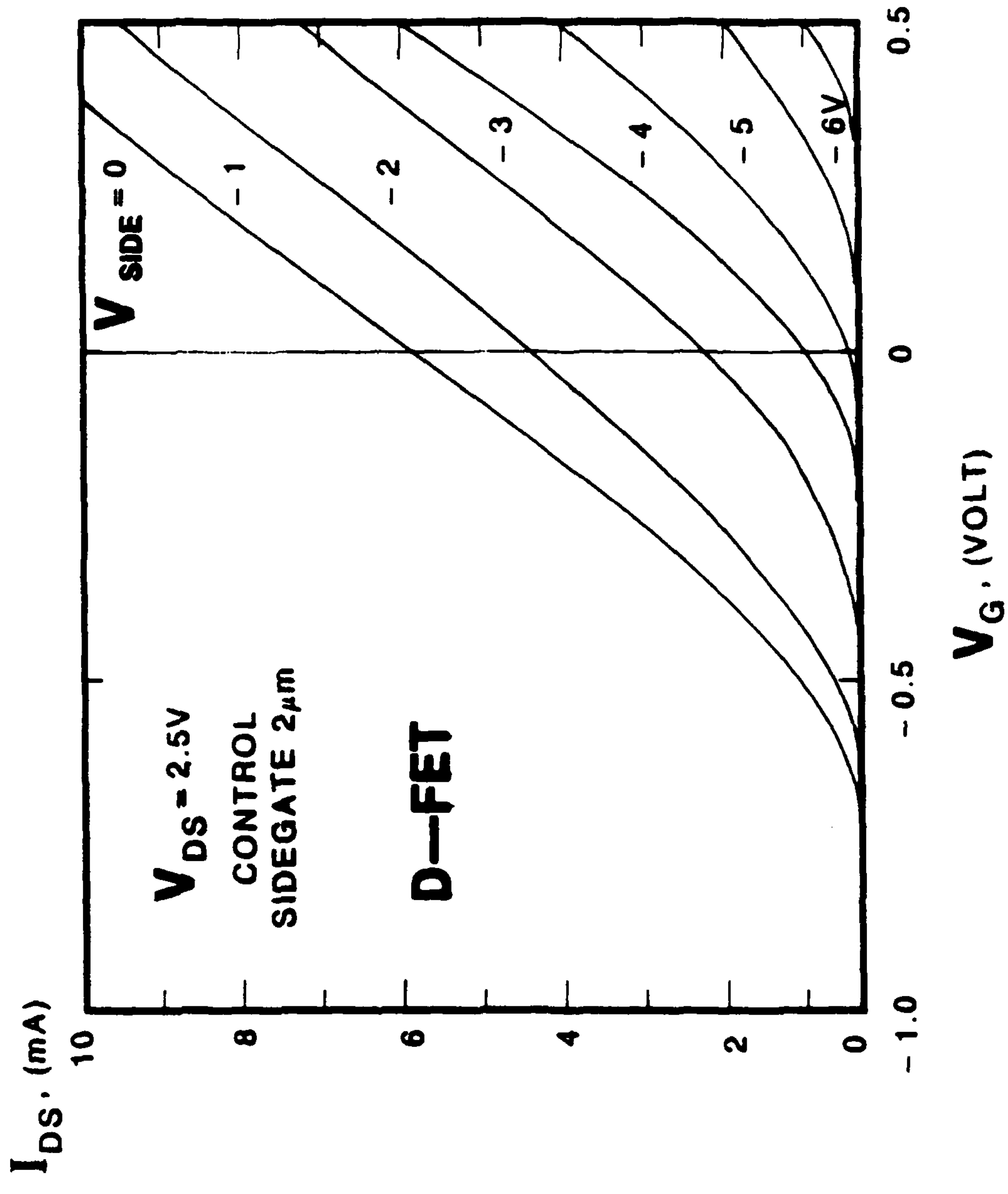


Figure 60 - Effect on I_{DS} of a Sidegate with 2μm Spacing

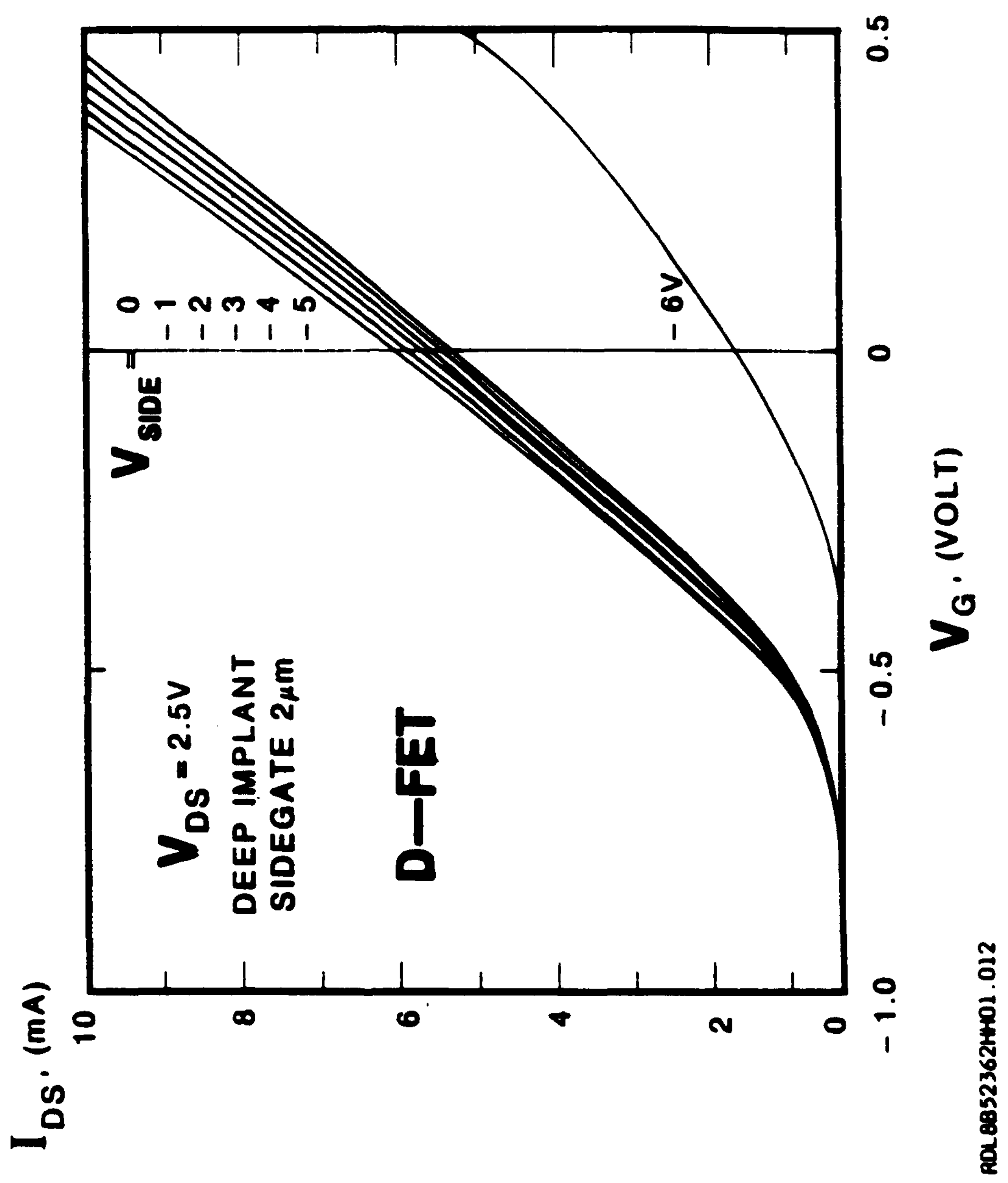


Figure 61 - Effect on I_{DS} of a Sidegate with 2μm Spacing. Sidegating is Reduced by Extending the Implant Isolation Through the Superlattice Buffer

Manufacturing Issues

Once the initial process development was complete, we turned our attention to manufacturing issues like process variations. A major concern in the manufacture of SARGIC-HFETs is uniformity and reproducibility of FET thresholds. A continuing task in the Pilot Line program was to reduce threshold variations. Figure 62 schematically shows the improvements that were made in 1989. For example, the standard deviation, σ, of the inter-wafer variation of the EFET Threshold Voltage (V_{th}) was reduced from 100 mV to 30 mV, and σ of DFET V_{th} was reduced from 160 mV to 100 mV. The improvements resulted from tighter control of key processes, many of which were identified by the focus team set up for this purpose. The key processes were:

1. MBE growth, which implemented daily calibration of layer thicknesses and doping, and which has stringent criteria based on these and other parameters for shipping wafers into the processing line.

2. Furnace anneal, where a dependence of V_{th} with wafer position in the furnace boat was identified and eliminated by avoidance of certain positions and by keeping a constant thermal mass during each run. This also largely eliminated the GaAs particulate deposition.

3. Gate metal deposition. We found that the gate metal composition varied at the end of a gate target life, thereby introducing additional V_{th} variation. Daily calibration of the gate metal composition is now implemented.

After the major improvements which were implemented in 1989, the variation of FET parameters continued to be small. However, while the EFET threshold voltage for ED10 was well centered within the target window, the DFET threshold voltage was too positive. Figure 63 shows the difference between the measured and predicted threshold voltages. The distribution for the EFET was centered near zero, which is optimum, and that for the DFET was centered around ~60 mV. This discrepancy was significant with respect to the target window and was consistent with a shift calculated for the effect of a carbon impurity layer at the interface. Some positive shifts of threshold voltage with the ED10 structure were correlated with eddy current sheet resistance (R_S) which were too large, and thus, a specification on R_S after MBE growth was initiated.

To bring the DFETs on-target, we made our final MBE structure change: ED11 became our standard. The ED11 structure is closer to target than the ED10 for the DFET threshold voltage and current, the EFET and DFET breakdown voltages, and the EFET and DFET sidegating currents. The ED11 EFET threshold and current are about the same as ED10 (that is, they are on target). The ED11 structure also shows softer pinchoff characteristics than ED10.

Several key issues with respect to the Pilot Line baseline technology arose during this period. FMA of the PT-1 memory circuit showed that some circuits fail by means of via blowout in some locations within the circuit. Close examination of the layouts showed that a lower metal layer, usually gate or ohmic, was too close to the via, resulting in formation of the via over severe morphology. Circuits designed before a design rule update of August, 1988, were susceptible to this problem. A full review of design rules resulted in a more conservative approach to all design rules.

Also during this period, a re-entrant via profile was found to cause poor step coverage of the interconnect metal. The via profile had changed as a result of contamination in the etch chamber, which was cleaned. Optimum etch conditions were then determined by means of a statistically designed experiment, and the via contact resistances returned to their normal, low values. The via profile problem resulted in several flawed wafer processing lots.

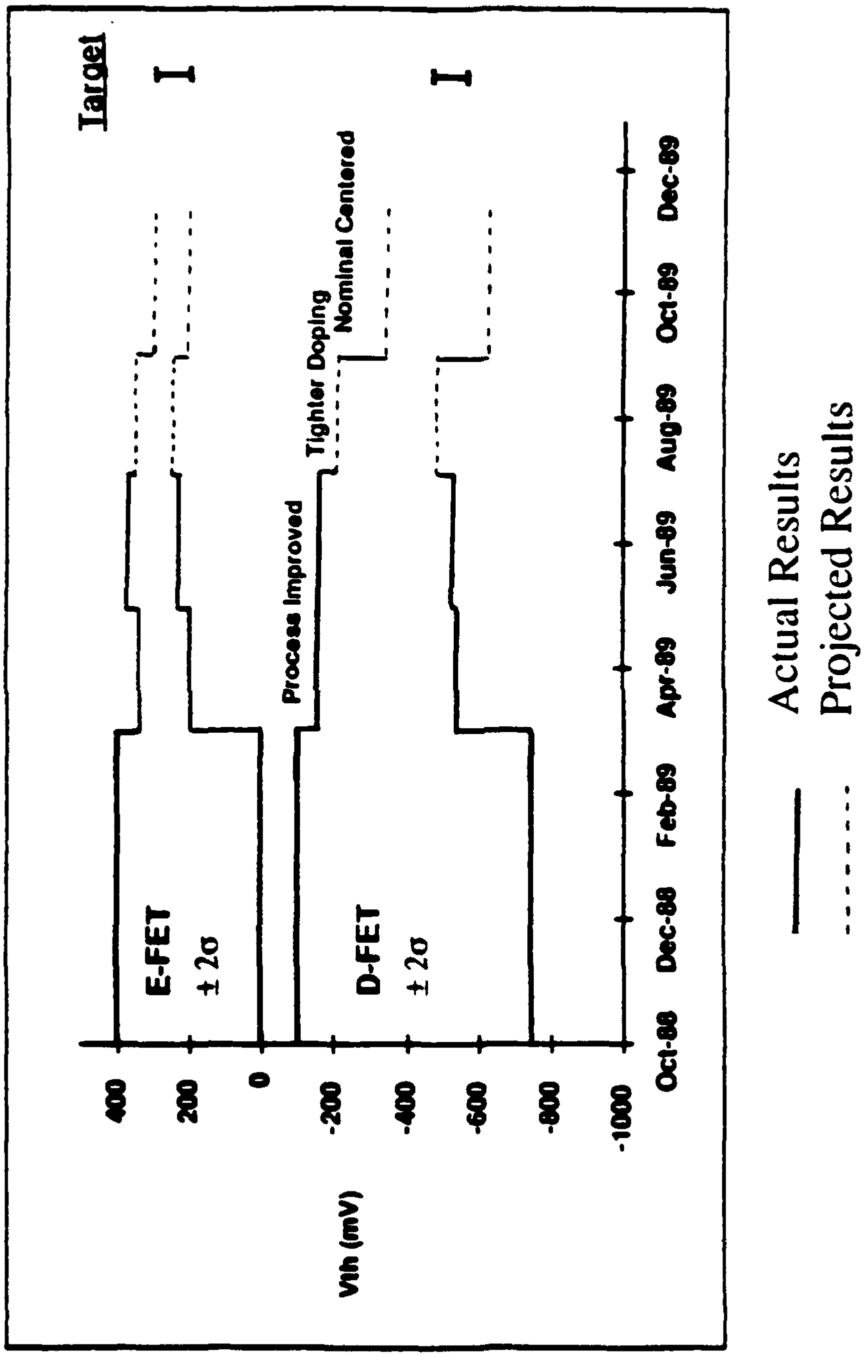


Figure 62 - Progress in Vth Control

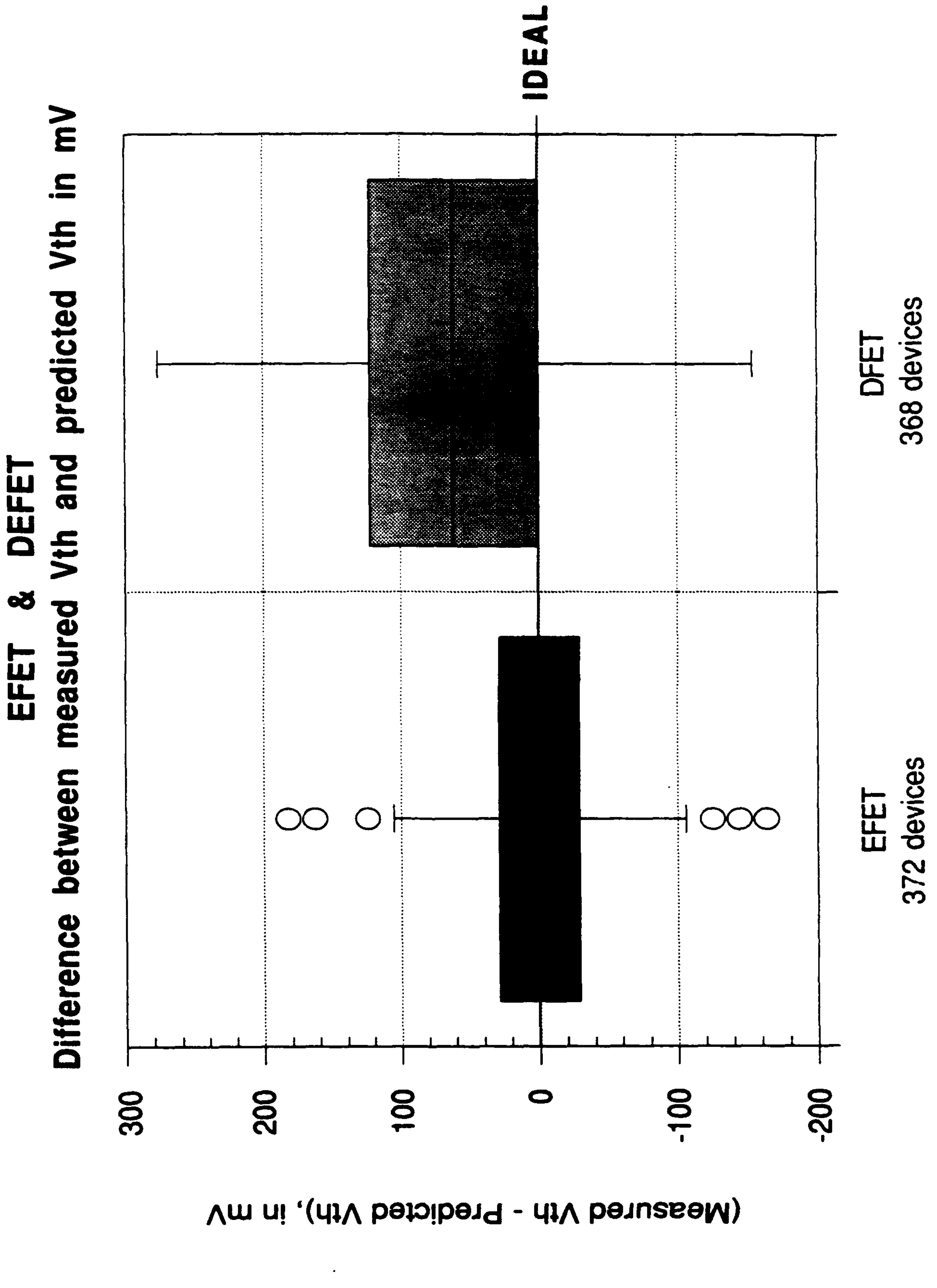


Figure 63 - Comparison of Measured and Predicted Threshold Voltages for ED10 MBE Structure

Final Development

An expected benefit of the change to the ED11 structure was a reduction in the sidegating which affects the performance of LSI circuits with small design rules. A negative potential to the ohmic contact of one device can reduce the drain current of a nearby device. The improvement with ED11 results from the order of magnitude or greater reduction in the amount of carbon at the substrate/epitaxy interface as a result of doing an ozone clean to the substrate prior to loading the wafer into the MBE system. To compare sidegating with ED11 to sidegating with each version of MBE growth, an appropriate figure of merit is the percent of channel current remaining when -2V is applied to a sidegate contact 2μm away from the device in question. With ED11 the percent of channel current remaining is 92%, while it is only 41% for ED10. Sidegating for ED11 is comparable to that for Picogiga wafers, which also have a reduced amount of carbon at the interface.

We discovered that our FETs were not symmetric. We found that a FET with its source toward the wafer flat had a more negative threshold voltage than the same FET with its drain toward the flat. (That is, even though the FETs were supposed to be geometrically symmetric, their characteristics changed when the electrical polarity was reversed.) This asymmetry was traced to the n+ implant used to make the ohmic contacts. The n+ implant step was symmetrized, and now the devices are symmetric. Figure 64 shows these results for EFETs and DFETs. Lot 36200 (1st 4 wafers) was implanted using the old recipe resulting in 10-15 mA/mm asymmetry in I_{dss}. Lot 36800 (last 4 wafers) was implanted using the new recipe resulting in symmetric devices. In the figure, the plotted asymmetry is the change in I_{dss} when the polarity is reversed.

Based on the results described earlier, ED11 was introduced into the Pilot Line. Initially, the production ED11 wafers performed the same way as the experimental ED11 wafers. Then we saw a sudden increase in the EFET threshold voltage and diode voltage of about 100 mV. The DFET characteristics were not affected. See Figure 65 for the EFET data. We examined the obvious possible causes for threshold shift (e.g MBE layer thickness and doping, furnace anneal process), but we found no problems with them. We therefore suspended wafer starts and initiated a more extensive failure analysis.

Scanning electron microscope examination of device wafers suggested improper etching of the AlGaAs etch stop layer during formation of the EFET tub. See Figure 66a for an SEM photo of a rough tub with residual AlGaAs. These results were confirmed by transmission electron microscopy (TEM) and static secondary ion mass spectrometry (static SIMS). TEM observations revealed the presence of a non-uniform AlGaAs layer under the WSi gate, while static SIMS showed AlGaAs in the EFET tubs immediately prior to gate deposition. Data in the literature indicate that the Schottky barrier height of a metal on AlGaAs increases from ~0.65V to 0.9V as the Al fraction increases from 0 to 0.5. We concluded that AlGaAs remaining in the EFET tubs was the source of the threshold voltage problem. Wafers fabricated with an EFET-only process (that is, no DFET layers and no tubs) had the same threshold voltages as the original experimental ED11s. This also supports the above conclusions about residual AlGaAs in the EFET tubs.

On the basis of etching studies, we determined that the problem was related to the KI/I_2 EFET tub etchant, so we sought a replacement. The PA (NH_4OH and H_2O_2) and PP tub (H_3PO_4 and H_2O_2) etches were more effective than KI/I_2 in removing AlGaAs in the EFET tubs. The PA etch is advantageous because it has different etch rates in GaAs and AlGaAs, while the PP etch has the advantage of being used in other GaAs wafer fabrication and in being automated. See Figure 65b for an SEM photo of a smooth tub.

To choose a new tub etchant, we collected electrical data using our SARGIC-SA process from nine lots in which the tub etchant was split among KI/I_2, PA, and PP. The SARGIC-SA process is used for other AT&T wafer fabrication and is similar to the process used in all previous Pilot Line lots (SARGIC-S). The SARGIC-SA process differs in two ways from SARGIC-S. It uses 1) a bilayer WSi/W gate metallization and 2) a higher (1.5E14 vs. 1E13 cm^{-2}) dose for deep isolation

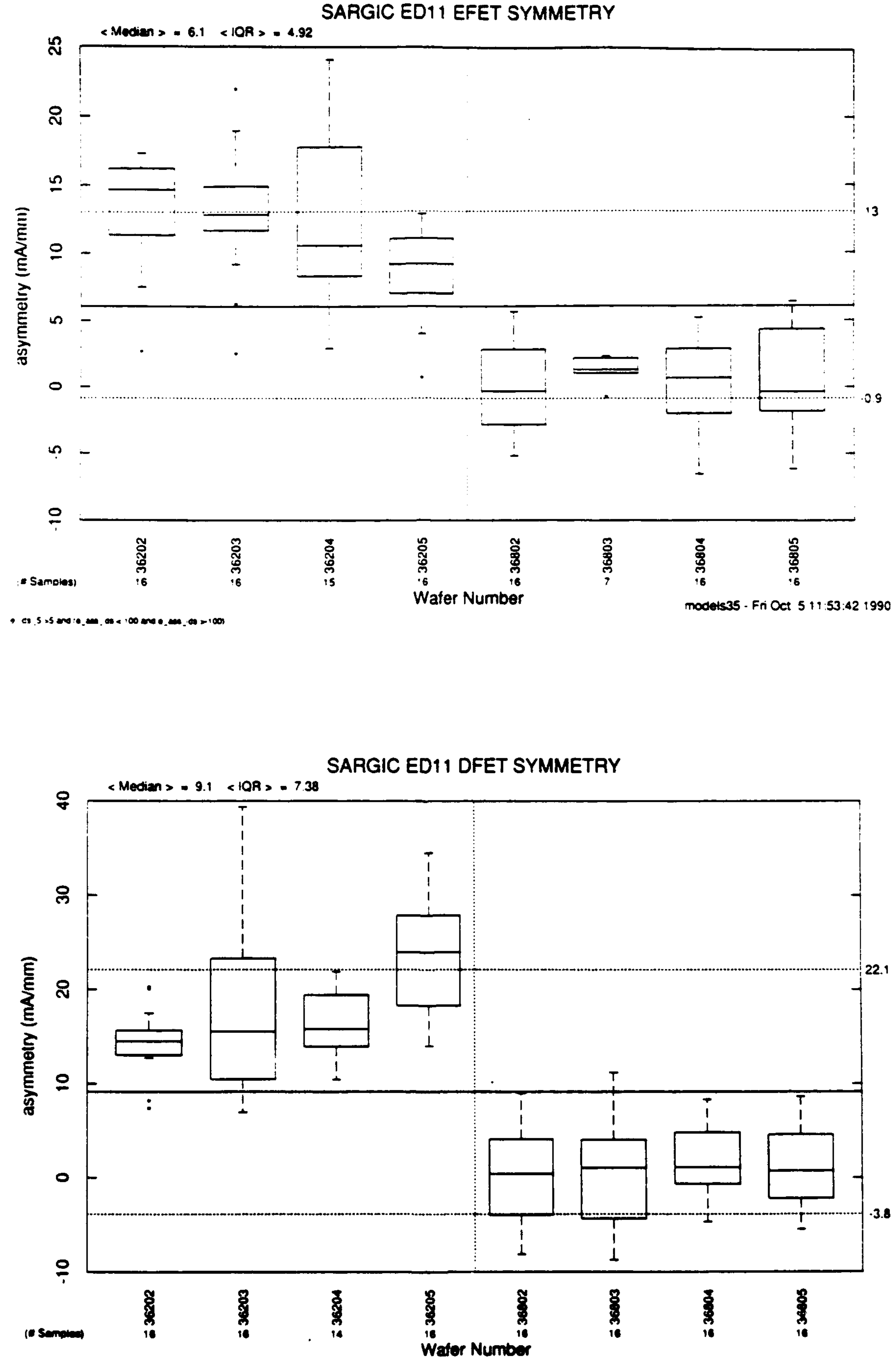


Figure 64 - EFET and DFET Symmetry

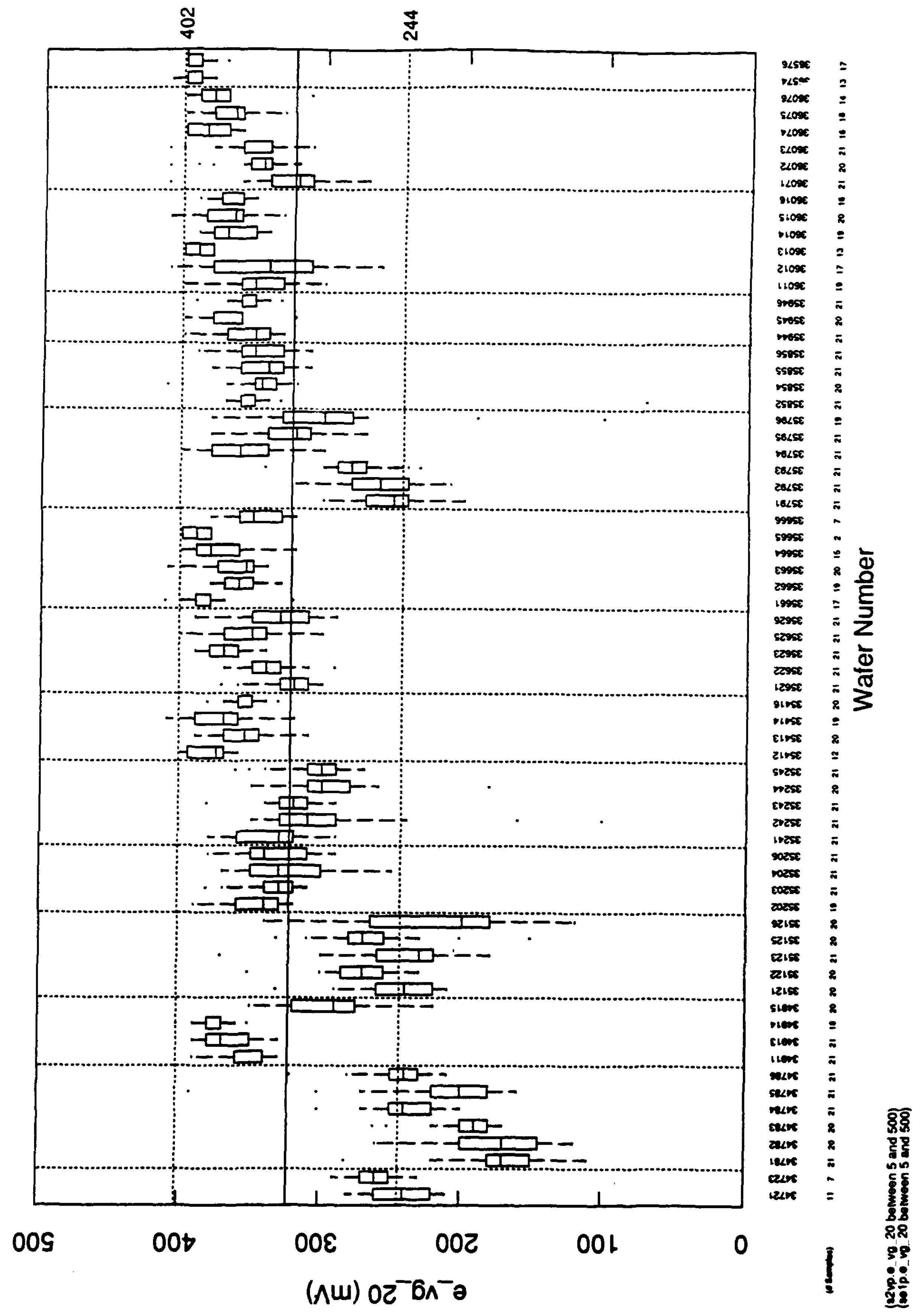


Figure 65 - EFET Threshold Voltages During the Period When Control Was Lost

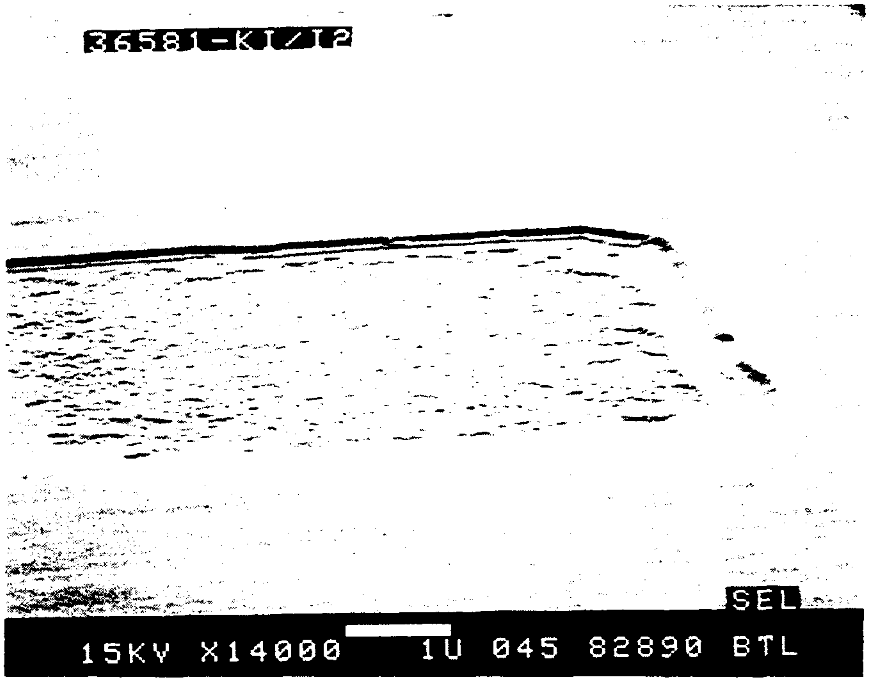

36581-KI/I2
SEL
15KV X14000 1U 045 82890 BTL

Figure 66a

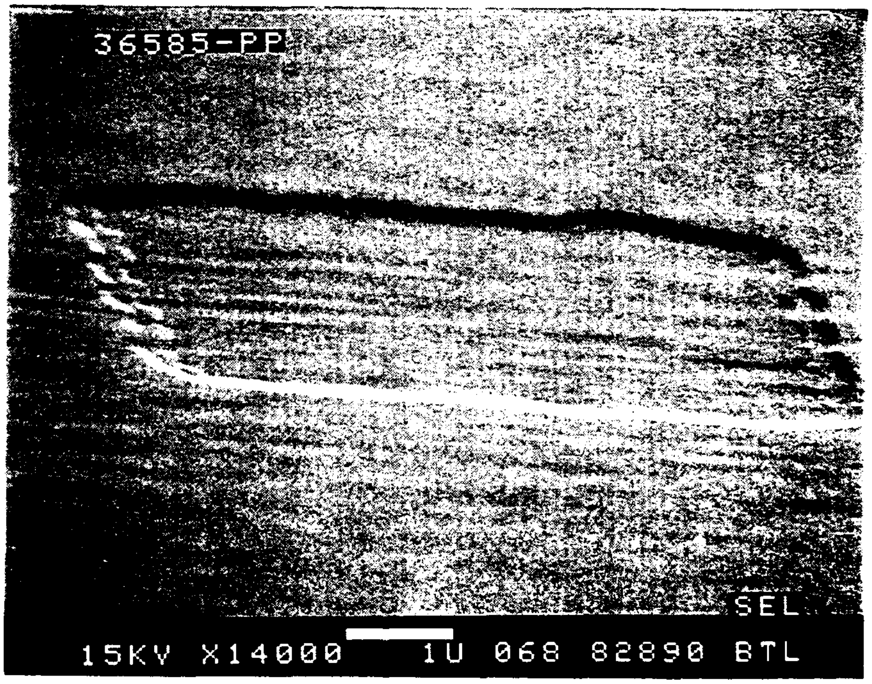

36585-PP
SEL
15KV X14000 1U 068 82890 BTL

Figure 66b

SEM Micrographs of (A) Rough and (B) Smooth EFET Tubs implant. The bilayer gate metal has lower gate metallization resistance, which may be beneficial and certainly won't be detrimental. An advantage of the SA isolation dose is that it prevents a rapid increase in leakage at higher voltages. Also, the SA implant provides the same reduction in sidegating as the S implant. On the other hand, the higher dose SA process causes ten times the leakage current (30-40 nA at 3V rather than 3-5 nA) for two 75µm ohmic pads separated by 2µm. Leakage currents of this magnitude are not important in our circuits, and further, this combination of geometry and bias are unlikely in actual circuits. An additional concern for the SA process was that the higher dose deep isolation implant must be done outside the cleanroom, with potential risk for increased particulate contamination. However, the implant machine is one which is used occasionally for other GaAs wafer fabrication and was used previously for Pilot Line fabrication without adverse consequences. Data on PT-2M memories for which the wafers were implanted both inside and outside the cleanroom indicate no yield differences. Thus, we concluded this was not a problem. Taking all these issues together, we chose to use the SARGIC-SA process for the final 16 lots of Pilot Line wafer fabrication. There are no series disadvantages, and the advantages are significant: all electrical data describing the new etch process came from SA wafers. Also, this was the appropriate time to consolidate two process variations into one.

The electrical data on the nine experimental lots split among the different etches support the results from our etching studies. Where the original process with KI/I_2 yielded EFET threshold voltages which are ~100 mV too positive, the wafers fabricated with either the PA or PP etches had threshold voltages and currents near target. Since use of the KI/I_2 etchant was unacceptable, the real question was whether to choose PA or PP. Of the nine split lots, each contained two or three wafers etched with PA and PP so that a total of 14 wafers of each etchant successfully reached BOTMET testing, the first electrical test in our process.

Table 35 shows the channel currents obtained from these wafers. It also shows the average intra-wafer variations of these currents (sigma). In all cases, the data are BOTMET data corrected to predict the values that would be obtained at final test.

Table 35 - Predicted Current at Final Test

	EFET Current (mA/mm)		DFET Current (mA/mm)	
	Mean	Sigma	Mean	Sigma
Target	55	–	85	–
PA	51.1	6.8	86.8	12.8
PP	56.7	9.0	86.9	16.1

On the basis of the data in the table, both etchants produce the same average value for DFET current, which is close to target. The intra-wafer standard deviation is slightly larger for wafers fabricated with the PP etch. For EFETs, PP seems to provide currents closer to target. A two-way analysis of variance shows that PP gives a current significantly different statistically from PA, but within-wafer and wafer-to-wafer variations overwhelm the effects of etchants.

In the end, we chose the PP etchant for the final Pilot Line lots. It is closer to target and is preferred from a manufacturing point of view. The use of the SARGIC-SA process also consolidates two of AT&T's processes into one. The final 16 wafer fab lots for this program were run in the SARGIC-SA process with the PP etchant. Figure 67 gives control charts showing the EFET and DFET currents for these lots. For the EFET, the average value is 61.3 mA/mm with a standard deviation of 15 mA/mm (the dotted lines in the graph show 3 standard deviation limits). The EFET target is 55 mA/mm. For the DFET, the average value is 84.5 mA/mm with a standard deviation of 21 mA/mm; the target is 85 mA/mm. Figure 68 shows the PCM yield for these wafers, using the criteria 40 < Ids (EFET) < 70 mA/mm, 65 < Ids (DFET) < 120 mA/mm, and 1000 < 4K via chain resistance < 20,000 Ω (see Section 2.22). Finally, Table 36 shows the fabrication yields of these 16 lots (8 lots of 4K SRAM II, 4 lots of 32-Bit Multipliers, and 4 lots of Cell Array Casino Test Chips).

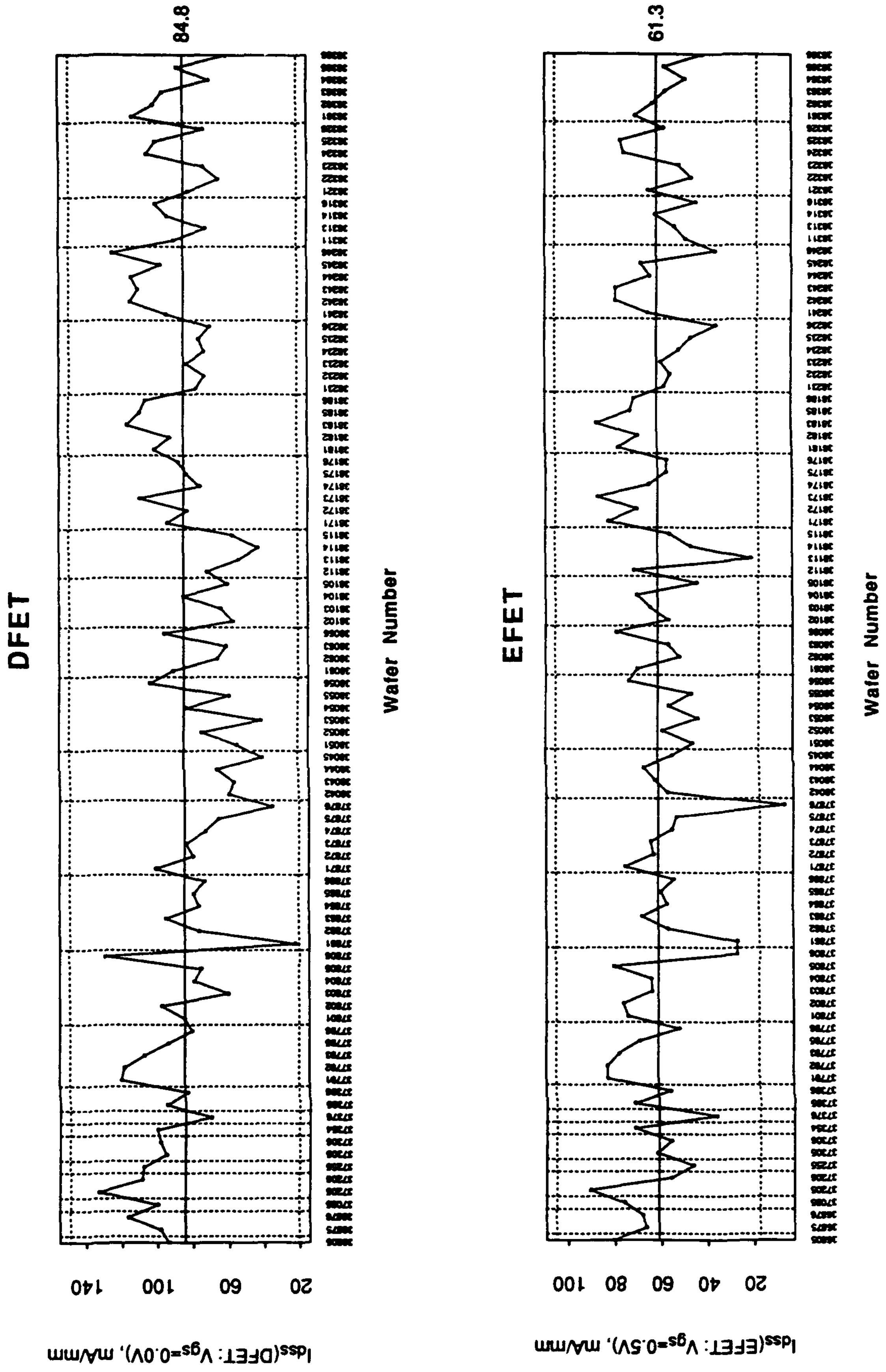


Figure 67 - DFET and EFET Average I_{dss} for All PP-Etched Lots

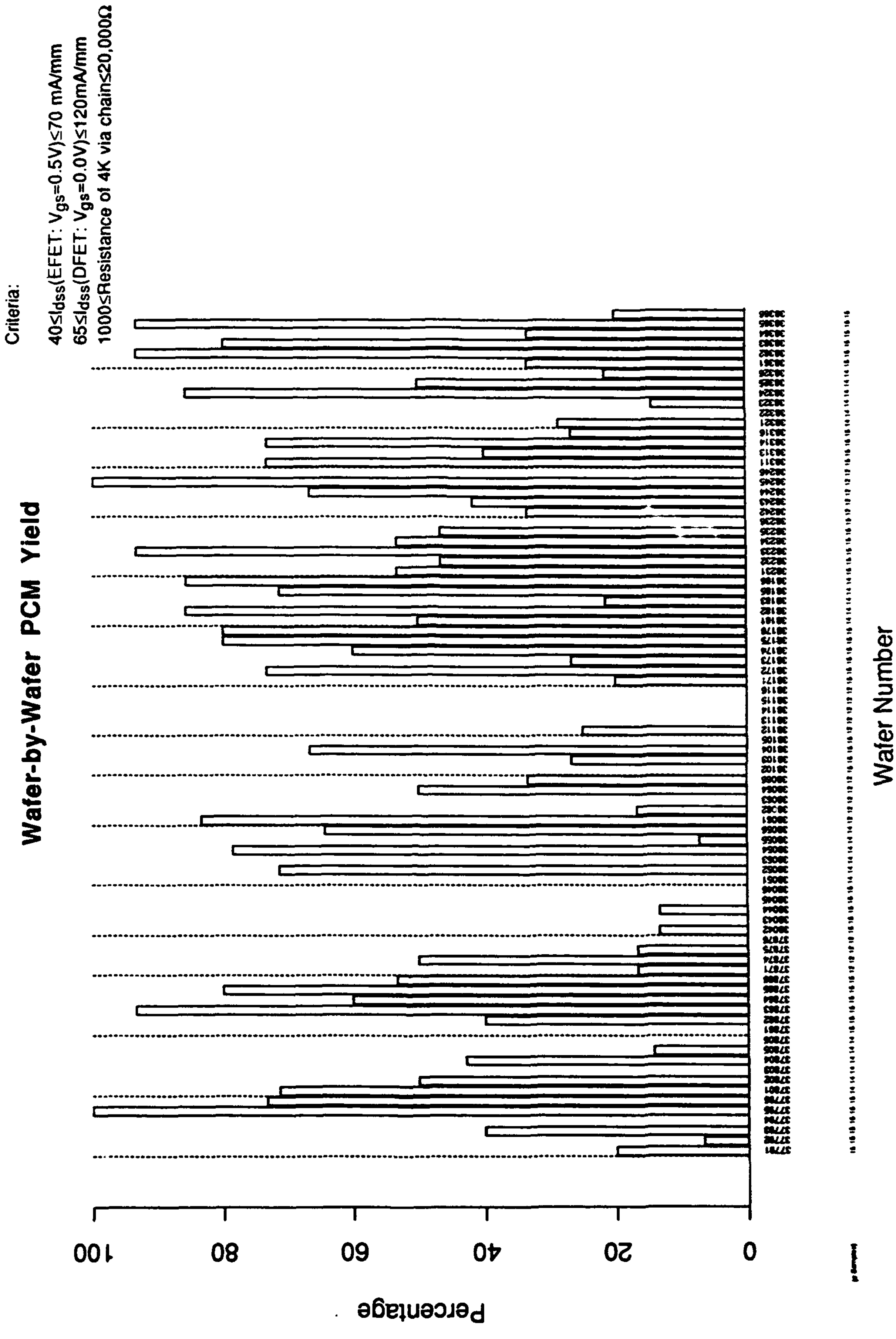


Figure 68 - Wafer-by-Wafer PCM Yield for Final 16 Lots

Table 36 - Fabrication Yields for Final 16 Lots

Wafers Started:	96	
Wafers Completed (Mechanically Good):	86	Yield: 90%
Total PCM Sites on Completed Wafers:	1204	
Good PCM sites on Completed Wafers:	491	Yield: 41%
Wafers Completed (Mechanically Good):	86	
PCM Good Wafers*:	44	Yield: 51%

*(at least 37.5% of PCM Sites are Good)

In addition to solving the EFET threshold problem, the PA and PP etches also solve a scaling problem that we had with EFETs. that is, with PA and PP etches, key EFET electrical parameters are essentially constant over a wide range of EFET widths. Scaling data for typical EFETs processed using the PP etch is shown in Table 37.

Table 37 - EFET Scaling Data

Wafer	Type	Width mm	Ids mA/mm	Vg(Ids=10mA/mm) mV	Vg(Ids=50mA/mm) mV	Vf(Ig=10mA/mm) mV
37306	e	.002	42.761	239	545	683
37306	e	.005	52.781	206	484	687
37306	e	.010	51.157	213	493	695
37306	e	.025	53.71	194	479	705
37306	e	.050	52.991	194	483	711
37306	e	.100	49.505	208	503	732
37306	e	.150	50.273	209	498	753
37306	e	.200	49.079	208	505	781

Ids (Vgs=0.5V, Vds=2.5V) is drain current.
Vg (Ids=10 or 50 mA/mm, Vds=2.5V) is gate voltage.
Vf (Ig=10 mA/mm, Vds=0V) is diode forward voltage.

It can be seen that devices from 5µm to 200µm scale very well. In contrast, with KI/I_2, there was a 100 mV shift in Vg when device width changed from 3µm to 50µm. In Table 37, the increase in Vf for large devices is due to gate metal resistance and is included in the device design model.

3.4 Shorts and Interconnect Yields (C. H. Tzinis, Y. C. Shih, A. V. Harton, and S. S. Patel)

Failure Analysis on PT-1

In the first 150 PT-1 wafers (7500 dice), 61.8% fell into three major failure categories: contact failure, shorts, and high power (see Table 38). Failure analysis revealed that most of the contact failures were due either to a photolithography error that affected only the first few processing lots or to experimental wafers having high resistance regions. We no longer see a significant number of contact failures.

Liquid crystals were used as temperature sensors to look for hot spots indicative of shorts or high power. We found hot spots near the EFETs of the column and row decoders, and not at crossovers of power buses as originally suspected. This ocurred in chips having low EFET thresholds so that the chips drew abnormally high power. Many of these chips also showed blowouts through the dielectric between two close-spaced metal runners. To prevent future blowouts, the design rules were revised. The remaining devices labeled as shorts and high power were really part of the same distribution, and they indicated how many devices had unacceptably low thresholds. Also, there was a discrepancy between actual and simulated power, so that the definition of high power needed to be revised based on experimental data.

Table 38 - Failures in PT-1 Memories

Failure Mode	**% of Tested Devices**	**Failure Mechanism**
Contact Failure	10.6	• Stepper programming error • Experimental wafers with different materials structure • Experimental wafers with high resistivity regions
Short	22.4	• Low V_{th} EFET • Blowouts due to metal levels proximity
High Power	28.8	• Low V_{th} EFET • Current limit inconsistent with power distribution

D_0 Model for Shorts

The wealth of data available from our memory circuits allowed us to do Y_0/D_0 calculations for shorts (liftoff metallization technology) and interconnects (via technology). The memory circuits also allowed us to directly compare the same design in two different sizes, 256 bits and 4096 bits. The total "crossover" area between top and bottom metal was extracted electronically from the mask design information. Table 39 summarizes the percentage of shorts, top-to-bottom metal crossover area and calculated D_0 assuming $Y_0 = 100\%$ (no parametric failure allowed in short testing).

Table 39 - Shorts in Memories

Code	Percentage Shorts (median)	Crossover Area (cm^2)	Crossover Area as a Percent of Chip Area	D_0 (cm^{-2})
PT-2M	2.85	1.8×10^{-3}	4.02	16.0
4K SRAM I	31.4	27.8×10^{-3}	9.88	14.0

The model used to calculate D_0 is

$$Y_D=Y_0\left(\frac{1-e^{-D_0\cdot A_a}}{D_0\cdot A_a}\right)^2$$

where A_a is the crossover area, and Y_D is the yield of the step (100% - 2.85% = 97.15% for PT-2M).

The derived D_0 is the defect density per crossover area and not per chip area. To get the contribution of shorts to the total defect density per unit chip area (D_0^T), we must multiply the D_0 for shorts times the crossover area as a fraction of chip area (e.g., $0.0988 \times 14.0cm^{-2} = 1.4cm^{-2}$). Since D_0 from PT-2M (110 wafers) and D0 from 4K SRAM I (34 wafers) are virtually the same, we believe the value is representative of our gold liftoff process.

Interconnect Yields

Our circuits contain large numbers of vias to connect one metal layer to another. For example, the 4K SRAM I has 223,805 vias, of which about half stand alone, and the other half are members of clusters that connect one bus to another. We can estimate circuit yield loss due to interconnects by constructing a model from via yields in our PCMs. Each PCM contains a via chain with 4300 1.5μm vias connecting various metal layers in a repeating pattern. To model the yield due to random via failures, we first discard wafers which have failed catastrophically (i.e., where more than half of the via chains are bad). Then, using data from the three PCM patterns that were used in Pilot Line III (s2v, s2vp, and se1p), we can make a rough estimate of via yield. We assume that a failed via chain contains only one bad via. Table 40 shows the estimate of yield.

Table 40 - Estimate of Via Yields

	s2v (1988)	s2vp (1989)	se1p (1990)
Total Via Chains	3870	2709	1772
Bad Via Chains = Number of Bad Vias	164	139	47
Probability of One Via Being Bad	9.9×10^{-6}	1.2×10^{-5}	6.2×10^{-6}
Probability of a Good Circuit with 100,000 Isolated Vias	0.37	0.30	0.54

The last line of the table shows the expected yield due to defective vias in 4K SRAM I, where there are about 100,000 isolated vias.

3.5 Advanced Technology (A. G. Baca, A. I. Faris, R. M. Havrilla, S. E. Lengle, D. D. Manchon, R. J. Niescier, S. F. Nygren, P. J. Robertson, R. Shul, M. Spector, P.F. Thompson, and S. B. Witmer)

The goal of this task was to investigate the manufacturing feasibility of an advanced technology that would operate at least twice as fast as the baseline technology's 200 MHz. We achieved this by 1) using an advanced implementation of the SFFL logic gate, and 2) developing an aluminum interconnect technology to allow decreasing the design rules to 1.5μm lines and spaces. We demonstrated our advanced technology by fabricating 8 x 8 multipliers based on the design used in PT-2L. The advanced technology multiplier successfully operated at 125 ps/gate delay, the equivalent of 400 MHz for 15-20 gate delays. Details are in Appendix D.

3.6 Circuit Packaging (K. J. Brady, R. S. Moyer, D. E. Miller, T. S. Freese, and R. B. Crispell)

Through a survey of commercially available high speed packages, we identified suitable packages for each of our circuits. Table 41 shows the choices and gives important characteristics. The survey itself in included as Appendix C of this report. In addition, the following paragraphs describe the characterization and fixturing issues that were considered after the survey was published.

Table 41 - DARPA Pilot Line III Package-Circuit Assignment Summary

Package Cost @ 100 Quantity	Pitch Z_0	Signal Leads Total Leads	Cavity Size Max Die Size	High Speed Fixture Available	Burn-in Sockets Available	Circuit Reticle Date	Die Size	Signal Count Total I/O
Tri-Quint PK-MLC-44S $65	.050" 50Ω	24 44	.130" SQ .090" SQ	Yes TriQuint	Yes JEDEC	PT-1 11/87	.060" SQ	24 44
						PT-2M 10/88	0.80" SQ	16 44
Interamics 64/88 $170	.020" 50Ω	64 88	.250" SQ .210" SQ	Yes In House	2/89 Azimuth Elect.	PT-2L 6/88	.204" SQ	64 88
						4K SRAM 9/89	.216" SQ	~36
						1K Cell Array 4/89	.212" SQ	64 88
TriQuint PK-MLC 196-S $180	.025" 50Ω	128 196	.430" SQ .390" SQ	Yes TriQuint	6/89 Yes	Transversal Filter Chip 9/89	.360" SQ	105 173
						Custom ALU 3/89	.292" SQ	120 168
						Standard Cell ALU 8/89	.292" SQ	120 168
						32-Bit Floating Point Multiplier 12/89	.360"x.380"	110 160
NTK/256 pin $50	.020" 58-60Ω	224 256	.560" SQ .520" SQ	No	Yes Yamaichi	Cell Array Casino Test Chip 12/89	.462" SQ	172 236

PT-2M, PT-1: TriQuint MLC-44 Package

A difficulty with deformed package leads was encountered during PT-2L testing. The package leads are very fine pitch and easily deformed. Any amount of deformation results in misalignments between test fixture and package, and difficulty in maintaining good connections. A plastic carrier, developed in anticipation of a need for burn-in sockets, was ordered. The plastic carrier protects the leads during shipping and can be used to straighten package leads.

For the completion of the PT-2M reliability study, we qualified a parallel seam seal hermetic process and fabricated hermetically sealed 44-pin packages. In order to seam seal, a modification of the TriQuint PK-MLC-44-S package was required. This involved adding a Kovar seal ring to the package (see Figure 69). Twelve electrically good devices were selected and assembled in hermetic packages; one failed to seal properly and was removed from further study. Of the remaining 11, no gross failures were detected at testing. We measured memory access time in both pipeline (Tap) and ripple (Tar) modes before and after sealing. The differences between the "before" and "after" measurements are plotted in Figure 70. The reproducibility of each measurements is ±0.1 ns, and the no differences exceed ±0.3 ns. Accordingly, we consider the hermetic sealing process to be qualified. A sealing yield of 84% was achieved on 140 devices assembled for High Temperature Operating Bias.

The MLC-44 package and test fixture combination have been characterized by measuring two-port scattering parameters using an HP 8510-B network analyzer. The data listed below shows that this fixture-package combination will perform well with respect to the 1.3 GHz bandwidth requirements of the circuits.

Insertion Loss	Return Loss	Adjacent Line Isolation
1.0 dB @ 1.5 GHz	20 dB @ 2 GHz	-20 dB @ 1.5 GHz

PT-2L, 1K Cell Array, and 4K SRAM: Interamics 64/88 Package

Difficulties were encountered with loading packages into test fixtures and maintaining alignment with all of the package leads. A new package clamping mechanism was designed and fabricated by AT&T, eliminating all of the problems that we were experiencing. A schematic view of the design is shown in Figure 71. This approach was applied to TriQuint 196 lead package testing as well as to Interamics 64/88 package testing. Additionally, the design was communicated to TriQuint so they could incorporate it into their test fixtures if they wish to do so.

Two port scattering parameters of the Interamics package, AT&T test fixture, and cable interfaces were measured using an HP 8510-B network analyzer. In order to interface the network analyzer with the test fixture, an SMA to Chabin cable adapter was fabricated. This adapter had a VSWR of 1.8 which masked the performance of the fixture and package. The large insertion loss and return loss reported here would be improved if the test fixture could be accessed directly with an SMA connector. Listed below are the measured results of the entire system under test which include the effect of the adapter.

Insertion Loss	Return Loss	Adjacent Line Isolation
1 dB @ 1 GHz	15 dB @ 1 GHz	-22 dB @ 1 GHz
3 dB @ 1.5 GHz		
7 dB @ 2 GHz	10 dB @ 2 GHz	-15 dB @ 2 GHz

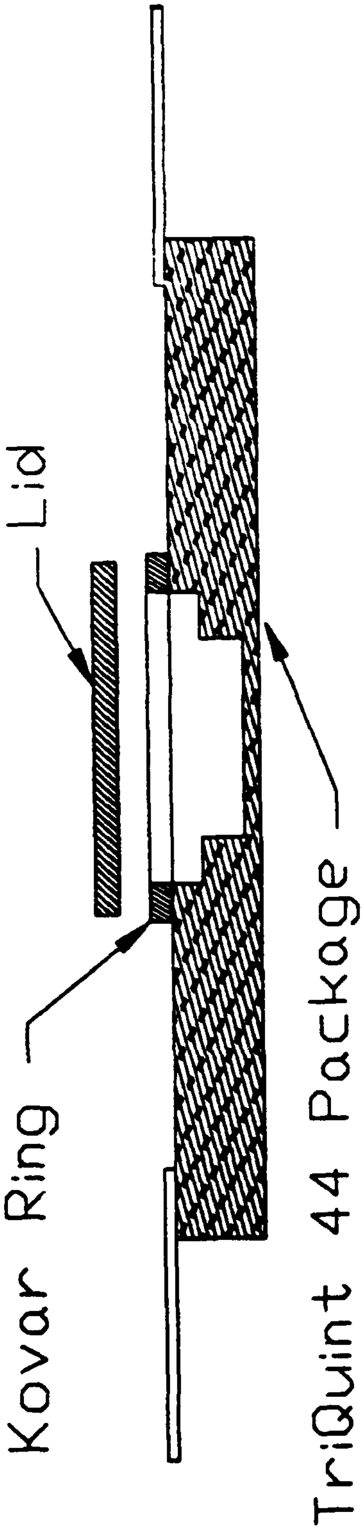
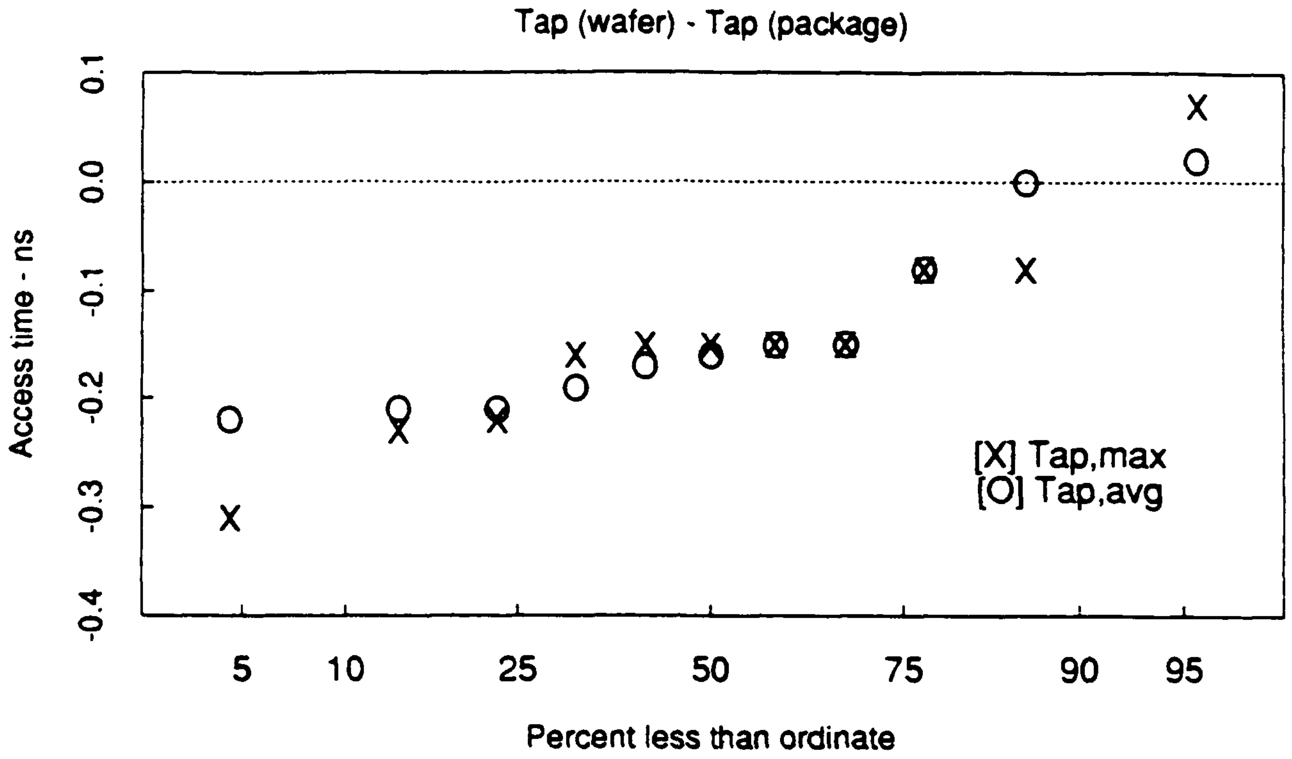

Lid
Kovar Ring
TriQuint 44 Package

Figure 69 - Cross-Section of TriQuint 44 Package, Showing Seal Ring



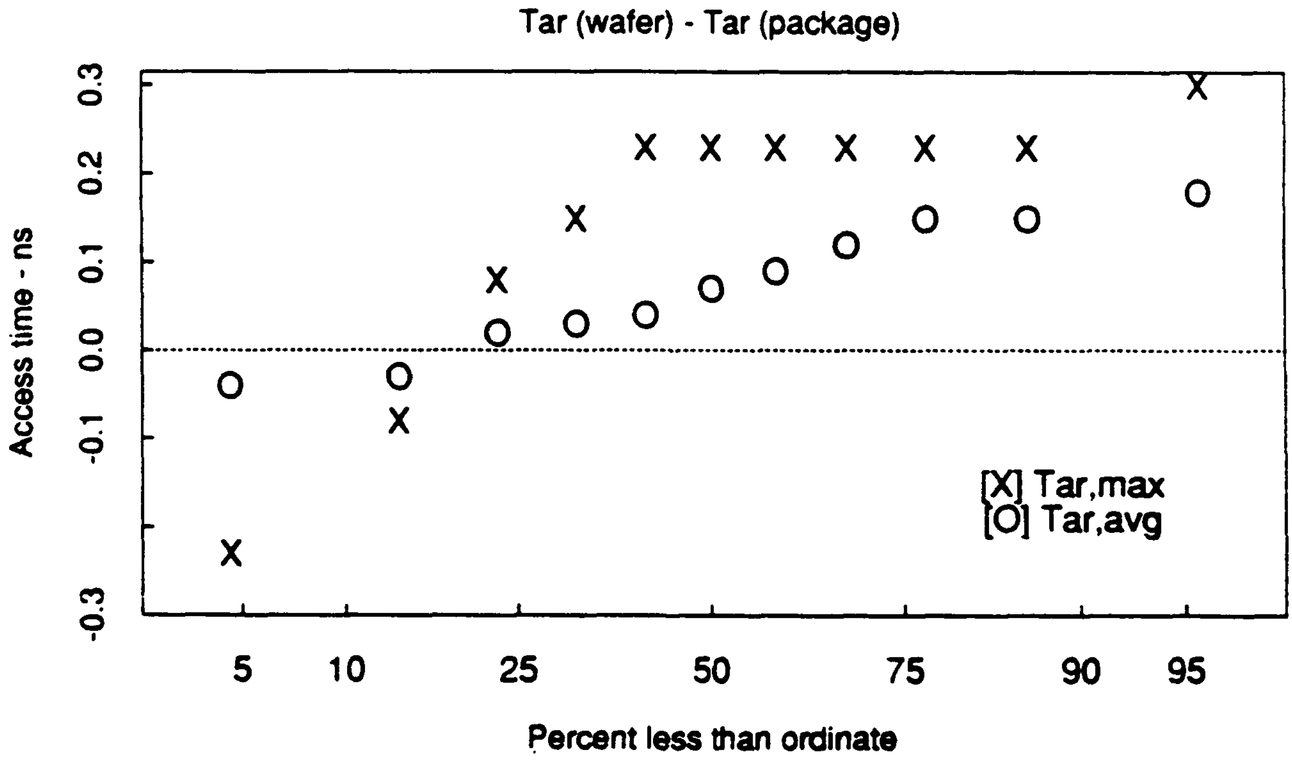


Figure 70 - Change in PT-2M Memory Access Time During Hermetic Sealing

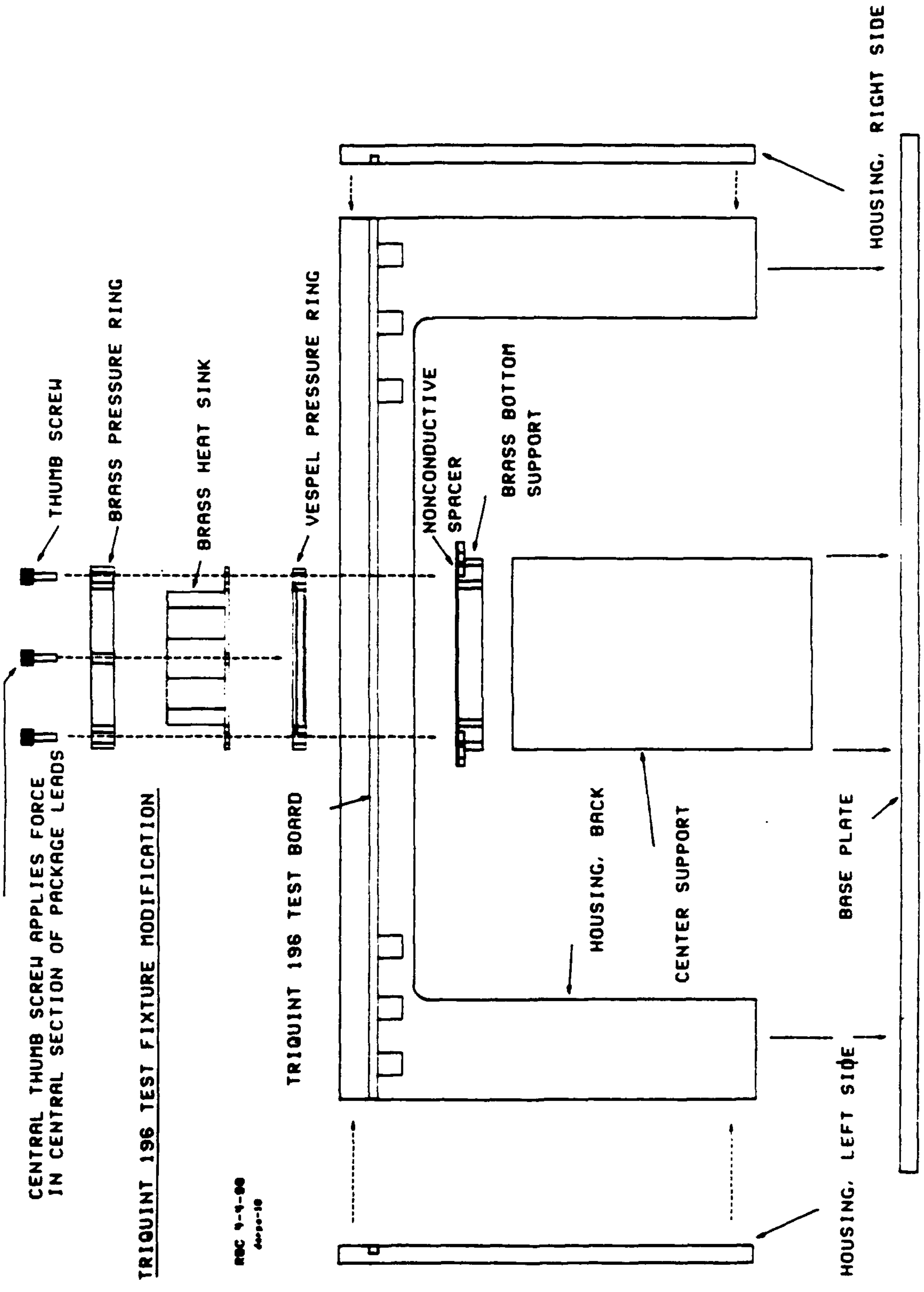

CENTRAL THUMB SCREW APPLIES FORCE
IN CENTRAL SECTION OF PACKAGE LEADS
TRIQUINT 196 TEST FIXTURE MODIFICATION
RBC 9-9-88
THUMB SCREW
BRASS PRESSURE RING
BRASS HEAT SINK
VESPEL PRESSURE RING
TRIQUINT 196 TEST BOARD
NONCONDUCTIVE
SPACER
BRASS BOTTOM
SUPPORT
HOUSING, BACK
CENTER SUPPORT
BASE PLATE
HOUSING, LEFT SIDE
HOUSING, RIGHT SIDE

Figure 71 - Clamping Mechanism for TriQuint 196 Package Testing

Transversal Filter Chip, Custom and Standard Cell ALUs, 32-Bit Multiplier: TriQuint MLC-196 Package

The MLC-196 is a new package developed for us by TriQuint after the Industry Survey was prepared. Five prototype packages and a high speed test fixture were delivered to AT&T as promised in early March, 1989. This package has two power busses, multiple ground planes and 128 50-ohm signal lines. The maximum die size is recommended to be 0.390 inches (9.75 mm) square. TriQuint designed and provided a lead trim and form tool for this package. Low frequency burn-in type sockets were tooled through TriQuint as well. The package is similar to the MLC-44 in concept and is designed to handle clock rates up to 3.5 GHz and edge rates less than 125 ps.

Standard Cell and Cell Array Casino Test Chips: AT&T-NTK 256-pin Package

To evaluate automatic and manual wire bonding for chips with a large number of pads, we bonded several mechanical samples with each method. The mechanical samples had 0.004 inch pads on a 0.006 inch pitch, the same as the Cell Array Casino Test chip and the 32-Bit Multiplier. We could achieve a 100% yield with manual bonding, but only 89% with automatic bonding. There were two primary failure mechanisms with automatic wedge bonding: 1) shorts when the tail of one bond wire touched another pad, and 2) wires that didn't stick due to attempts to bond them off-center to avoid shorts. The major problem with automatic bonding is that the package is not customized to the chip. In manual bonding, the operator can tailor the path of each wire. With automatic bonding, the different wire angles, variable wire length, and small spacing created problems. If these chips were to be packaged in high volume, we could undoubtedly solve these problems by designing custom packages.

4.0 RADIATION HARDNESS AND RELIABILITY

4.1 Radiation Hardness (S. B. Witmer, M. Spector, S. D. F. Jones, and R. L. Remke)

We tested radiation hardness in three steps. First, we used PT-0 HFETs to characterize the basic features of the technology. Then we used PT-1 to examine radiation effects on ring oscillators, early memories, and more HFETs. Finally, we tested the PT-2M memory and the Custom ALU to characterize our primary circuits.

PT-0

Total dose radiation testing was performed on PT-0 HFETs and ring oscillators. The DC characteristics were measured before and after exposure to 1×10^8 rad (GaAs) of gamma radiation from a Co^{60} source. The HFETs were tested with and without bias. After 1×10^8 rad (GaAs), no measurable change in the DC characteristics was observed for biased or unbiased HFETs. Figure 72 shows the drain current both before and after irradiation with 0.7V gate bias.

Ring oscillator AC characteristics were also measured before and after irradiation. After 1×10^8 rad (GaAs), the average drain bias current decreased by 6.8% and the frequency decreased by 4.2%.

The transient ionizing dose response of HFETs was measured using the LINAC at the Naval Research Laboratory. HFETs were evaluated both with and without an insulating layer between the metallization paths (including the bonding paths) and the GaAs. During the radiation pulse, the response of the HFETs without an insulating layer was dominated by substrate leakage currents between metallization areas of different potentials. HFETs with an insulating layer showed a transient leakage current at 10^9 rad (GaAs)/sec., but a photovoltaic effect dominated at higher dose rates. At does rates from 1×10^9 to 1.3×10^{11} rad (GaAs)/sec., the magnitude of the radiation induced change in the FET characteristics was less for the FETs with an insulating layer than those without an insulating layer. For both types of FETs, their electrical characteristics returned to their initial values after the radiation pulse ended.

Later, HFETs were irradiated with 20 nsec. pulses of 40MeV electrons. Positive voltage transients were measured at the drain node and negative voltage transients were measured at the gate node of the HFETs during the irradiation (Figure 73). These results indicate that the photocurrent flows into the gate and out the source and drain. The magnitude of the transient voltages strongly increased with dose rate. The transient gate and drain currents are reduced slightly with decreasing gate voltage and increasing drain voltage. The transient voltages observed during irradiation are believed to result from the collection of electron-hole pairs within the depletion regions of the junctions (photovoltaic effect). The photocurrent generated in the heterojunction depletion region dominates over the photocurrent generated in the Schottky barrier depletion region and hence the observed result of current flow into the gate of the HFET. The substrate currents, which dominated earlier measurements, were reduced by depositing a silicon nitride layer under the metallization and by growing a superlattice structure in the GaAs. The reduction in substrate current made it possible to characterize the photovoltaic effect.

Single event upset testing was performed on PT-0 HFETs. Alpha particles emitted from 1μ Ci of Am^{241} were used to irradiate the HFETs. Negative voltage transients were measured at the drain node during the alpha particle irradiation using the experimental setup shown in Figure 74. The transient response for HFETs was much smaller than that observed for MESFETs as shown in Figure 75. This result suggests that memories made with HFETs with be more immune to single event upset than those made with MESFETs.

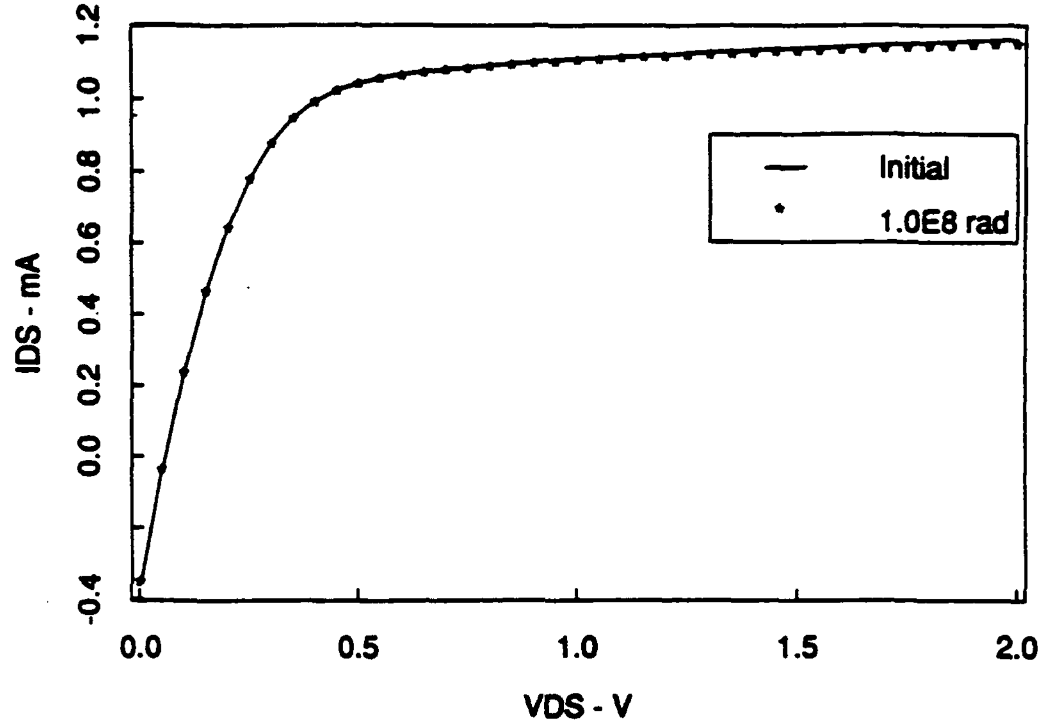


Figure 72 - PT-0 Wafer 3223 FET Drain Characteristics as a Function of Total Ionizing Dose (Biased, $V_G = 0.7V$)

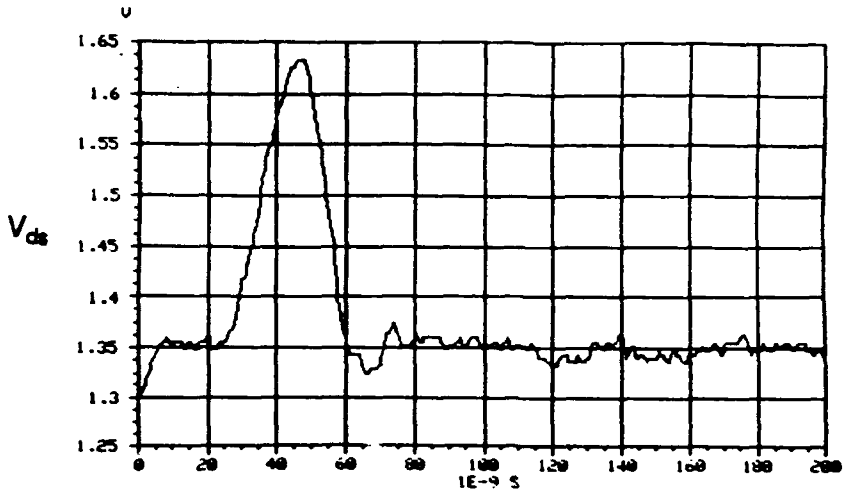


Figure 73a - PT-0 Wafer 3223 FET Drain Voltage (V_{ds}) Response to 5 x 10^{10} rad (GaAs)/s
(V_{DD} = 1.5V, V_{GG} = 0.6V)

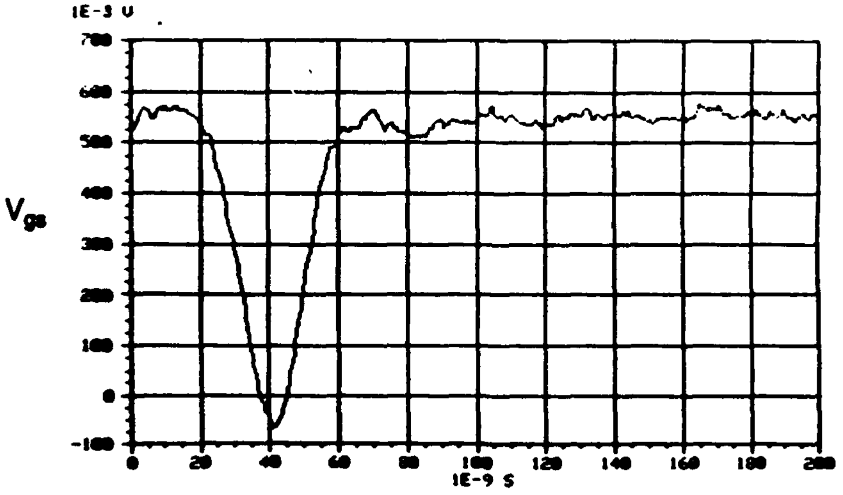


Figure 73b - PT-0 Wafer 3223 FET Gate Voltage (V_{gs}) Response to 5 x 10^{10} rad (GaAs)/s
(V_{DD} = 1.5V, V_{GG} = 0.6V)

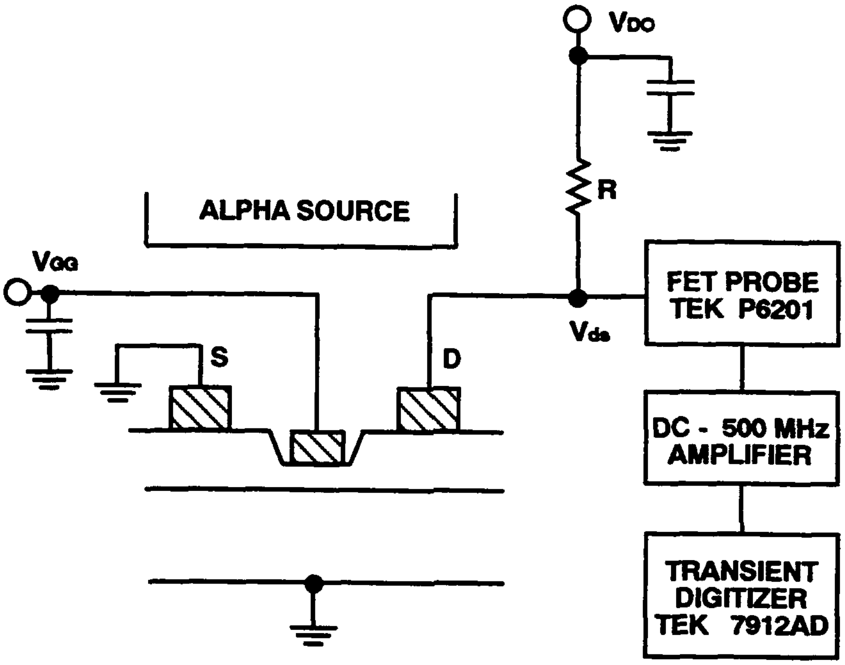

VDO
R
ALPHA SOURCE
VGG
S
D
Vds
FET PROBE TEK P6201
DC - 500 MHz AMPLIFIER
TRANSIENT DIGITIZER TEK 7912AD

Figure 74 - Experimental Setup for Alpha Particle Irradiation Experiments

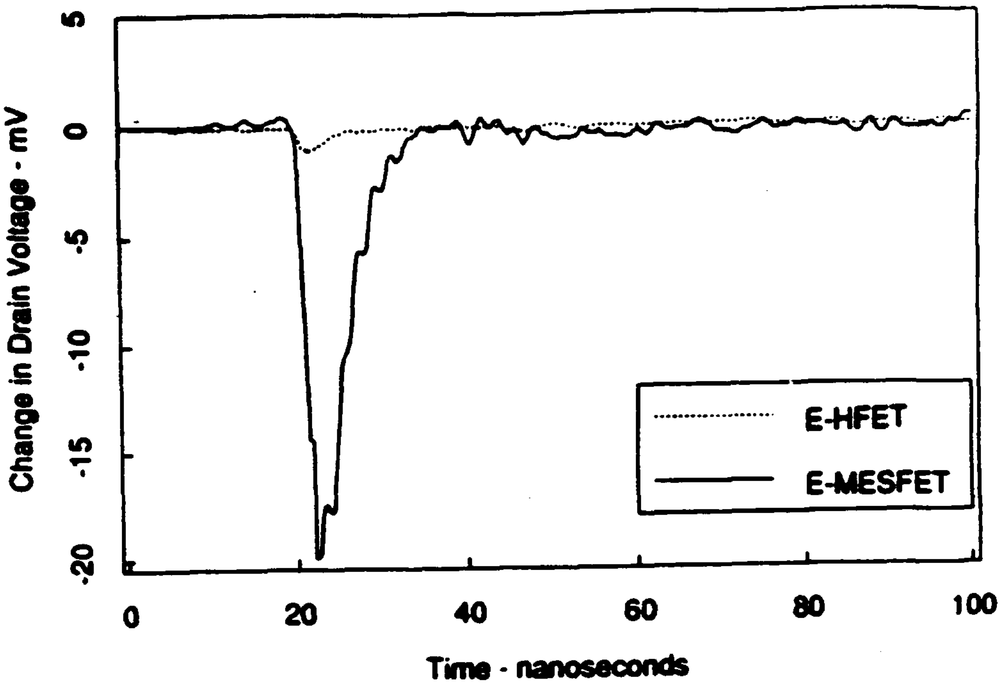


Figure 75 - The Drain Voltage Response of an E-MESFET and an E-HFET to an Alpha Particle. V_{GG} = -0.5V, V_{DD} = 1.5V, Gate Length = 1.0μm, Gate Width = 17.5μm

PT-1

Total dose radiation experiments were conducted on PT-1 HFETs, ring oscillators, and 256 bit SRAMs. They were exposed to gamma radiation from a Co^{60} source up to a dose of $6x10^8$ rad (GaAs). The SRAMs were irradiated with and without bias and all devices were periodically tested, visually inspected, and photographed under high magnification. After $1x10^8$ rad (GaAs), all devices showed very small changes in electrical characteristics (~5%). No significant differences were observed between the biased and unbiased SRAMs.

Transient ionizing dose testing was performed on HFETs, ring oscillators, and SRAMs. Transient dose testing of HFETs showed a photovoltaic signal with the source and drain nodes grounded and no bias applied. Testing of ring oscillators and inverters showed that they recovered promptly after the radiation pulse at dose rates less than $1x10^{10}$ rad (GaAs)/sec. The SRAMs tested had low noise margins which contributed to the large number of bit errors (5-10%) at dose rates less than $1x10^9$ rad (GaAs)/sec. and also to the row and column failures. By masking out the marginal cells, a threshold of $1x10^9$ to $2x10^9$ rad (GaAs)/sec. was observed in two devices. The transient response of the SRAM was also measured by connecting the DATAOUT line to a transient digitizer and placing the memory in the read mode. These measurements show that some cells are not toggled by dose rates as high as $1x10^{10}$ rad (GaAs)/sec.

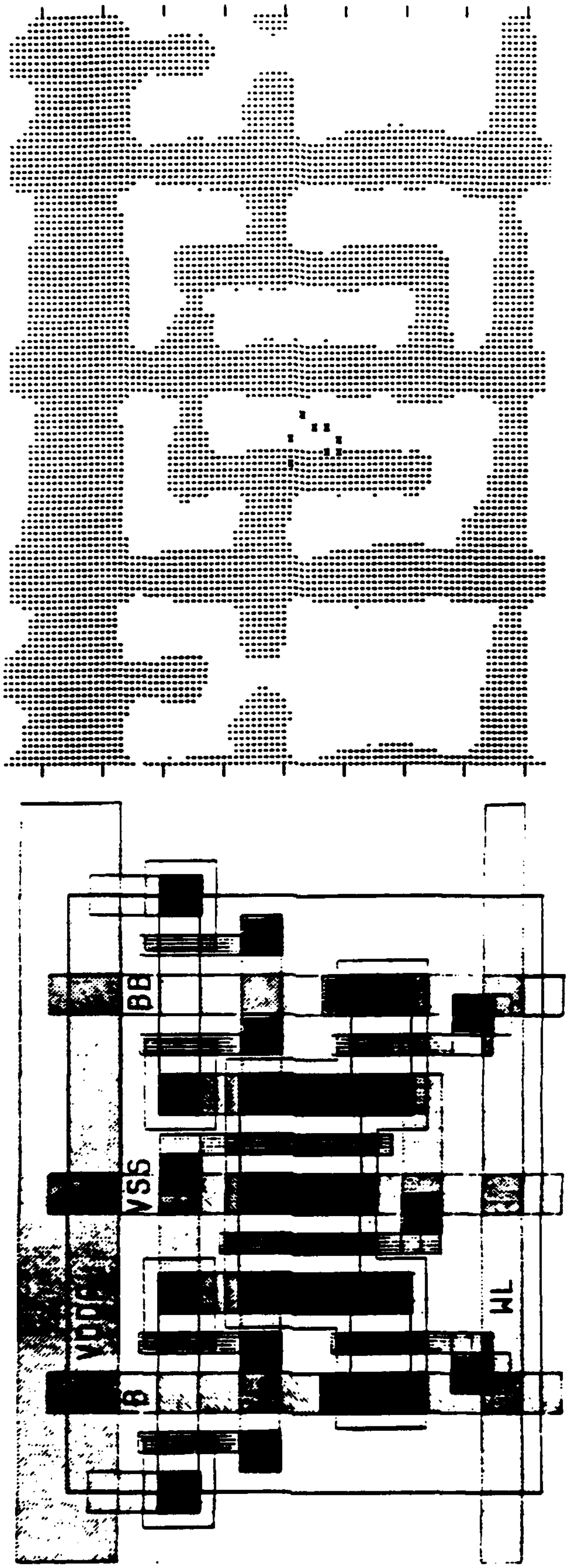
Single Event Upset (SEU) measurements were made on the Standard and Rad-Hard memory cells (256 bit SRAM) using the electron beam source at NOSC (Larry Flesner). These measurements showed an error rate of about $5x10^{-8}$ errors/bit day for the Rad Hard cell and about $2x10^{-7}$ errors/bit day for the Standard cell. The testing also showed that the most sensitive area for both types of cells was the area between the drain and source of the off driver FET of the memory cell (see Figure 76). Comparing the experimentally observed error rates with analytical expressions for the error rate suggests that the HFET collection depth is less than previously reported values for GaAs devices. This reduced collection depth is believed to be due to the superlattice below the HFET.

256 Bit PT-2M SRAM

Total Ionizing Dose (Gamma): The total ionizing dose hardness of the SRAM was evaluated to $5x10^8$ Rad (GaAs) using a Co^{60} source. The following circuit parameters were monitored after each irradiation: Access time, output voltage high, output voltage low, and supply currents. Less than 10% degradation was observed in the monitored circuit parameters at $1x10^8$ Rad (GaAs). The SRAMs continued to operate at $5x10^8$ Rad (GaAs). Figure 77 shows the percent decrease in supply current (I_{DD}/I_{DD0}) versus total dose and Figure 78 shows the percent increase in the access time. The decrease in IDD and increase in access time are consistent with measurements on discrete HFETs which showed that the radiation produces an increase in the HFET threshold voltage. The increase in DFET threshold voltage reduces the on state inverter bias currents in the memory array and peripheral circuitry, and increases inverter propagation delay. The vertical line is $1x10^8$ Rad (GaAs) in Figures 77 and 78.

Transient Ionizing Dose: Transient ionizing dose testing was performed on the PT-2M SRAM at the Naval Research Laboratory using 25ns pulsed ionizing radiation. Transient ionizing dose measurements were made on standard and radiation-hardened (rad hard) PT-2M SRAM testers. The best upset threshold obtained on the rad-hard and standard designs was $1x10^8$ Rad (GaAs)/sec. and $5x10^9$ Rad (GaAs)/sec. respectively (see Figure 79). The average value of upset threshold for all SRAMS tested is approximately $2x10^9$ Rad (GaAs)/sec. with a minimal difference between the rad-hard and standard design. In all cases the access row (one row always accessed by design) is more susceptible to upset than unaccessed rows.

Single Event Upset Testing: The 256 bit PT-2M SRAM was tested for single event upsets at Brookhaven National Laboratory. The SRAMS were irradiated with the following ions: He, Li, F, I, and Ni, which produced linear energy transfers in GaAs ranging from $0.1 MeV{*}cm^2/mg$ to



Upset pattern for Non-Rad-Hard memory (effective LET = 8.4 MeV/mg/cm^2, state "1")

Figure 76 - Upset Pattern for Standard Memory (Effective LET = 8.4 MeV/mg/cm^2, state "1")

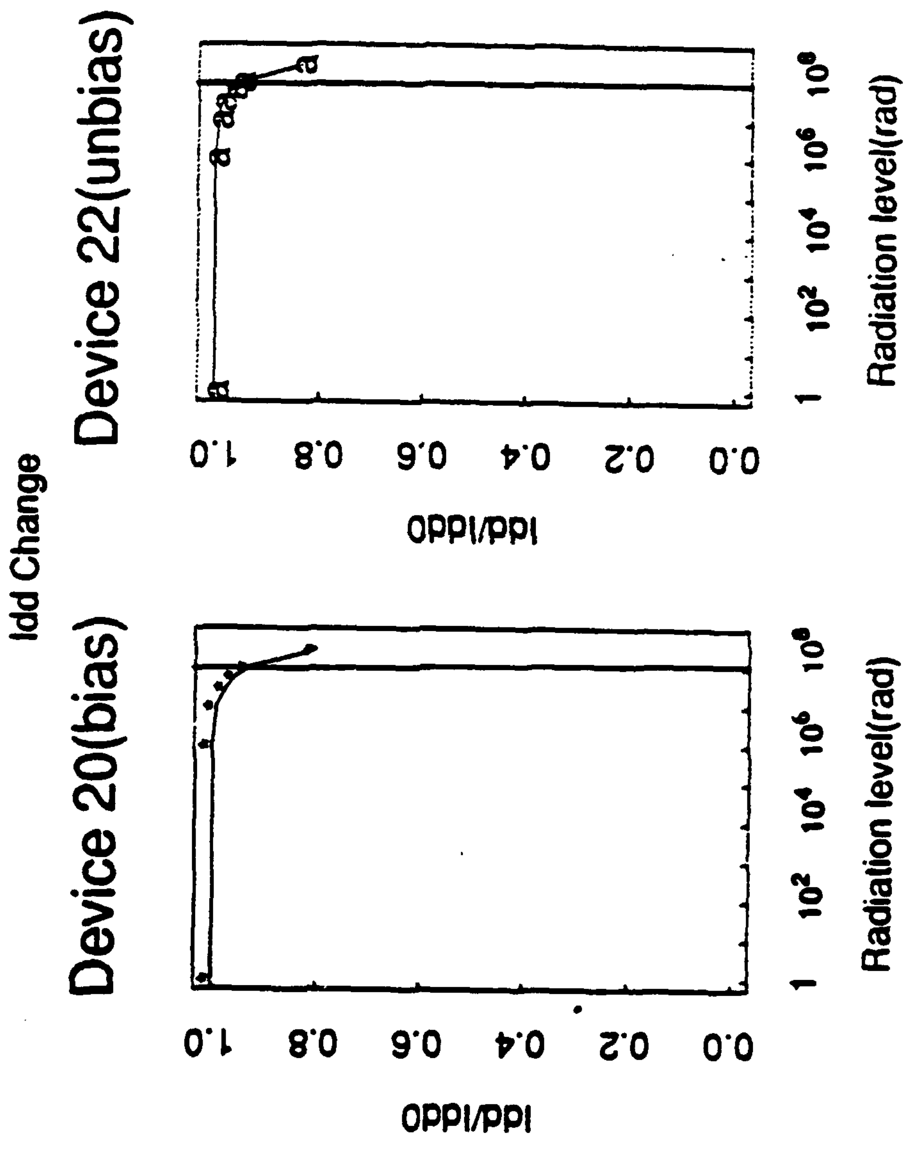


Figure 77 - Effect of Total Dose Irradiation on PT-2M Memory Power Supply Current

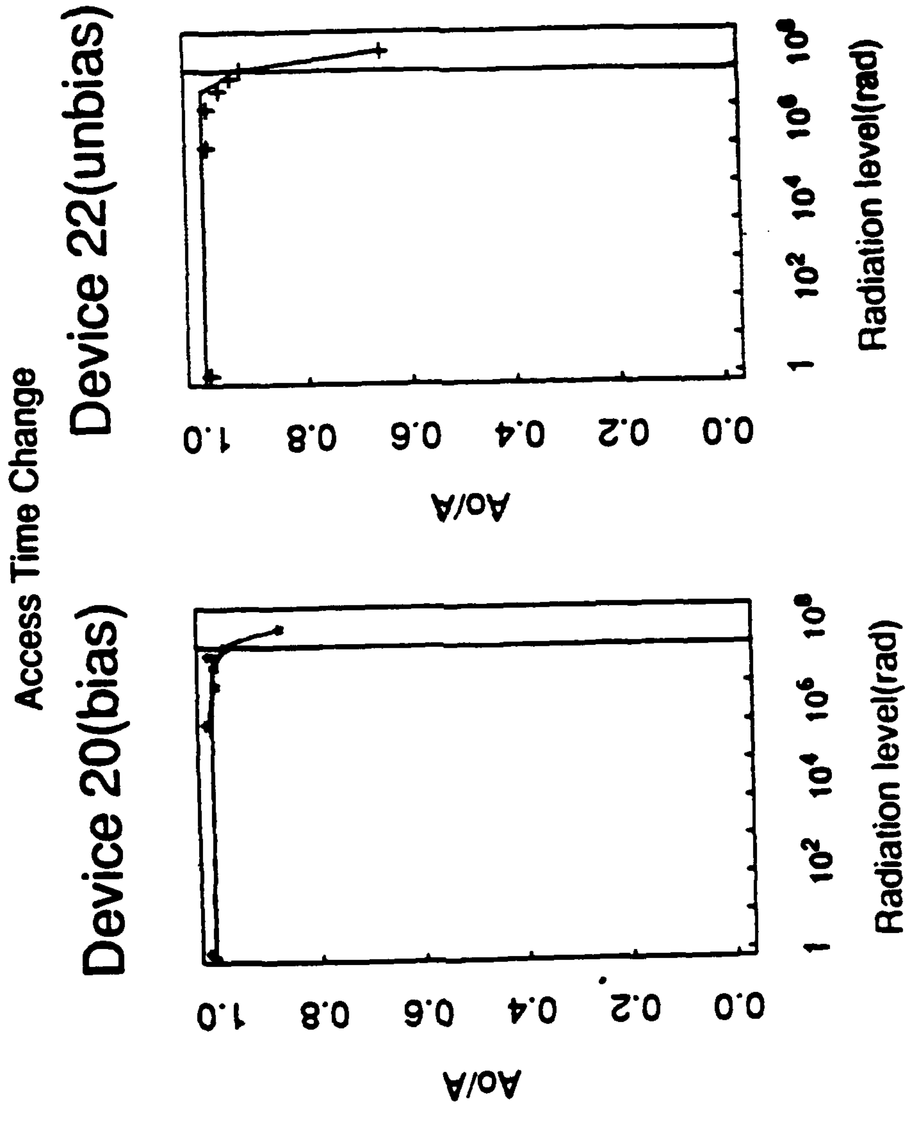
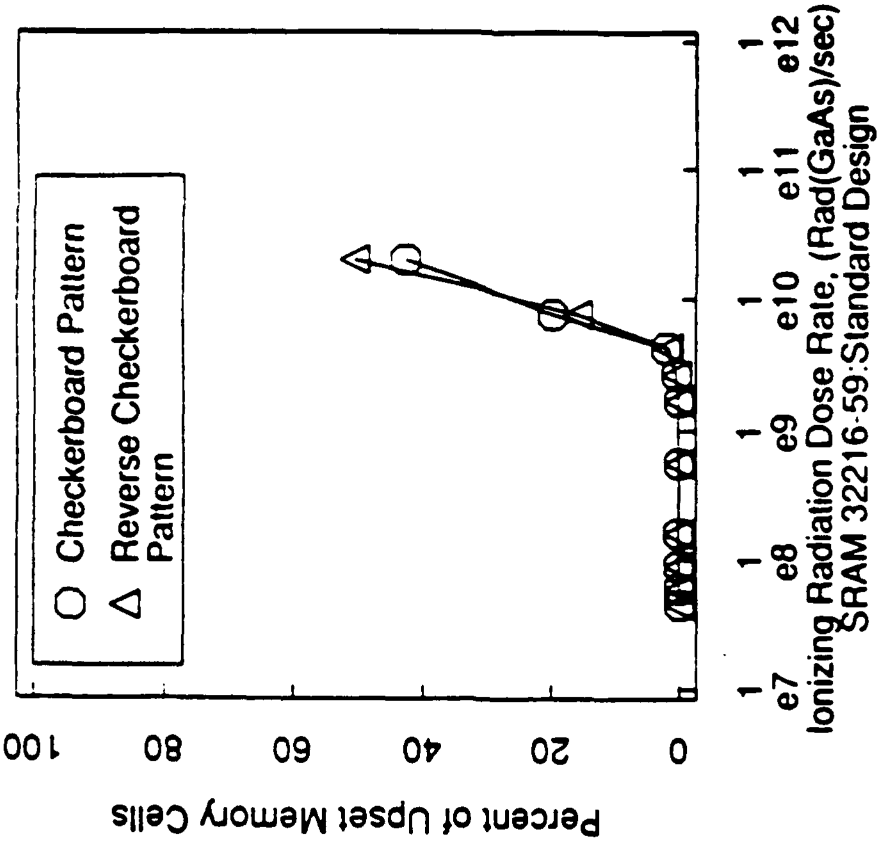


Figure 78 - Effect of Total Dose Irradiation on PT-2M Memory Access Time



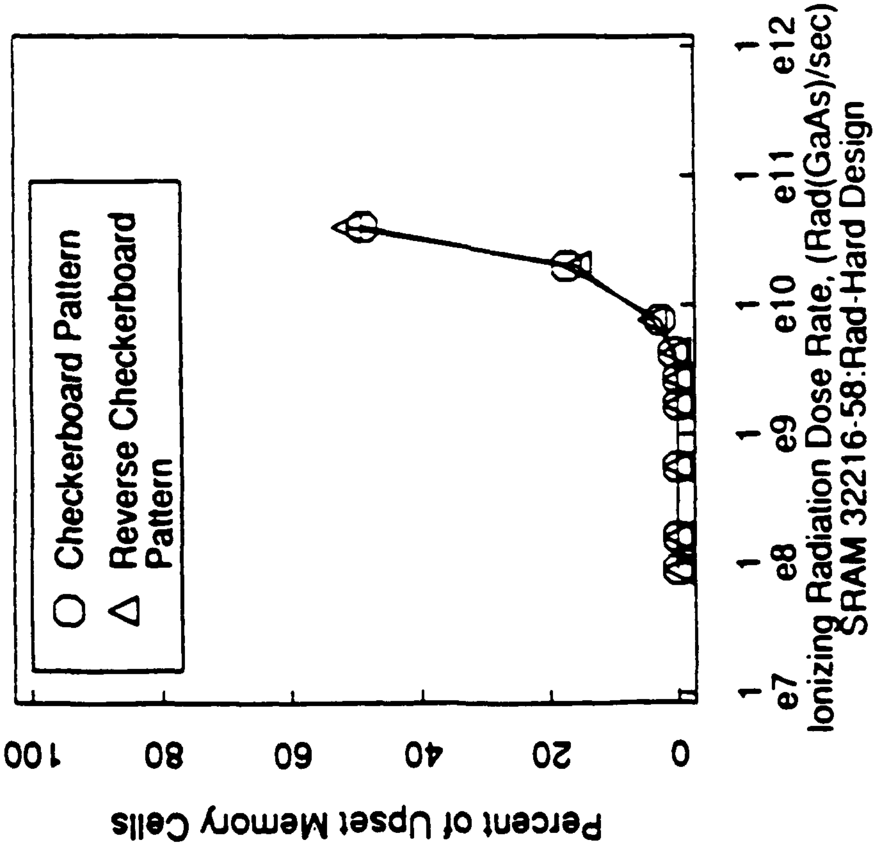


Figure 79 - Effect of Total Dose Irradiation on PT-2M Memory Stability

44MeV*cm^2/mg. Both static testing, where the SRAM is read only once after the radiation exposure, and dynamic testing, where the SRAM is read and corrected continuously during the exposure, were used to evaluate the SRAMS. In both the static and dynamic test modes, the LET threshold was about 0.2MeV*cm^2/mg and 0.35MeV*cm^2/mg for the standard and rad-hard designs, respectively. At a LET value of 44MeV*cm^2/mg using Ni, the upset cross-sections per cell were approximately 2.25x10^{-6}cm^2 and 1.22x10^{-6}cm^2 for the standard and rad-hard SRAMs, respectively (see Figure 80). Row failures (multiple bits in a row fail simultaneously) occurred frequently during the dynamic and static testing, when the memory was irradiated with Ni (LET=44MeV*cm^2/mg at 30° tilt), indicating that multiple upsets occur from one ion hit. Using the approximation of cosmic ray upset rates outside the earth's geomagnetic cut-off given by Peterson, Langworthy and Diehl, the upset rate can be approximated as:

$$R=5\times10^{-10}*\left(\frac{\text{(upset cross section (25\% below max))}}{\text{(LET-threshold)}^2}\right)$$

with R equal to 1.2x10^{-3} and 6.8x10^{-3} for the rad-hard and standard SRAMs respectively.

Custom ALU

Total Ionizing Dose (Gamma): The total ionizing dose hardness of the ALU was evaluated to 1x10^8 Rad(GaAs)/sec. using a Co60 source. Four circuits from four different lots were tested before irradiation, and after 1x10^7, 3x107, and 1x10^8 Rad(GaAs)/sec. Shmoo plots of five circuit parameters versus V_{DD} were obtained after each irradiation to evaluate the degradation in circuit performance. The shmoo plot reveals the region of error free operation in a space defined by the ranges of V_{DD} and one of the six circuit parameters. The six circuit parameters monitored were input voltage low, input voltage high, output voltage low, output voltage high, operation frequency, and supply current. In ALU 33814-0506 and 33096-0507, the shmoo plots show the area of error free operation to be shrinking with increasing radiation dose. This trend can be seen in the shmoo plots of V_{DD} versus V_{IL} of ALU 33814-0506 in Figure 81, where the white space shows the area of proper operation. This trend is also seen in the shmoo plots of the other monitored parameters of ALU 33814-0506 and 33096-0507. Reduction in the area of error free operation occurs at approximately 3x10^7 Rad(GaAs) but for a fixed value of V_{DD}=2.25V the degradation of the circuit parameters is less than 10% at 1x10^8 Rad(GaAs). In the other two ALUs, no substantial shrinking of the error free operating region was observed even at 1x10^8 Rad(GaAs).

Transient Ionizing Dose: Transient Ionizing Dose Testing was performed on the ALU at the Naval Research Laboratory using 20 ns and 500 ns pulsed ionizing radiation. The custom ALU circuits were operated at 50 MHz during the irradiation. Figure 82 shows the test configuration.

When using the 20 ns pulsed irradiation, errors in data-out were strongly dependent on when the radiation pulse occurred compared to the ALU clock cycle. Errors in data-out occurred after the radiation pulse in many instances, indicating upsets occurred in the input latches. Four levels of clocked-input data-latches cause upsets in the input latches to be delayed by as much as 4 clock cycles before they can be observed.

The work-thru dose rate of the custom ALU was determined by evaluating the ALU during 500 ns pulsed ionizing radiation. A work-thru dose rate of 1x10^8 Rad(GaAs)/sec. to 2x10^8 Rad(GaAs)/sec. was achieved. At dose rates above 2x10^8 Rad(GaAs)/sec., the ALU circuit operation becomes unreliable, with one or more output bits in error during the radiation pulse. Figure 83 shows the least two significant bits, C_0, and C_1 during a 500 ns ionizing radiation pulse. An error in the output data occurs approximately 50 ns after the start of the radiation pulse at .2μs. The custom ALU becomes totally inoperable at dose rates of approximately 5x10^8 Rad(GaAs)/sec. Recovery times approach 150 ns after the radiation pulse ends at dose rates above 3x10^9 Rad(GaAs)/sec.

SINGLE EVENT UPSET:256-BIT GaAs SRAM

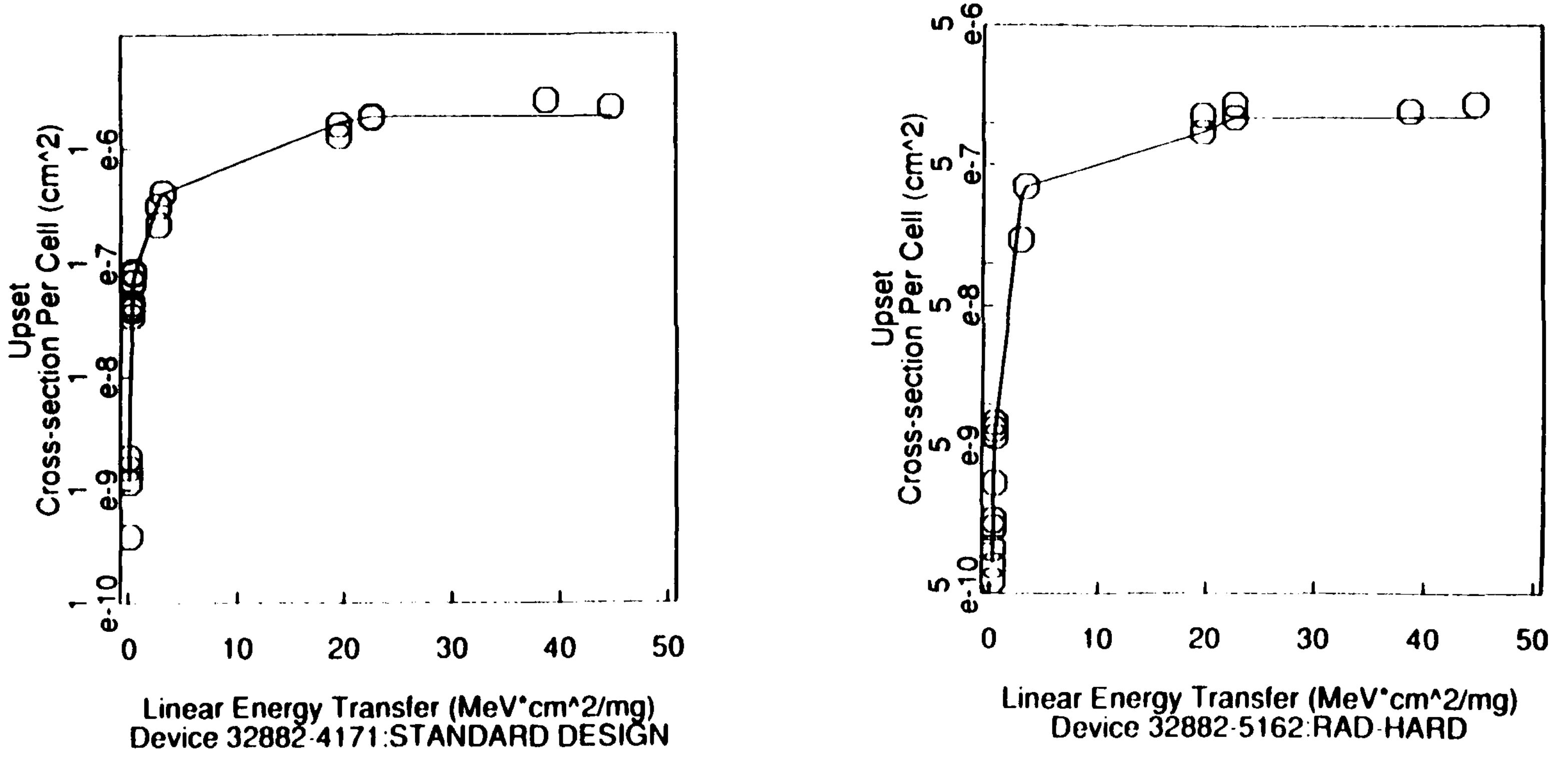


Figure 80 - Single Event Upset Results for PT-2M Memory

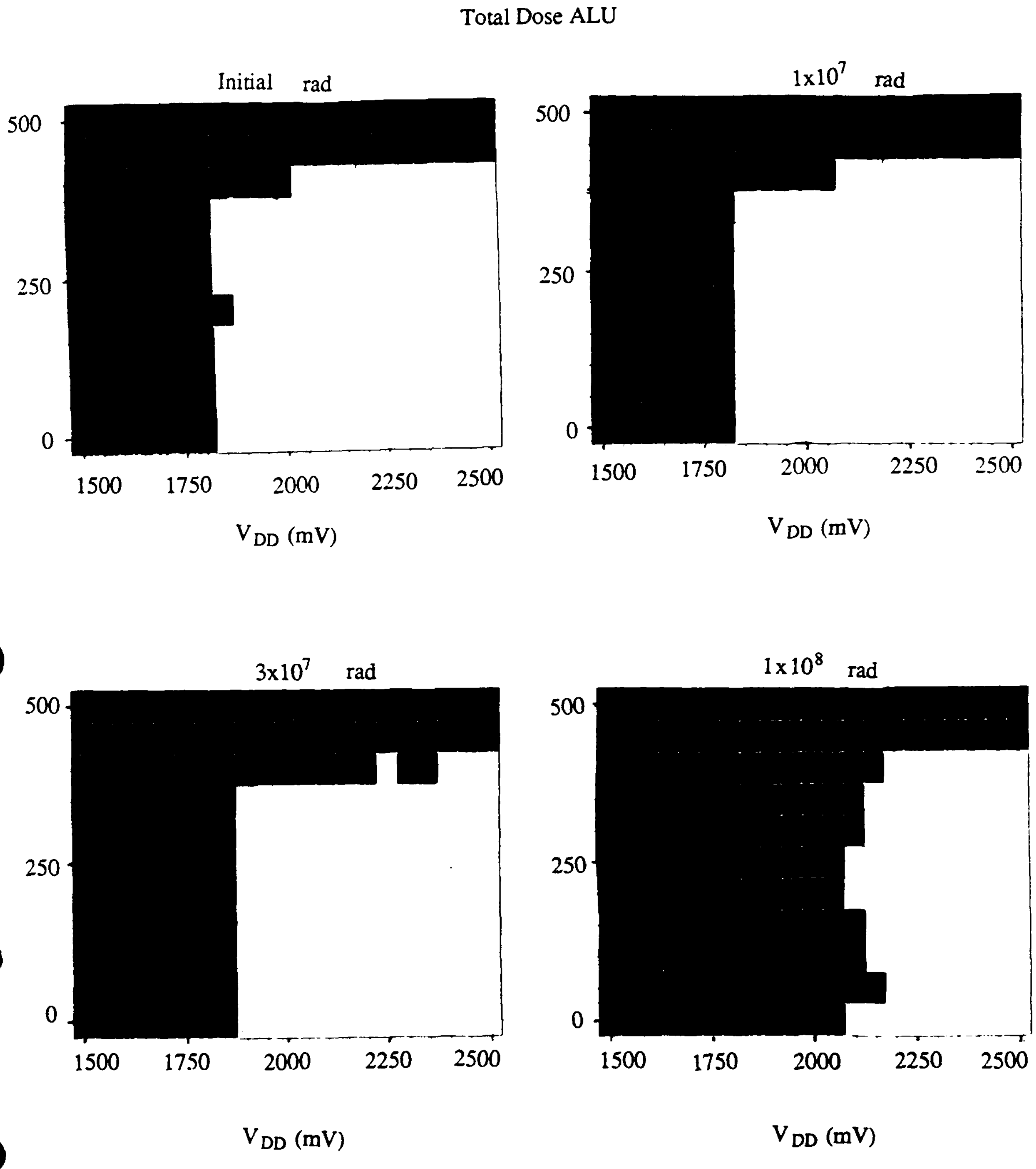


Figure 81 - Effect of Total Dose on ALU Shmoo Plots (V_{IL} vs. V_{DD})

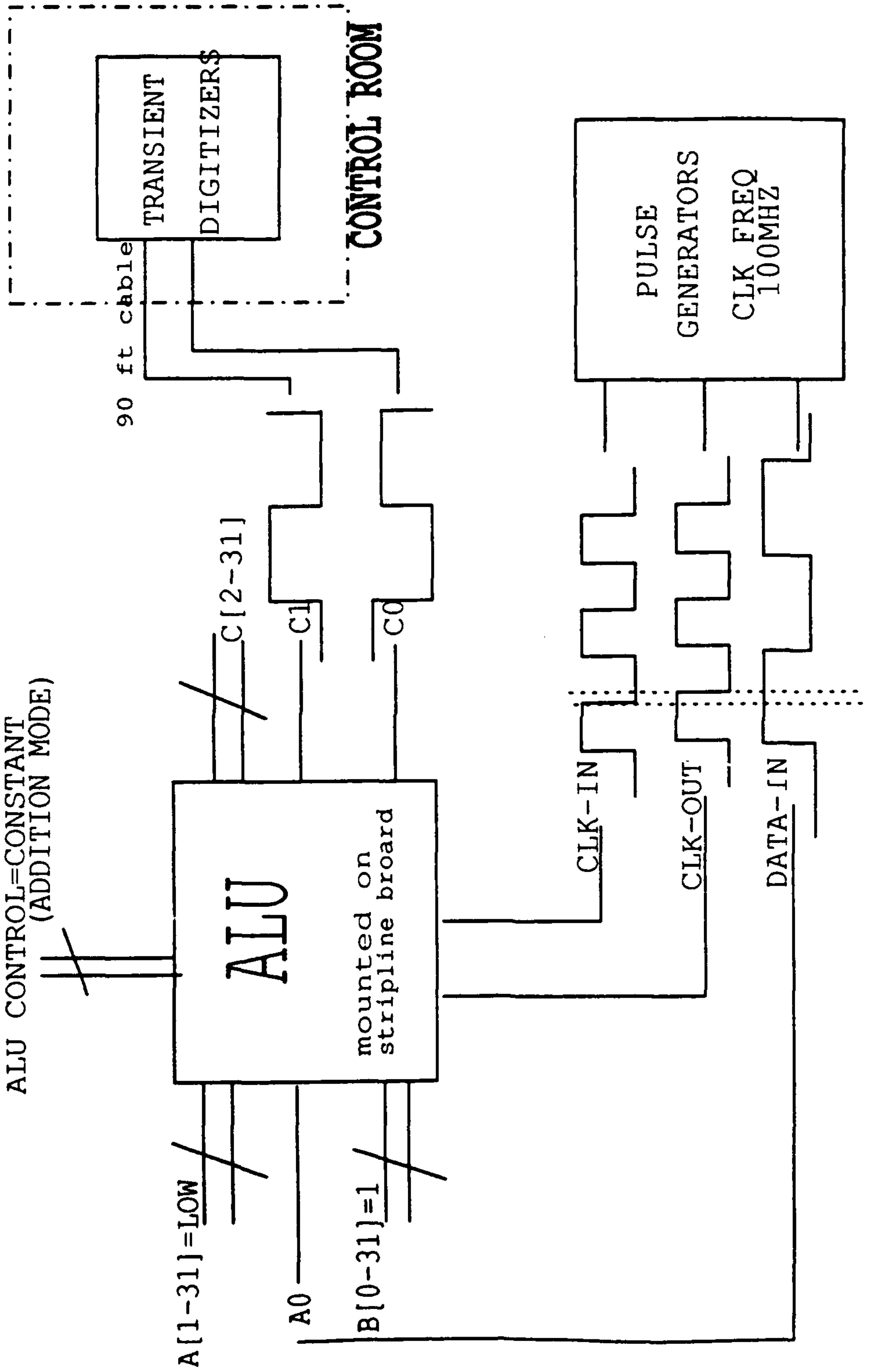
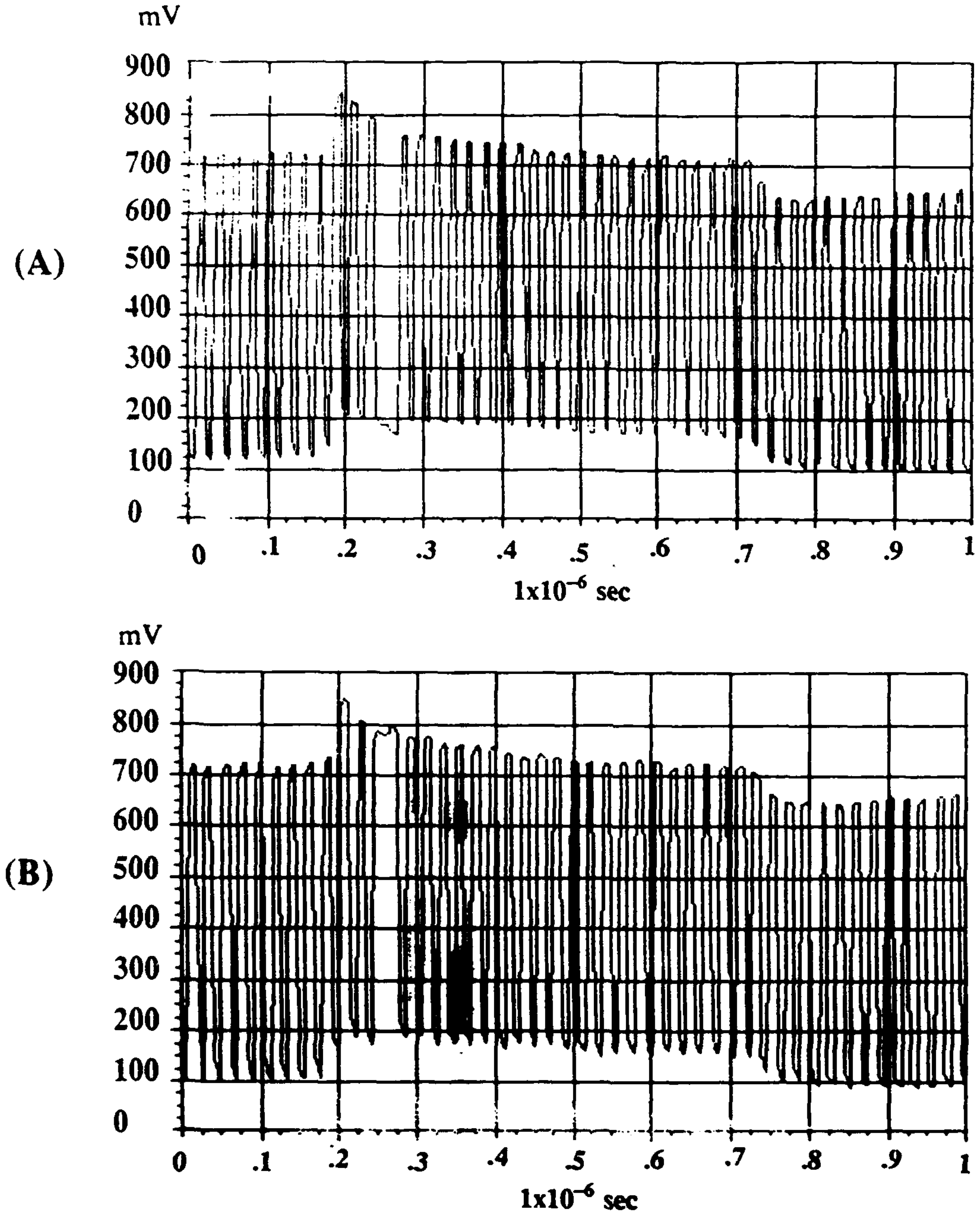

CONTROL ROOM
TRANSIENT DIGITIZERS
90 ft cable
PULSE GENERATORS
CLK FREQ 100MHZ
C[2-31]
C1
C0
ALU CONTROL=CONSTANT (ADDITION MODE)
ALU
mounted on stripline broard
CLK-IN
CLK-OUT
DATA-IN
A[1-31]=LOW
A0
B[0-31]=1

Figure 82 - ALU Transient Ionizing Dose Test Configuration

TRANSIENT IONIZING DOSE TESTING



ALU output bit (A) C_0 and (B) C_1 during 500ns pulsed ionizing radiation: Upsets just start occurring ($3x10^8$rad(GaAs)/sec, addition mode, Clk Freq=100MHZ).

Figure 83 - ALU Transient Dose Testing

Conclusion

Table 42 summarizes the radiation testing results of the SRAM. The average and best results are shown for total dose, transient dose, and SEU radiation tests. The SRAM lived up to expectation for total dose hardness at 1×10^8 Rad(GaAs). This result is consistent with discrete HFET total dose measurements. The best transient ionizing dose result was far beyond expectation based on discrete HFET transient measurements, where large gate and drain photo currents were measured at approximately 1×10^9 Rad(GaAs)/sec. The SEU results were far short of expectation. This is due in part by the large upset cross sections caused by the row failures from particles with large LET values and by the very low LET threshold caused by the small memory cell off-driver FET drain voltage of approximately .7V. This voltage is limited by the EFET Schottky barrier height.

Table 42 - SRAM Radiation Test Results

Radiation Test	Average Results	Best Result
Total Dose	1×10^8 Rad(GaAs)	1×10^8 Rad(GaAs)
Trans. Dose	2×10^8 Rad(GaAs)/sec	1×10^{10} Rad(GaAs)/sec
SEU	1.3×10^{-3} errors/bit day	1.3×10^{-3} errors/bit day

Table 43 summarizes the radiation test results of the ALU. The table shows the average and best results for transient ionizing dose and total dose testing. For total dose testing, the difference between the best result and the average result is due to the small sample size coupled with lot to lot variation. The transient ionizing dose results are work-thru dose rates and can be expected to be lower than the SRAM static transient results, where device logic is not changing states during the irradiation. The results were expected to approach those of the PT-1 ring oscillator, 1×10^9 Rad(GaAs)/sec. range, but due to threshold variation and correspondingly low inverter noise margins, it is not surprising that we did not achieve 1×10^9 Rad (GaAs)/sec.

Table 43 - ALU Radiation Test Results

Radiation Test	Average Results	Best Result
Total Dose	7×10^7 Rad(GaAs)	1×10^8 Rad(GaAs)
Trans. Dose	1×10^8 Rad(GaAs)/sec*	3×10^8Rad(GaAs)/sec*

*work-thru dose rate

4.2 Electromigration (Y. L. Cho and R. L. Remke)

Electromigration experiments were performed on PT-0 top metallization strip patterns. The samples were subjected to different sets of stress levels to induce failures which in turn would enable us to determine the activation energy E_a and the n-factor from Black's expression (J. R. Black, "Electromigration - A Brief Summary and Some Results," IEEE Trans. Electron Devices, ED16, April 1969). According to the model, median time to failure (MTF) can be written as:

$$\mathrm{MTF} = AJ^{-n} \exp\,[E_a/k_B T]$$

where A = constant, J = current density, k_B = Botzman's constant, and T = temperature in degrees Kelvin.

At the high stress level of 250°C and current density of $J = 7\times10^6$ A/cm^2, we have been able to induce an electromigration failure on the Ti/Pt/Au metallization in a relatively short period of time. During this aging, the resistance of the metallization increased steadily up to 70th hour. At this point, the resistance started to fluctuate. A microscopic inspection showed a series of void formations in the metallization line, and the resulting mass transport was clearly observable (Figure 84).

To establish the activation energy and the n-factor involved in the electromigration process, we used the TRACE method (Temperature-ramp Resistance Analysis to Characterize Electromigration - R. W. Pasco and J. A. Schwarz, 1983 IEEE Intl. Reliability Physics Symp.). Additional electromigration aging tests were conducted at various temperature and current density levels, using a failure definition of any change exceeding 10% from the original resistance value of the sample. Combining the results, an expression for median time to failure (MTF) in hours was obtained:

$$\mathrm{MTF} = 2\times10^{11}\, J^{-n} \exp\left(\frac{E_a}{k_B T}\right)$$

where J = current density (A/cm^2), $n = 2$, and E_a = activation energy = 0.43 eV. Using the above MTF expression, a MTF of about 10^8 hours was predicted for the current density of 10^5 A/cm^2 and temperature of 55°C.

4.3 Reliability Testing: High Temperature Operating Bias (P. F. Thompson)

Thermal Aging

PT-2M memories were thermally aged for 2000 hours. Four parts each were aged (no bias) at 150°C, 175°C, and 200°C, with an additional four parts as controls. All four 150°C devices survived 2000 hours. One 175°C and one 200°C device failed at 1000 hours. One additional 175°C and all three remaining 200°C devices failed at 2000 hours. A failure is defined as less than 256 working bits in either pipeline or ripple mode. Thermal aging was used as a "disaster check" - an early look for large-scale catastrophic problems while preparations for formal reliability testing were progressing. No lifetime or failure rate predictions were planned due to the small sample size. The initial values of two parameters, V_{GS} and V_{DD} (Min) may be sensitive indicators of potential device failure. They were studied during thermal aging, but no consistent or significant changes were observed among the devices as a whole or the devices that failed.

HTOB-1

Two High Temperature Operating Bias experiments were conducted with the PT-2M memories. In the first test, seventy-nine devices were examined: 26 at 150°C, 27 at 175°C, and 26 at 200°C. Eight additional devices were used as controls. Chips were taken from two wafers and assembled into 44-lead ceramic packages. A non-hermetic lid-attach was used. All tested and control devices were fully functional, with 256 working bits in both pipeline and ripple modes and an operating speed of at least 200 MHz. Devices were statically biased during HTOB. At 16, 32, 64, 128, 256, 600, and 1000 hours, devices were removed from reliability testing and electrical characterization was performed. After the 1000 hour electrical characterization, failures were inspected and lifetime parameters determined.

Bit loss was used as the failure criterion, with failure statistics being determined for 1, 10, and 26 lost bits. (26 is 10% of the 256 bits.) While the loss of one bit indicates a failed memory, we believe a single bit loss is not an accurate indicator of reliability statistics. The 256-bit PT-2M memory is a preliminary design. One known weakness is the propensity for bit flipping, and another problem is sub-threshold current. These and other early design weaknesses were addressed in the revised memory design (4K SRAM II). Failure criteria from one bit to 10% bit

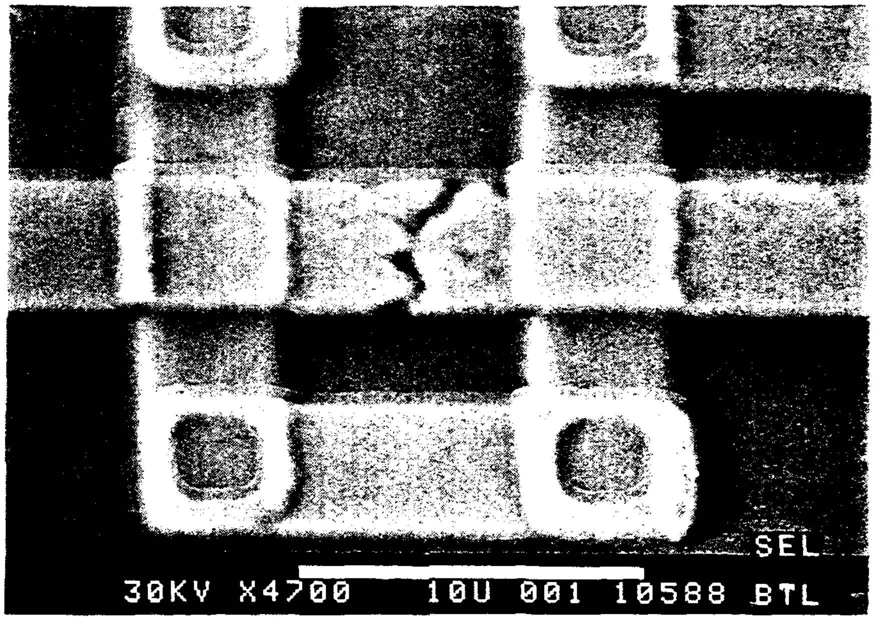

SEL
30KV X4700 10U 001 10588 BTL

Figure 84 - Metal Migration Voids Formed due to Current and Temperature Stressing

loss were used to determine lifetime. The intent of the HTOB test was to gauge reliability of the digital technology, and not to examine the reliability of the preliminary PT-2M design in particular.

Relative changes in electrical parameters, such as Vgs (an equivalent gate-drain voltage), VddMn (minimum supply voltage for the part to work) and I_{dd} (total current), were considered as possible failure criteria, but these parameters did not change in a consistent manner. There were no statistically significant differences in parameter changes between failed and good devices and between control and failed devices. In addition, the changes were extremely small (typically less than one percent), even in the case of 10% bit loss.

Electrical test data for the eight control devices remained stable through 1000 hours. No bits were lost, and electrical parameters showed no statistically significant changes.

All failed devices were delidded and visually inspected at 200X. There were no signs of physical damage, electromigration, etc. Such a result is not surprising, since the parametric changes were generally gradual.

Lifetime parameters were calculated with the assistance of STAR (STatistical Analysis of Reliability), an AT&T software package. The lognormal distribution (Equation 1) was used to model failure behavior. In Equation 1, T_{50} refers to the median lifetime, and σ is the shape parameter for the lognormal distribution.

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} \exp\left[-(1/2\sigma^2)\,(\ln t - \ln T_{50})^2\right] \qquad (1)$$

Median lifetimes from the three test temperatures are used with the Arrhenius relation (Equation 2) to determine the activation energy (E_a) and the constant C. k is Botzman's constant, and T is temperature in K.

$$T_{50} = C \exp(E_a/kT) \qquad (2)$$

Once T_{50} for one temperature and E_a have been calculated, T_{50} for any desired temperature can be found from Equation 2.

Table 44 contains MTTF, E_a and s values for 65°C ambient, for each bit loss criteria considered.

Table 44 - PT-2M Reliability Results for Different Bit Loss Criteria

# bits	MTTF	E_a (std dev)	σ (std dev)
1	1.5×10^6	0.64(0.15)	1.30(0.15)
10	2.0×10^6	0.88(0.18)	1.01(0.15)
26 (10%)	2.0×10^6	0.86(0.18)	1.07(0.16)

E_a for electronic devices typically falls in the range of 0.7-1.7eV. As σ increases, the maximum failure rate increases and moves towards smaller time, and the distribution becomes less symmetrical. For a σ of about 1.0, peak failure rate is well before T_{50}, with a relatively large tail (asymmetry) to large times. The standard deviation for E_a and sigma are contributed to by the sample sizes, missing test data, and the nature of the preliminary PT-2M design. For ten percent bit loss at an operating temperature of 65°C, T_{50} is 1.96×10^6 hours (224 years), and the maximum failure rate over ten years is 75 FITs at ten years.

HTOB-2

In the second PT-2M memory HTOB test, 29, 30, and 29 devices were aged at 150, 175 and 200°C respectively. In addition, there were eight controls (non-biased, not thermally aged).

Nominal planned characterization timepoints were 100, 200, 500 and 1000 hours. These devices differed from those of HTOB-1 in two significant ways: First, while we used the same package type as in HTOB-1, these devices were hermetically sealed. Second, the devices themselves were higher quality than in HTOB-1. These devices came from the later stages of PT-2M fabrication, where yields and device performance were much higher than before (see Section 3.6).

After 1000 hours, only one device had failed according to the 26 bit loss (10%) failure criterion from HTOB-1. The failure occurred at the first electrical characterization, 96 hours, on a device aged at 150°C. The device was non-functional in both ripple and pipeline modes. This single failed device may be reasonably considered an infant failure (an isolated, early failure not representative of later reliability performance). In an effort to obtain additional reliability data, the test was extended to 2000 hours. No failures occurred in the 1000 to 2000 hour interval.

To try to obtain failure rate information, bit losses other than 26 could be used as a failure criterion. Since no device other than the previously described non-functional device lost more than two bits, both one and two bit failure criteria were considered. Neither provides usable reliability information. In both cases, failures show no temperature dependence. In fact, 150°C devices showed the highest early failure fractions. Also, assignment of failure times is difficult because low bit losses tend to be intermittent. Of the 14 devices that lost one bit at some test point, five contained 256 working bits at 2000 hours. Similarly, two of six devices losing two bits recovered by 2000 hours.

A conservative reliability estimate can be obtained by using the lifetime parameters from HTOB-1 and the fact that no reliability failures had occurred by 2000 hours. The parameters of interest from HTOB-1 are the activation energy, E_a (=0.86eV) and sigma (=1.07). To obtain a worst-case failure rate, assume the first 200°C failure occurred at 2000 hours, even though there were no real failures at that point. Then, using the lognormal distribution, the median life (T_{50}) is calculated to be $2.6X10^7$ hours (>2900 years) at the use condition of 65°C. The maximum failure rate in the first ten years occurs at ten years and is much less than one FIT. In comparison, for AT&T GaAs lightwave codes, the maximum failure rate is 40 FITs at 65°C ambient during a ten year life.

It is interesting to note that the substantial increase in reliability between HTOB-1 and HTOB-2 corresponds to a substantial increase in manufacturing yield and device performance between the two sets of devices. This is not unexpected, since the higher performance devices are more robust and are much less susceptible to circuit failure caused by small FET parameter shifts.

5.0 LESSONS LEARNED DURING THE CONTRACT (R. C. Vehse)

Managers at DARPA and AT&T found that the Pilot Line contract did not unfold as intended, and both parties had to make changes in their approach for successful contract execution. For example, some of the inter-contractor interactions envisioned for this contract did not occur, and the prospects for viable growth in digital GaAs IC products dimmed as the projected ramp-up drew near. Still, accomplishments were an important by-product of the Pilot Line contract: (i) the GaAs IC technology has wide application for other AT&T programs, (ii) foundry procedures for Government procurements are now in place, and (iii) program management skills became the cornerstone for AT&T business practices.

A. Departures from the Statement of Work (Two Examples)

EXAMPLE 1: – The Statement of Work (¶4.8.1) requires that the contractor (AT&T) "establish an interfacing agreement with Raytheon, the prime contractor of AOSP, and Mayo Clinic, DARPA contractor for GaAs, CAD, to facilitate utilization of the Pilot Line products in the ACE module of the AOSP." The Advanced, On-Board Signal Processor (AOSP) provides the system lead for the demonstration circuits in the Pilot Line program. That is, circuit design and technical feedback provided by Raytheon for the chips produced by AT&T would help identify approaches leading to improved performance of the digital ICs.

During the first year of contract activity, it became clear that Raytheon would not provide the support expected. In fact, the entire program (Casino) built around the development of the AOSP collapsed and was discontinued. The Pilot Line contract was left without systems direction, and worse, no demonstration vehicle designs could be offered to link the contract with a viable military program. Considerable effort, not planned in the contact bid, was devoted to locating suitable demonstration device designs to build subject to Government approval.

EXAMPLE 2: – In another example, the Statement of Work (¶4.2.6) requires the contractor to develop a "user-friendly" CAD system "to allow outside users to design both fully custom and semi-custom circuits to be fabricated by this Pilot Line." Unfortunately, a string was attached: the contractor was expected, not required, to use existing software packages developed by another DARPA contractor, the Mayo Foundation. One can argue that the authors of the SOW had the best interests of the DARPA program in mind. Repeat development work is avoided, and the Pilot Line becomes an outlet for the software development contractor. Unfortunately, two problems prevented execution of this work task as intended: (i) the contract tasks did not fit together; i.e., the tools developed by Mayo Foundation would not be compatible with the CAD tools available to AT&T and Hughes designers, and (ii) CAD tool availability from Mayo Foundation did not fit the project schedule needs of the Pilot Line contact. The alternate CAD system developed for the Pilot Line contract was compatible with design tools available at both Hughes and AT&T (no added expense in capital funding), and commercially available software was more easily adapted than the custom designed packages offered by Mayo Foundation. Finally, the CAD system could be made ready for Pilot Line use according to the project schedule for the contract. Some hard feelings were generated by the AT&T decision, and the issue is again at the contractor interface.

In summary, the interface between Government contractors is fragile and difficult to implement when specified in a Statement of Work. Obviously, everyone benefits when contractor teaming occurs, but it works best when companies join prior to contract award with an agreement to share expertise during its execution.

B. Dealing with Technical Challenges and Uncertainties

The Pilot Line contract challenged the contractor in six areas: (i) LSI capability, (ii) technology development, (iii) choice of circuit design logic, (iv) materials technology development, (v) modeling, and (vi) performance specifications. Design, manufacture and testing for four logic circuits and one memory circuit, not including iterations, were planned and executed against a background of parallel development and prove-in of these six topics. The most serious problems were created by the contract team's inability to provide adequate design models for the existing technology and deliver product that was within the manufacturing tolerances required. AT&T determined specifications for I/O voltage levels consistent with component integration requirements, and these specifications, coupled with those based on contract goals, set high standards for success. Also, circuit size and complexity requirements pushed chip size to the limits of the reticle opening, and D_0 factors became important yield factors. In hindsight, program objectives, technical obstacles and current capabilities determine contract performance expectations. The customer desires programs that "stretch" the contractor, and it may be that the "stretch" outweighed the possibility for accomplishment.

C. The Changing Business Environment

At the outset, both the contractor (AT&T) and the contracting agency (DARPA) agreed on contract goals. The Pilot Line contract is the third in a series of such contracts offered by DARPA to promote development of digital GaAs IC technology capable of large scale integration and high performance. AT&T bid and won the contract intending to develop the requisite technology to support expected opportunities in the marketplace of the 1990s. Basically, the market for digital GaAs components did not develop, and both parties, AT&T and DARPA, took different paths to accommodate the change. DARPA elected to stimulate the market by offering contractors the opportunity to gain acceptance for GaAs ICs in various insertion programs. Contractors would demonstrate clear advantages by using GaAs components and thereby gain access to existing military programs by replacing existing components. AT&T reviewed its position in this and other digital GaAs markets and decided that sufficient potential wasn't offered to warrant continued investment. This basic difference in marketing strategy caused significant stress in the relationship between contractor and contracting agency. It was resolved when AT&T agreed to pursue a specific OEM application for its product to test viability of its market projections. Circuits were designed and fabricated for an industry-wide competition. AT&T fared very well in the technical sense, but the business case developed for this opportunity suggested that AT&T would not realize significant financial gain because the required investment to achieve low cost manufacturing is too high. So, DARPA and AT&T agreed to follow their business directions separately.

What is the lesson learned? DARPA could have taken a more conservative approach by awarding the Pilot Line contract to a bidder with known and well-established traditions of long term involvement in military programs. Yet, new and competitive ideas are introduced by new players, and DARPA has to take some risk to realize the advantages of these ideas. AT&T could have put more effort in developing its investment in the digital GaAs market. The financial risk would be large, but sometimes big gains result from taking big risks. Given the actual case, it's better to look at the positive responses resulting from the decisions made by AT&T and DARPA.

D. Contract Benefits

As listed in the introduction to this section, the Pilot Line contract produced tangible results in three areas that will benefit both AT&T and their future military customers.

GaAs IC Technology – The SARGIC-HFET technology development was the core of the Pilot Line contract. AT&T was able to meet the performance requirements of the program using both EFETs and DFETs in the same circuit, but modeling for the variations in processing and materials structure became the central issue. In the competition for the OEM product application (high speed computing), only one FET type was used in the IC, and this concept became the basis for better control and wider applicability of the SARGIC-HFET technology. Today, at the end of the Pilot Line contract, AT&T uses the variations of the Pilot Line technology for wireless and lightwave communications products.

Foundry Capabilities – Another fundamental requirement of the Statement of Work is to establish foundry operations for future military customers. Implied in this statement is the existence of a suitable manufacturing technology. Process variations must be stabilized and predictable performance criteria must be met. These conditions were not completely tested during the term of the contract; however, AT&T developed manufacturing practices that are now used in foundry operation for microwave products for the Government. Specifically, AT&T has volunteered to participate as a beta-site in the certification and qualification of the foundry processing line to meet the standards of the Qualified Manufacturer's List (QML), MIL-I-38535.

Program Management Skills – As a novice contractor, AT&T had to learn and develop program management skills to conform with conventional practices expected by the contracting agency. This task needed dedicated resources, training, and corporate support. To acquire the necessary skills in the shortest possible time, AT&T engaged the services of an outside contractor, who provided a week-long workshop for all of the contract task managers. The core of AT&T management personnel having program management responsibilities became the practicing "experts" for this contract and for all Government contracts to follow. Certainly, the contractor and the contracting agency are both beneficiaries of this approach.

E. Conclusion

AT&T provided an honest effort to meet all the contract requirements. The changing environment produced dramatic changes in program direction and emphasis, but AT&T emerged with a sound technical approach for manufacturing GaAs ICs, and current military programs rightfully expect AT&T to deliver high performance ICs meeting the most exacting specifications. As a GaAs IC foundry, AT&T supports the Government quality initiatives, and demonstrates a capacity for continuous improvement so that lower cost components may be available.

APPENDIX A

AT&T SARGIC/HFET
Processing and Layout Design Guide

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Preface

Section I.
Overview

Introduction

This manual describes the design and layout of GaAs integrated circuits using the SARGIC/HFET (Self Aligned Refractory Gate Integrated Circuit/Heterojunction FET) process. It is divided into five sections covering the foundry operation, process flow, process specifications, layout design rules, device terminal characteristics, and process control monitor.

The first section covers the customer interface to the GaAs foundry operations at AT&T. This section also serves as an introduction to the digital SARGIC/HFET process.

The second section provides an overview of the steps used in the SARGIC/HFET process. Contained in this section are drawings which show the placement of each layer as the GaAs chips are manufactured.

The third section contains information on the process including sheet resistance of the metallization and implant areas, interconnect capacitance and device break down characteristics.

The fourth section outlines the layout of digital GaAs circuits in the SARGIC/HFET, 2μm design rules. It describes the circuit layout procedure level by level, and includes the process' layout design rules.

The fifth section contains the terminal characteristics of Enhancement (EHFET), Depletion (DHFET), and diode devices. This includes drain and gate I/V and capacitance curves at 25 and 125°C. The parameters were extracted from measured HFET and diode characteristics and fitted to a model named "SargicS.15."

The last section, Section VI, includes electromigration information.

Foundry Operation

AT&T prefers to receive a customer's design on a magnetic tape using GDS II format. AT&T foundry mask sets have requirements that may not be met by a customer generated reticle mask. Also, the proper stepper alignment features must be incorporated on the reticle mask with the primary die and Process Control Monitors.

General Design Rules

The AT&T DIGITAL SARGIC/HFET process is based on 1.0 μm gate length Enhancement (EHFET) and Depletion (DHFET) heterojunction devices. It is a self-aligned semi-planar process that implements two levels of metal interconnect with 2.0 μm line widths and spacing. The two metal layers are separated by a silicon-oxynitride dielectric.

The process can fabricate EHFETs, DHFETs, Schottky diodes, N+ implanted resistors, tantalum nitride resistors, and MIM (Metal Insulator Metal) capacitors. Device isolation is achieved by oxygen implant between active regions, which yields a semi-planar process.

The process gives the freedom to layout active and passive component circuits with a full two level metal interconnect. However, designers should adhere to the following guidelines when laying out a circuit:

1. Metal runners are not allowed to cross the active HFET area. Metal crossing over a gate can induce piezo-electric effects that cause shifts in device threshold voltages.
2. No metal, with the exception of the gate tabs and ohmic contacts, can be in contact with the substrate. This rule forbids the use of gate and ohmic metals for the purpose of interconnects in radiation hardened circuits. High resistivity will limit the length of these lines in other cases.
3. It is recommended that top metal is used for power rails, due to the lower sheet resistance and higher current carrying density. The rails should be made as wide as possible to prevent rail collapsing during exposure to radiation, as well as, designing for electromigration and ir drop limitations.
4. Be certain that all HFET gates are laid out in the same direction. The process utilizes single gate orientations in order to eliminate threshold voltage shifts due to piezo-electric effects. When wafers are fabricated, all gates will be aligned parallel to the major wafer flat.
5. It is recommended that HFETs in excess of 50 μm wide be broken into multiple fingers, if possible, and that the gates of long FETs be driven from both ends. This alleviates the high gate RC delay associated with the resistivity of tungsten silicide.
6. All Schottky diodes should be made in EHFET tubs. Diodes made on the DHFET surface are not repeatable and should not be used.
7. The SARGIC HFET process allows a minimum of 100 x 100 μm bond pads with 25 μm spacing. However, designers should make sure that probe cards can be made to accommodate the design. If probe cards cannot be made for the above design rules, then the pads can be made 120 x 120 μm with 80 μm spacing for which probe cards are readily available.
8. During layout, overlap connecting polygons by at least 1.0 μm to prevent pull-aparts during premask compensation.

Future Updates

The SARGIC/HFET process design manual will be updated in the future to keep abreast of the latest developments in modeling, process, and design support. Future updates will include, but not be limited to, the following information:

- Changes in processing to enhance yield;
- Improvements and updates on the Process Control Monitors;
- Improvements in design tools;

This manual is written for the designers of digital GaAs ICs in AT&T's SARGIC/HFET process. Input from all designers is welcome. This input will help improve this manual by identifying additional information that should be included as well as changes to the current content.

Section II.
Digital SARGIC/HFET Process Flow

ALM - ALIGNMENT MARK **Mask Tone: clear on opaque**

The first mask level for the SARGIC/HFET process is ALM, alignment mark. This is shown in Figure 2.1. The primary purpose is to transfer stepper alignment features to the GaAs surface. ALM will provide a reference to which several subsequent levels will be aligned.

ETB - EHFET TUB **Mask Tone: clear on opaque**

The HFET wafers are grown as DHFETs. This mask level is required to remove the top two layers of the heterostructure, i.e. GaAs and AlGaAs, in those regions where EHFET fabrication is required. Figure 2.2 shows the formation of an EHFET tub. The top layers are thin i.e. <400 Å total and the removal leaves a nearly planar surface. ETB is aligned to ALM.

ISO - IMPLANT ISOLATION **Mask Tone: opaque on clear**

Figure 2.3 shows the implant isolation step. This level is used to provide device isolation by ion implantation. ISO is aligned to ALM. The isolation level defines the size of both EHFET and DHFET devices.

GMT - GATE METAL **Mask Tone: opaque on clear**

Gate formation involves deposition of WSi_x, photoresist patterning, and reactive ion etching to pattern the gate to a final length of approximately 1.0 micron. This level is also aligned to ALM. Figure 2.4 shows gate formations on both EHFETs and DHFETs. This metal is directly on the GaAs and should not be used for interconnect.

NIP - N^+ **Mask Tone: clear on opaque**

The N^+ implant is shown in Figure 2.5. The gate acts as a self-aligned mask for the patterned N^+ implant process. This level is expanded relative to the device area to compensate for process bias/alignment tolerance. After implant, the wafers are annealed to activate the dopant. This level is aligned to ALM.

OMT - OHMIC METAL **Mask Tone: clear on opaque**

Source and drain contacts are defined by a lift-off which employs Au/Ge/Ni/Au metallization as shown in Figure 2.6. Ohmic and gate interconnect on GaAs should be minimized due to concern regarding radiation hardness. This level is aligned to GMT.

VA1 - VIA1 **Mask Tone: clear on opaque**

Patterning of the first dielectric layer is shown in Figure 2.7. This level involves the deposition of the first level dielectric of plasma deposited silicon oxynitride. After photolithography, via holes are formed by reactive ion etching. This level allows for contact to both ohmic and gate metal. This level is aligned to GMT.

BMT - BOTMET **Mask Tone: clear on opaque**

Bottom metallization is placed on the first dielectric level as shown in Figure 2.8. This process is also based on a lift-off technique which employs Ti/Pt/Au metallization. BOTMET also serves as the lower layer of the bonding pads. BOTMET aligns to VA1.

VA2 - VIA2 **Mask Tone: clear on opaque**

This process involves the deposition of a second layer of dielectric, 4000 Å thick. This process is analogous to VIA1. As shown in Figure 2.9, VIA2 may only contact BOTMET. Direct contact of VIA2 to GATE and OHMIC is not allowed. This level is aligned to BMT.

TMT - TOPMET **Mask Tone: clear on opaque**

The TOPMET process, shown in Figure 2.10, is analogous to the BOTMET process. Besides interconnects to BOTMET, this level also serves to define the bonding pads. TOMPET is aligned to VA2.

TAN - TaN Resistor **Mask Tone: opaque on clear**

Tantalum nitride resistors are defined before TOPMET. This layer is not used in every design and has not been shown in any of the Figures. The tantalum nitride thickness is typically 400 Å. TAN aligns to BMT.

PAS - PASSIVATION **Mask Tone: clear on opaque**

The last step in the SARGIC/HFET process is the application of a dielectric passivation as shown in Figure 2.11. The passivation level involves the deposition of a third layer of dielectric, 4000 Å thick, to cover TOPMET. After photolithography, bonding pads are opened by a plasma etch process. This level is aligned to TMT.

Figure 2.1. Alignment Mark. The first mask is the stepper alignment features which are transferred onto the substrate. This level is the alignment reference for several mask levels. The alignment marks are placed in the dicing lanes by AT&T.

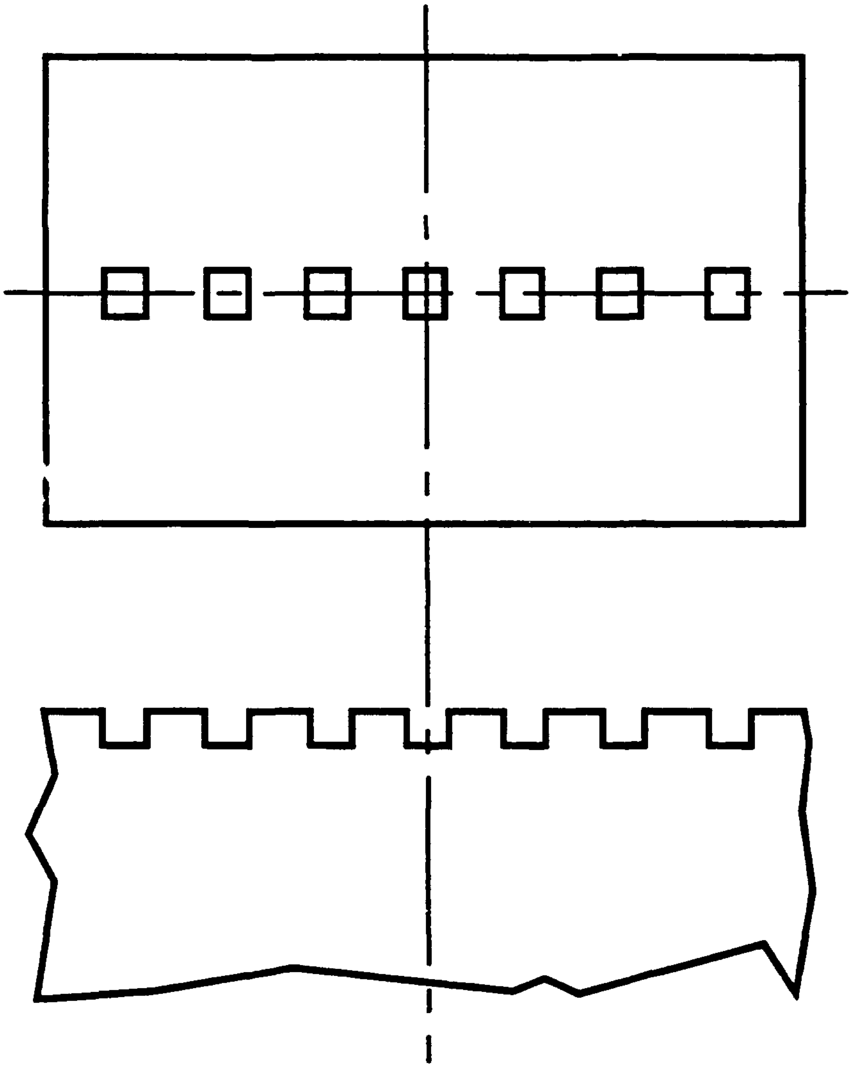


Figure 2.2. EHFET Tub. The SARGIC process starts with an all DHFET substrate. The formation of an EHFET requires the etching of the first two top layers in the starting substrate to form an EHFET tub. This tub is about 400 Å deep.

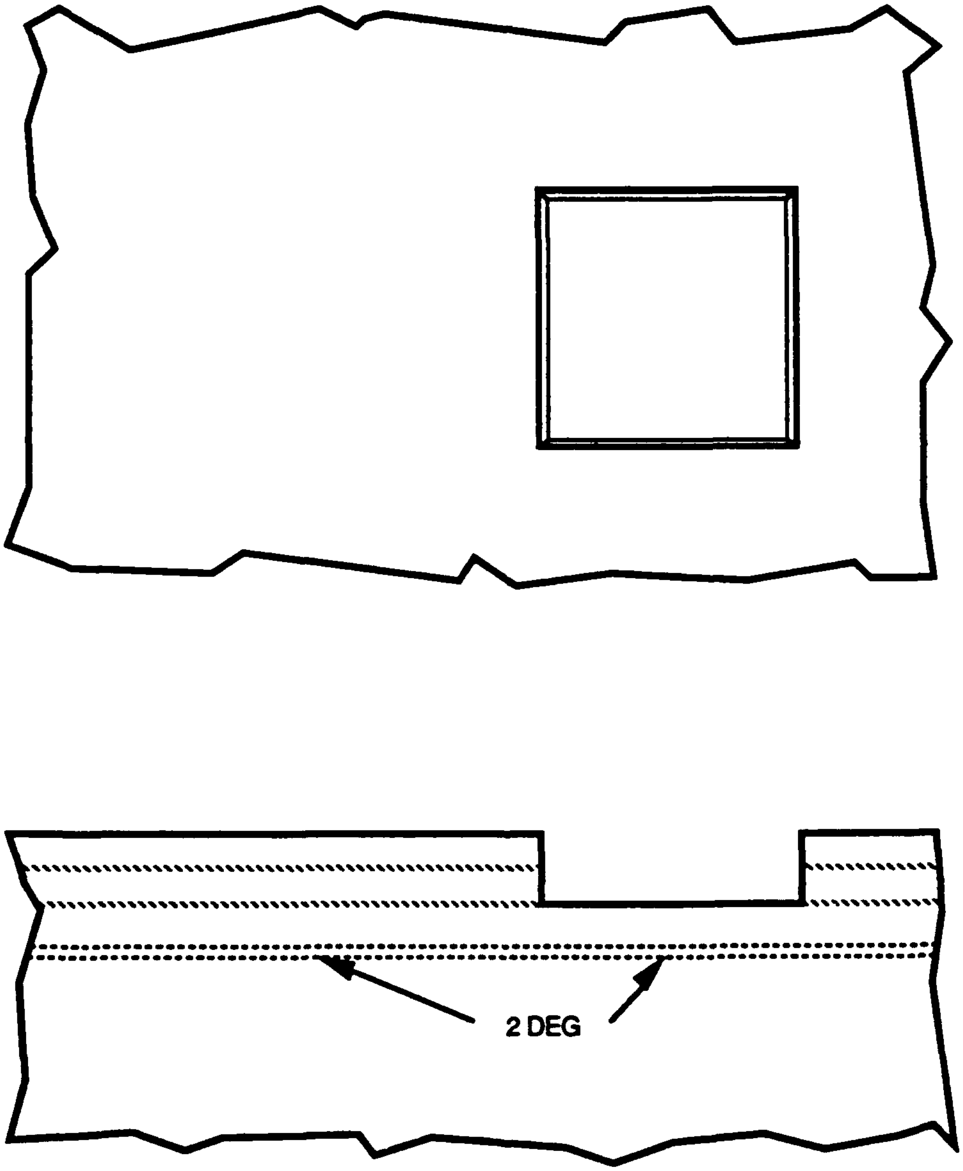


Figure 2.3. Implant Isolation. Device isolation is achieved by an oxygen implant into the substrate. This level will determine the active device dimensions.

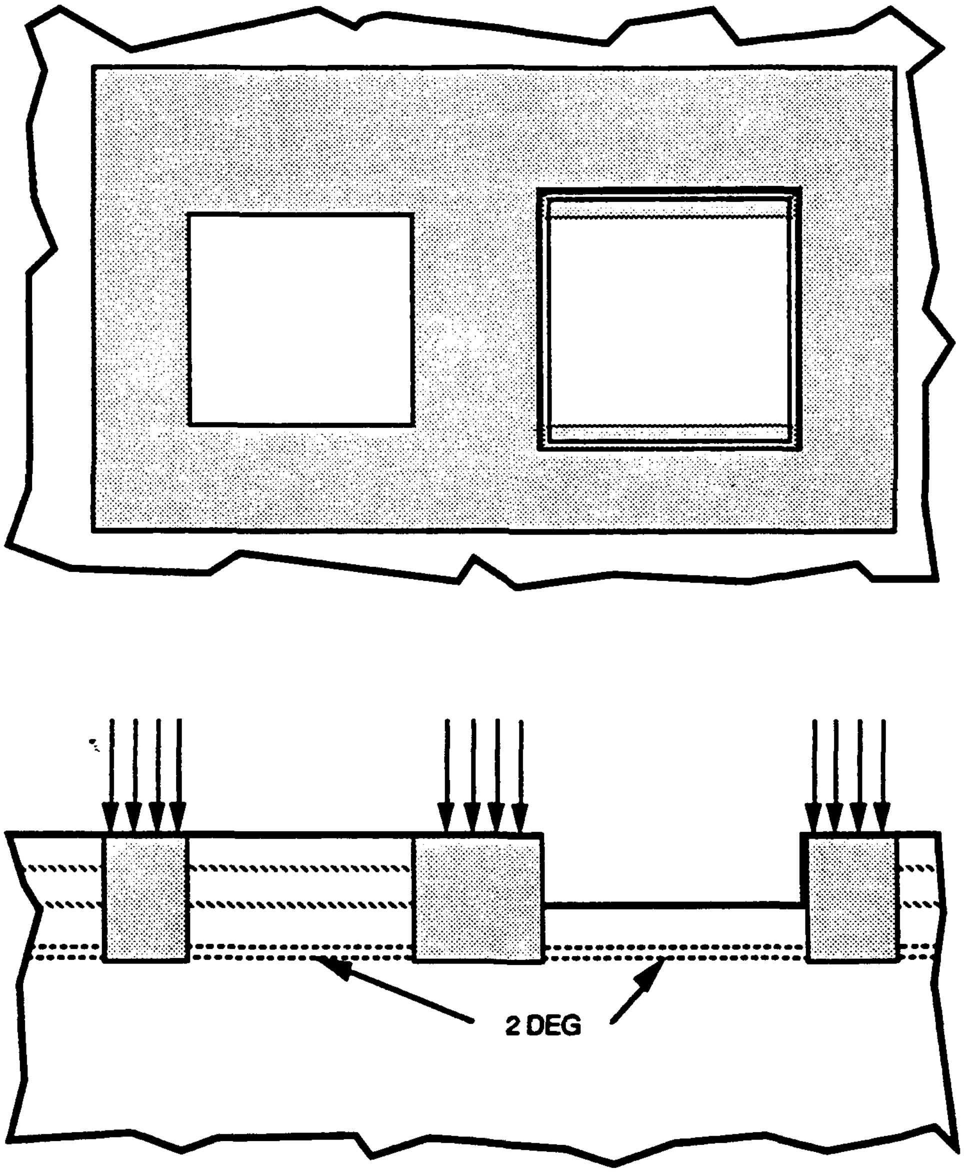
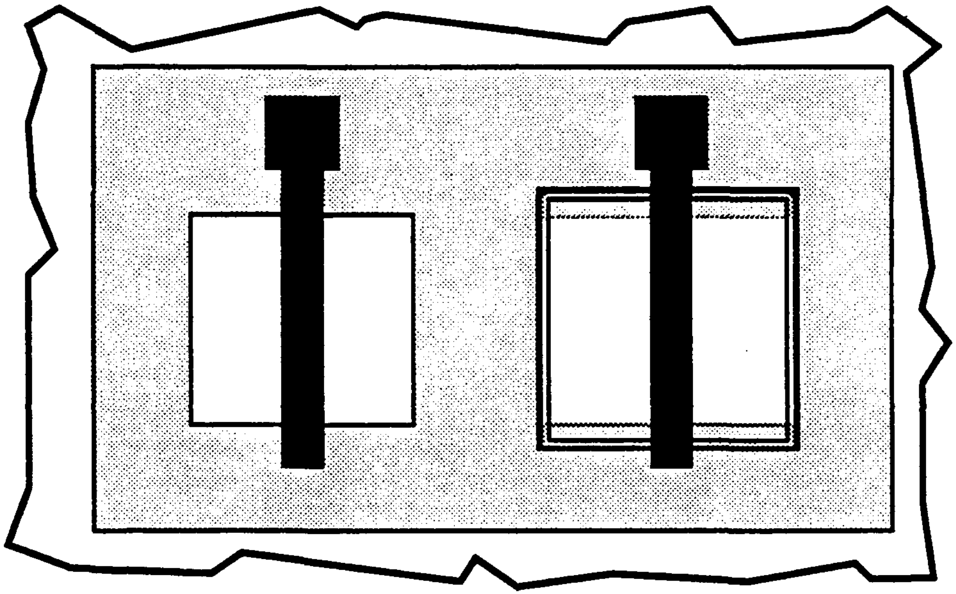


Figure 2.4. Gate Metal. The rectifying FET gates and Schottky diodes are formed by a WSi_x metal. After processing, the final gate lengths are 1.0 μm. Schottky diodes are designed to be 2.0 μm long. Gate metal should not be used for interconnect.



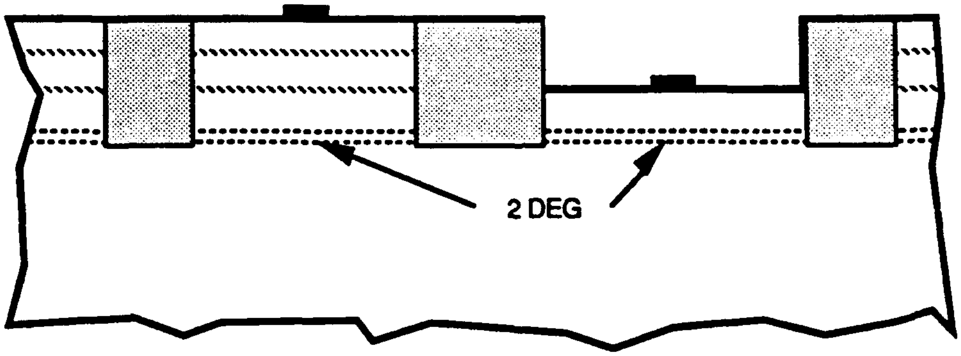
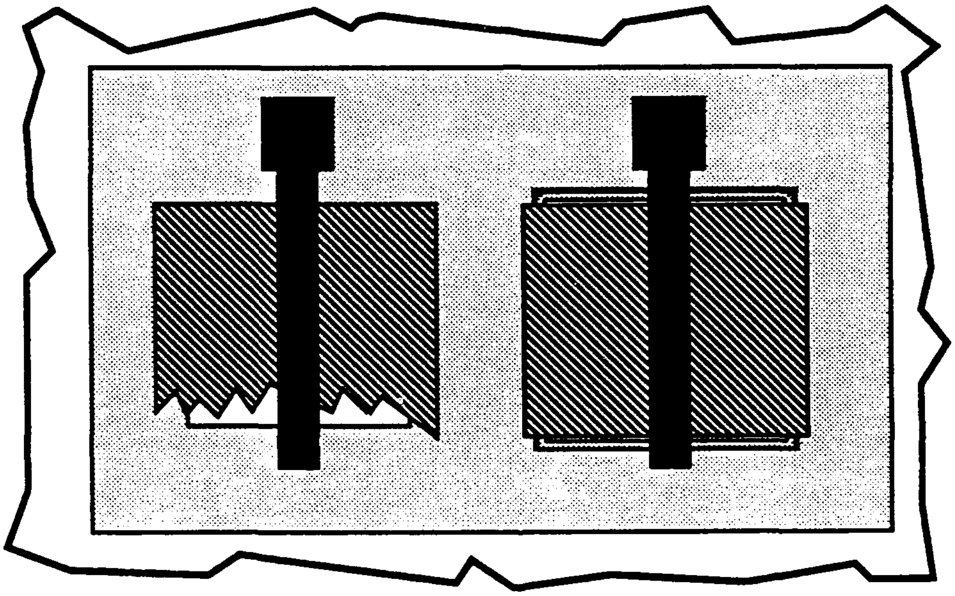


Figure 2.5. N^+ Implant. The N^+ implant mask is used for forming the drain and source contact regions. It is also used to form the implanted resistors and Schottky diode cathodes. N^+ runners should not be used for interconnect.



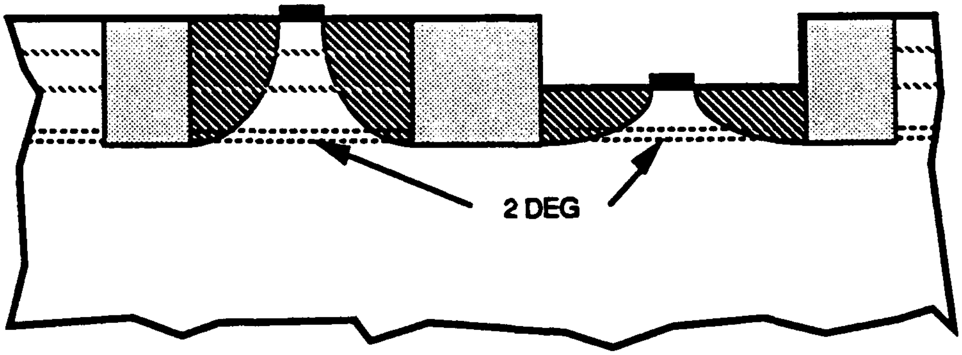


Figure 2.6. Ohmic Metal Contact. Ohmic metal is defined on top of the N^+ implant and alloyed to form the ohmic contact. This metal should not be used for interconnect.

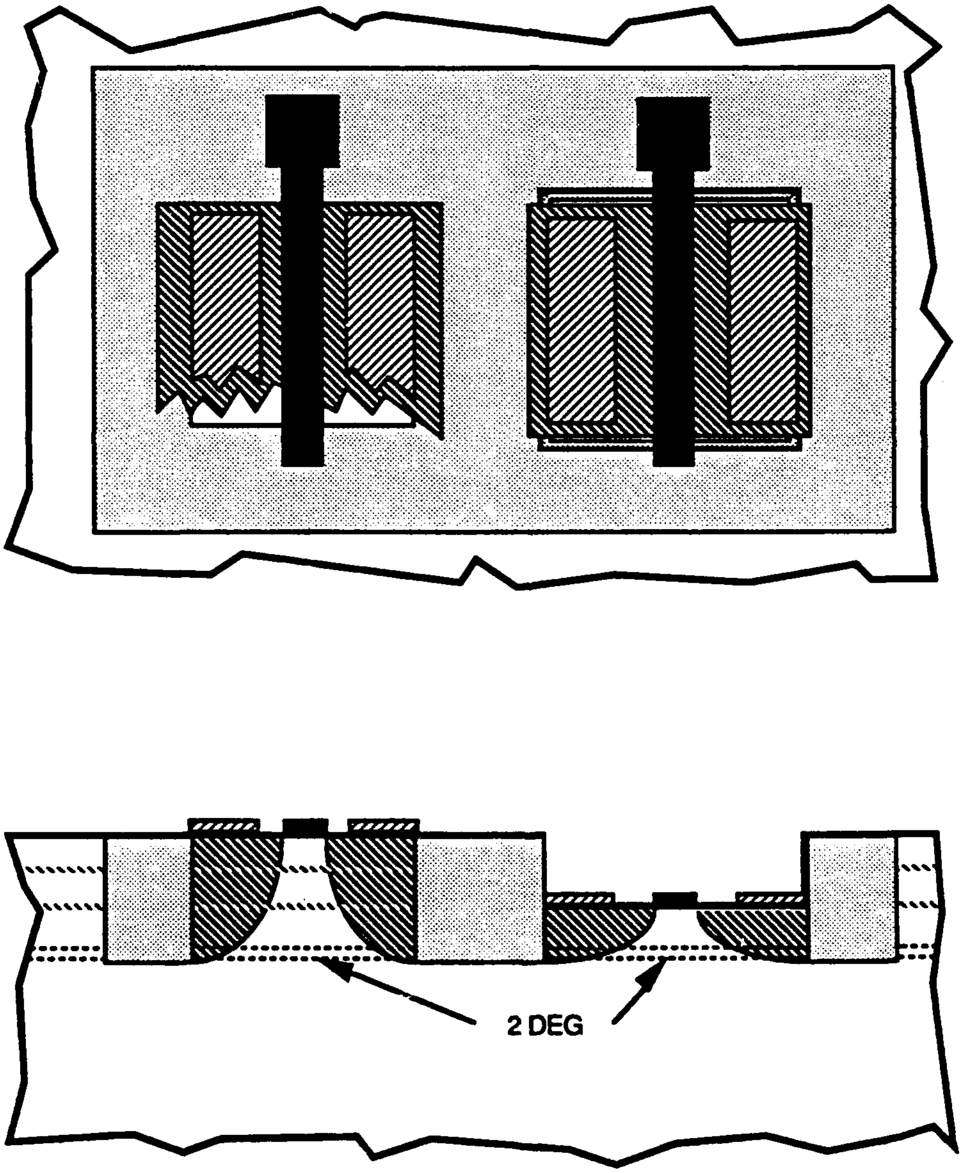
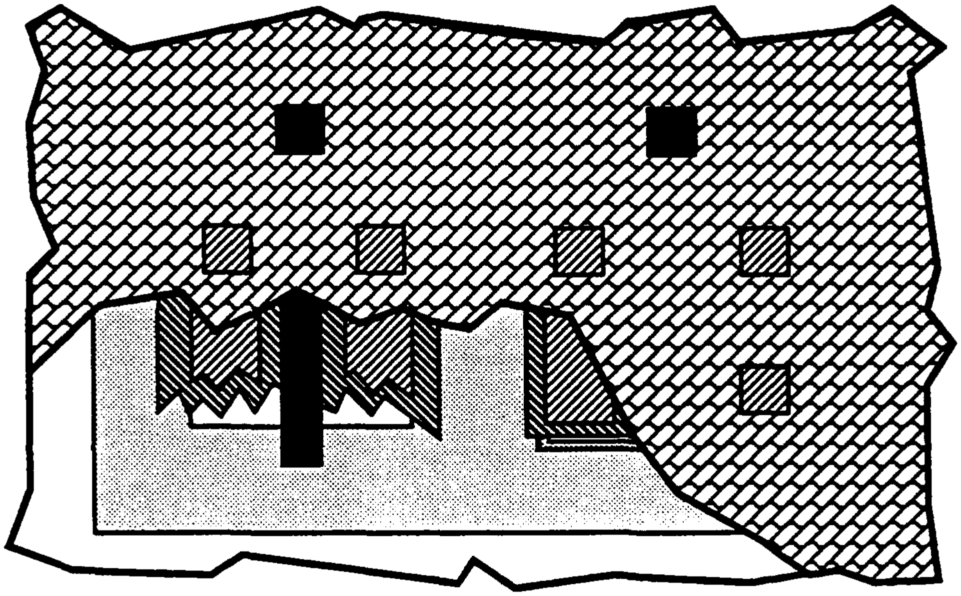


Figure 2.7. Dielectric Via One. A layer of silicon oxynitride is deposited on top of the gate and ohmic metals. A via is etched wherever an electrical contact is desired between the gate tab or ohmic metal and bottom metal.



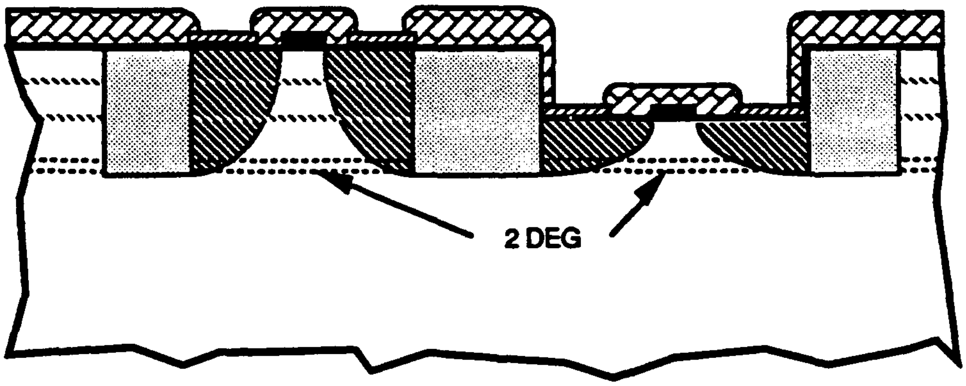
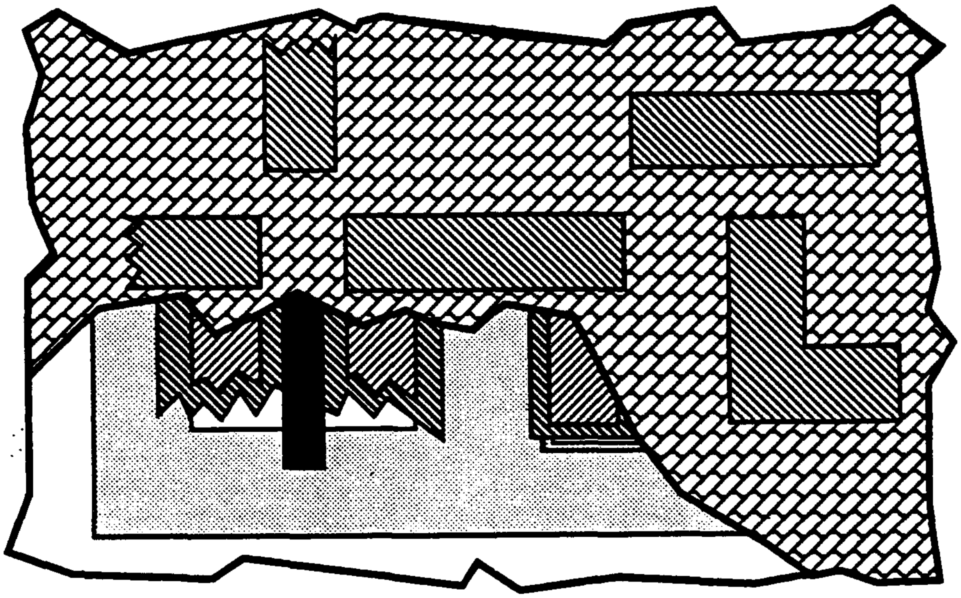


Figure 2.8. Bottom Metal. BOTMET is the first metal interconnection level. All electrical contacts to gate and ohmic metal must be done with BOTMET using VIA 1. This level also forms the bottom electrode of MIM capacitors and a bottom metal layer for the bond pads.



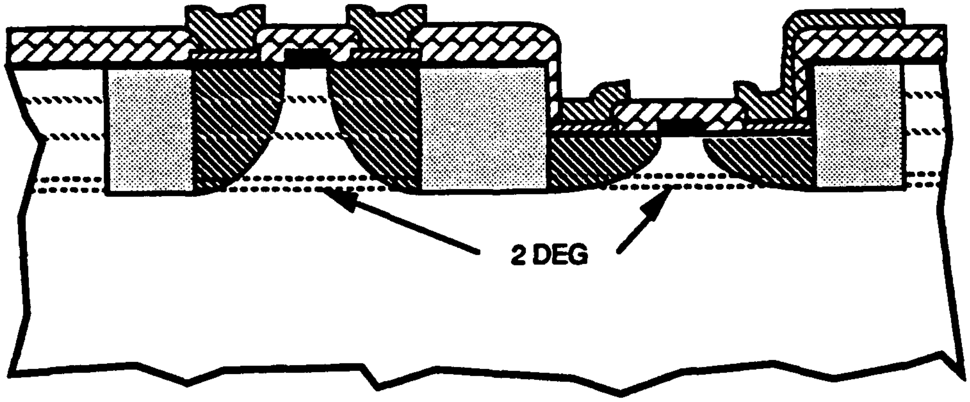


Figure 2.9. Dielectric Via Two. Following BOTMET, a layer of silicon oxynitride is deposited to isolate TOPMET from BOTMET. A via is etched wherever an electrical contact is desired between the two metal layers.

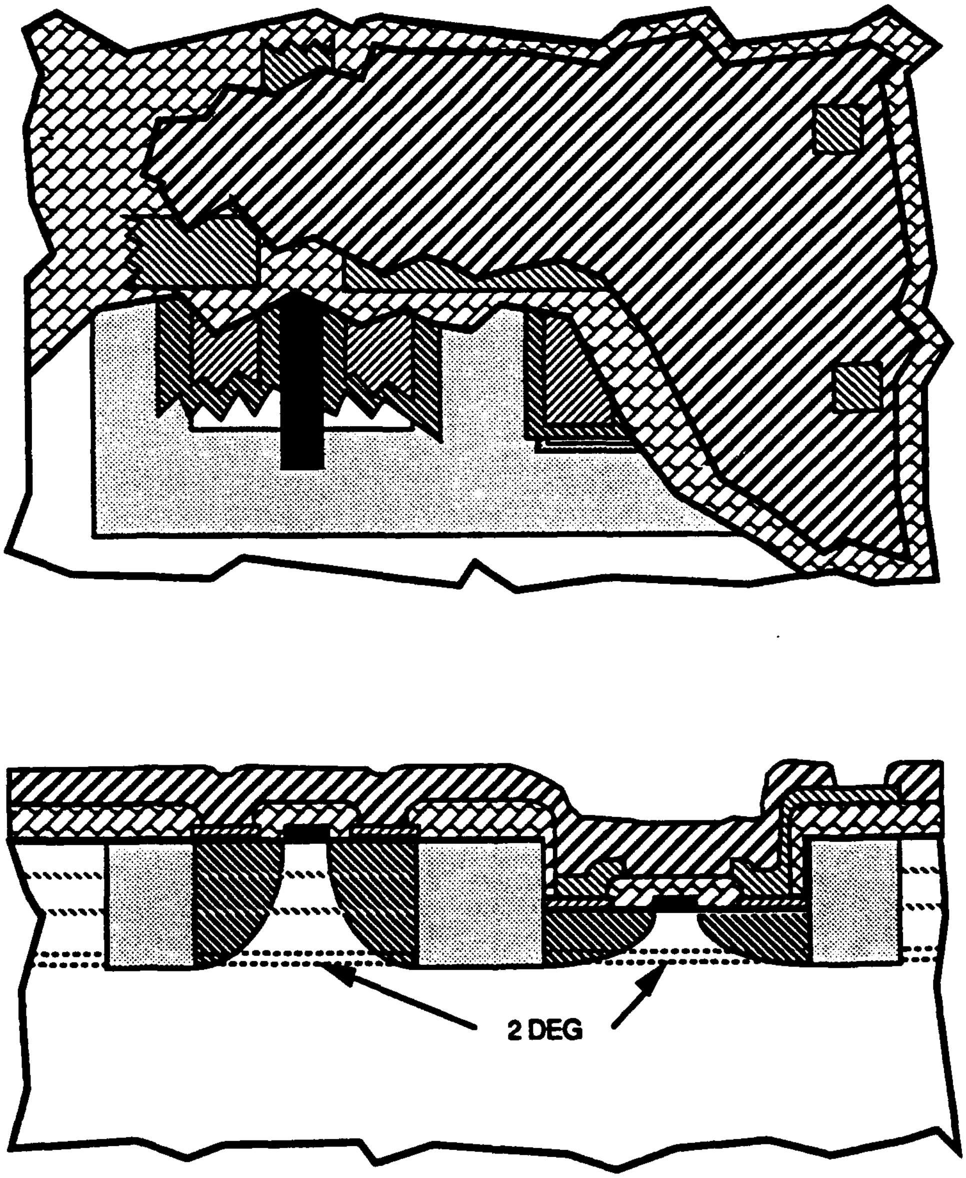
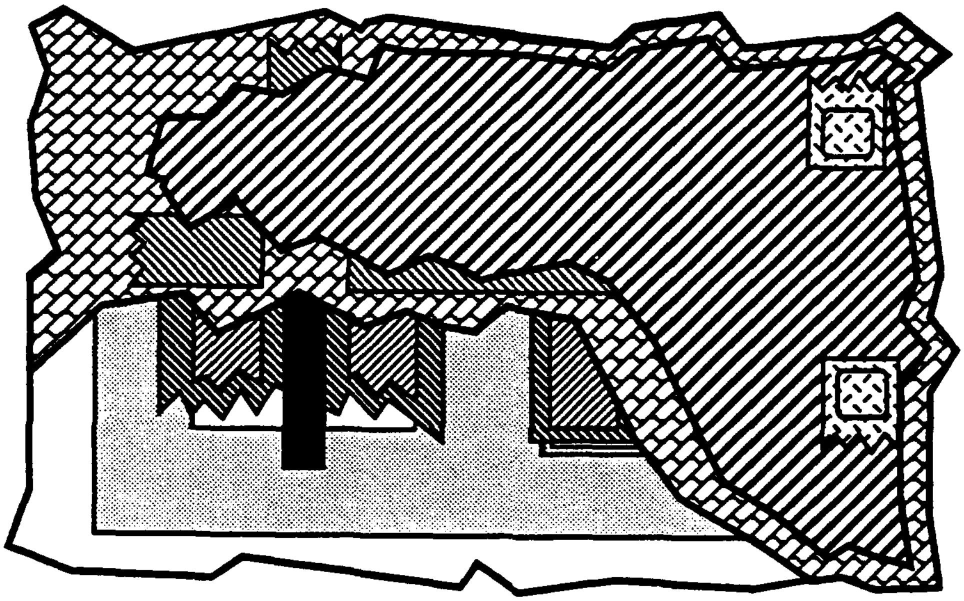


Figure 2.10. Top Metal. TOPMET is the second interconnection level. Slightly thicker than BOTMET, TOPMET is normally used for power runs to reduce IR voltage drops across the circuit. This level serves as the top electrode of MIM capacitors and top layer for the bond pads.



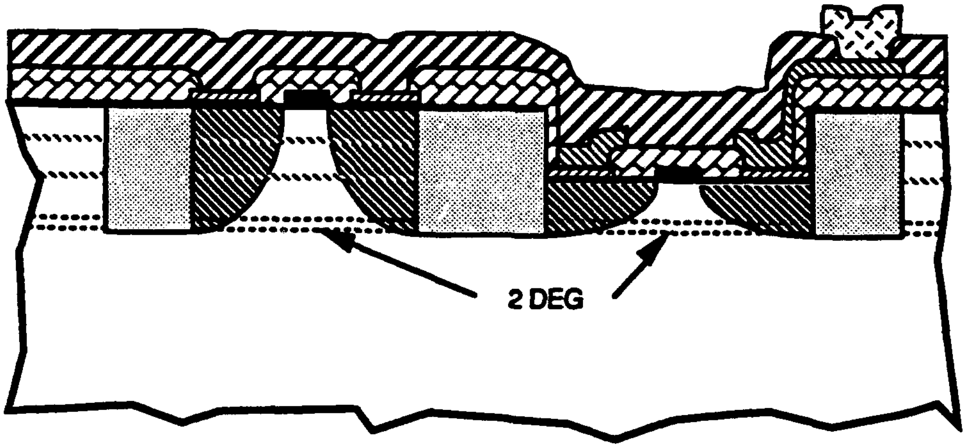
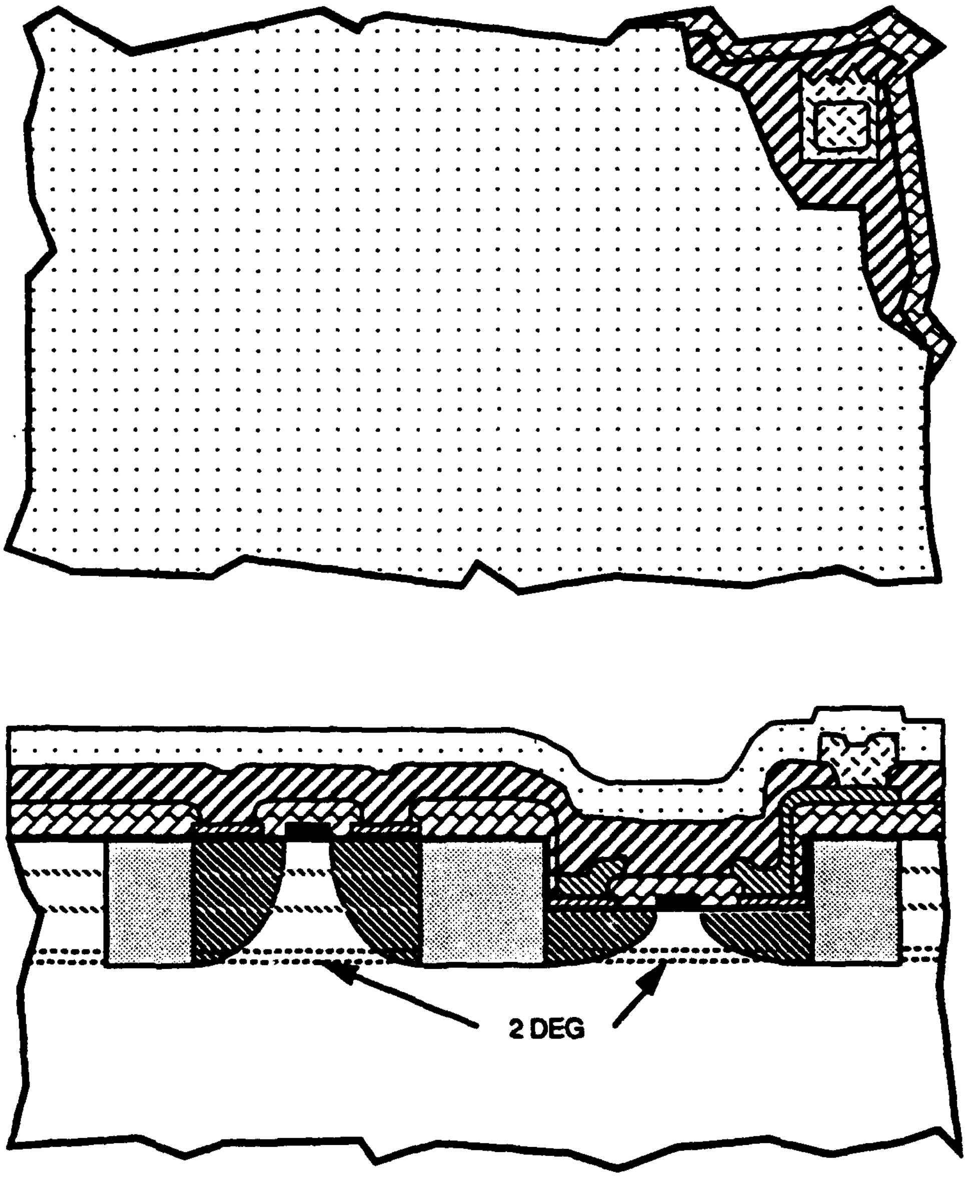


Figure 2.11. Passivation. The final process step involves the deposition of a passivating layer of silicon oxynitride over the entire circuit. This layer protects the GaAs circuit from mechanical and environmental damage. This level will have openings for the bond wires or solder bumps and PCM test pads.



Section III.
Process Specifications

Sheet Resistance

The following table describes the minimum, nominal, and maximum parameter values for the DIGITAL SARGIC process.

SYMBOL	PARAMETER NAME	MIN.	NOM.	MAX.	UNITS
RSNIP*	sheet R of N+	190	370	550	ohms/sq
RSTAN	sheet R of TaN				ohms/sq
RSGMT	sheet R of GMT	3.8	4.3	4.8	ohms/sq
RSOMT	sheet R of OMT	0.25	0.34	0.43	ohms/sq
RSBMT	sheet R of BMT	0.033	0.047	0.061	ohms/sq
RSTMT	sheet R. of TMT	0.020	0.031	0.042	ohms/sq
RC EHFET	EHFET ohmic contact resistance per unit width	0	90	400	ohms/µm
RC DHFET	DHFET ohmic contact resistance per unit width	40	170	400	ohms/µm
I_{ISO}	Current per unit width between two isolated pads spaced at 20 µm when +2.0V are applied.		31	91	pA/µm

* NOTE: THIS IS THE SHEET RESISTANCE OF THE DHFET N+ IMPLANT

Interconnect Capacitance

The following table gives the nominal values of gate, ohmic, and interconnect metal capacitances. These values were derived from parasitic extractions.

Area Capacitance

SYMBOL	PARAMETER DESCRIPTION	AREA[1]	PERIMETER[2]
ctmbm	cap/unit area of TMT to BMT	0.1265	0.056
ctm	cap/unit area of TMT to substrate	0.060	-
cbm	cap/unit area of BMT to substrate	0.060	-

Line-to-line capacitance[3]

SYMBOL	PARAMETER DESCRIPTION	TMT[1]	BMT[1]
ctml2,cbml2	cap/unit length for 0-2 μm separation	0.104	0.100
ctml5,cbml5	cap/unit length for 2-5 μm separation	0.029	0.027
ctml10,cbml10	cap/unit length for 5-10 μm separation	0.053	0.050
	cap/unit length for >10 μm separation	0.0	0.0

HFET Capacitance

The gate capacitance for the HFET is approximately 2.0 fF/μm.

---

[1] Units: fF/μm^2

[2] Units: fF/μm

[3] as extracted from layout using GOALIE

HFET Device Breakdown Voltages

	MIN	TYP	MAX
EHFET TUB DIODE:			
V_F (at $I_F = 10\ \mu A/\mu m$)		0.78V	
V_R	10V		
I_S (at $V_R = 3$ V)		2.0μA	
EHFET:			
BV_{DGO} (Open Source)	9.0V		
BV_{SGO} (Open Drain)	10V		
V_F (Drain & Source Connected at $I_G = 10\ \mu A/\mu m$)		0.8V	
DHFET:			
BV_{DGO} (Open Source)	10V		
BV_{SGO} (Open Drain)	10V		
V_F (Drain & Source Connected at $I_G = 10\ \mu A/\mu m$)	2.0V		

Definitions:

V_F	Forward Diode Breakdown Voltage
V_R	Reverse Diode Breakdown Voltage
I_S	Reverse Saturation Current
BV_{DGO}	Drain-to-Gate Transistor Breakdown Voltage
BV_{SGO}	Source-to-Gate Transistor Breakdown Voltage

Processing Layer Thicknesses

	TYP. (Å)	Material
Gate Metal	4000	WSi_x
Ohmic Metal	3000	Au
First Dielectric	4000	Silicon Oxynitride
Bottom Metal	6000	Ti/Pt/Au
Second Dielectric	4000	Silicon Oxynitride
Top Metal	8500	Ti/Pt/Au
Passivation	4000	Silicon Oxynitride

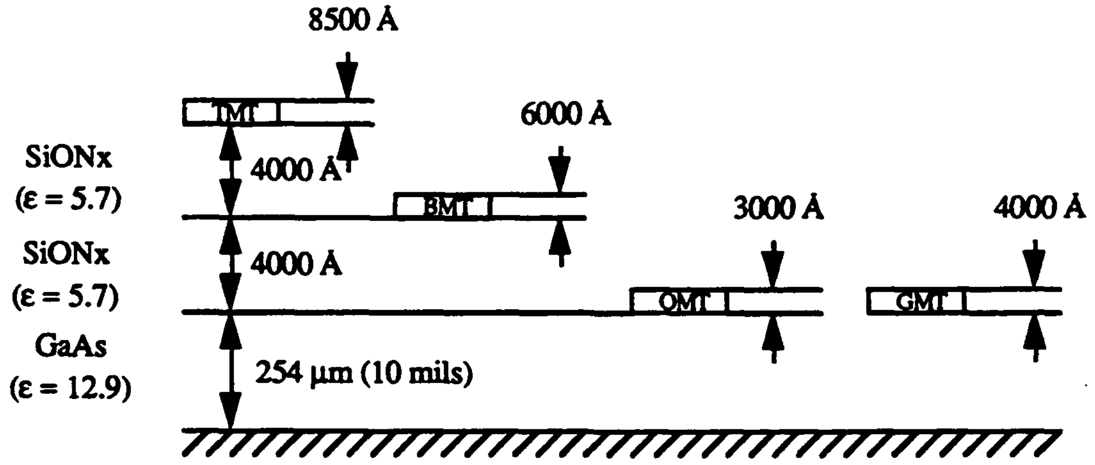

8500 Å
TMT
6000 Å
SiONx
(ε = 5.7)
4000 Å
BMT
3000 Å
4000 Å
SiONx
(ε = 5.7)
4000 Å
OMT
GMT
GaAs
(ε = 12.9)
254 µm (10 mils)

Figure 3.1. Dielectric and metalization thicknesses. (Not to scale.)

Section IV.
2.0 μm Layout Design Rules

Change History

This section describes the 2.0 μm Layout Design Rules for the SARGIC/HFET process. This is the third reissue of the design rules (originally issued June 27, 1987 and updated October 26, 1987, August 3, 1988 and February 15, 1989). This is the first update of the 3.0 Rules and has been designated *Issue 3.01 7/24/90*.

Issue 3.01 represents only a few changes in Issue 3.0 of the design rules. Rule 5.H eliminates the use of ohmic and gate metal for interconnect since these metals lie directly on the GaAs surface. Rule 7.D was added to require a 2 μm overlap of wires connecting to capacitors. Rule 10.A was added to eliminate pull apart when layers are compensated prior to mask fabrication.

Issue 3.0 represents a small change in the design rules issued in August 1988. The overall format of the document has been changed. It now contains a written description of the design rules, Table 4.1 which lists the design rules, and Figures 4.1 to 4.9 which show examples of the design rules. The design rules are grouped under nine major headings and the design rules are now referred to as Rule 1.A, Rule 5.C, etc.

Several changes have been introduced in this issue of the design rules. The drawings in Figures 4.1 through 4.9 have been modified to make the interpretation of the design rules clearer to the designer. Rule 5.G has been more clearly illustrated in Figure 4.5. Note **that TOPMET is not allowed to run over the device drain or source regions.** This restriction may be relaxed in the future. In Rule 5.J, lines can now be oriented 45 degrees with respect to the gate. The minimum distance between VIA1 and VIA2 has been increased (Rule 6.A) to 2.0 μm as shown in Figure 4.6. In Rule 6.A, the spacing between the contact areas of VIA1 and VIA2 has been increased to 2.0 μm. Unacceptable geometries for BOTMET and TOPMET runners have been more clearly defined with the introduction of Rule 6.D. Finally, Rule 8.A specifies the minimum overall resistor length to be 20 μm (previously this length had been reduced to 6.0 μm). This will reduce the effects of contact resistance on the overall resistance.

Design Rule Summary

1. HFET DEVICE GEOMETRY DESIGN RULES

Figure 4.1 illustrates the important dimensions required for HFET layout. The implant isolation level, ISO, defines the device size for both EHFET and DHFET. N^+ is expanded relative to ISOLATION by 0.25 micron in the direction of device width. The gate should extend beyond ISOLATION by 1.0 micron on each end. The final device gate length is 1.0 micron. Source-to-gate and drain-to-gate spacing is 1.0 micron. The source-to-drain spacing is then 3.0 microns. Since the sheet resistance of GATE METAL is large, 4.3 ohm/sq., wide FETs should use an interdigitated, multifingered geometry. All gates must be aligned parallel to each other to eliminate crystallographic effects.

2. DEVICE AND GATE SPACING DESIGN RULES

Figure 4.2 illustrates design rules which relate to device-to-device spacing. The minimum device-to-device spacing is 2.0 microns (as long as Rule 2.C is not violated). Devices which share a common node should overlap OHMIC METAL rather than butt as shown in Figure 4.3. The minimum gate tab area is 2 x 2 square microns with a separation from the device of 1.0 microns.

3. EHFET TUB DESIGN RULES

As previously mentioned, EHFETs (see Figure 4.3) are formed by removal of the top two layers of the MBE grown heterostructure. These features should be expanded 0.75 micron relative to ISOLATION at both ends of the device to prevent parasitic D-FET formation. The EHFET tub should be pulled back 0.75 micron along the width of the device to prevent an EHFET from being formed in the lower DHFET.

4. EHFET TUB DIODE DESIGN RULES

Diodes are formed in an EHFET tub using the same gate material used for HFETs (see Figure 4.4). The minimum diode width is be 3.0 microns and the minimum contact area of the Schottky diode is 2 x 3 square microns. BOTMET and VIA1 should be pulled-back 1.0 micron from OHMIC METAL to keep the metal-to-metal spacing at 2.0 microns thus conserving metallization design rules (see Figure 4.5).

5. INTRALEVEL VIA AND INTERCONNECT DESIGN RULES

Figure 4.5 shows the via and metalization design rules. The contact area or via size should be 1.5 x 1.5 square micrometers. BOTMET and TOPMET should extend 0.25 micron beyond the contact area. All TOPMET connections to the device must be made through BOTMET. The minimum spacing from VIA1 to VIA1 or VIA2 to VIA2 is 1.5 micron. BOTMET and TOPMET line and space rules are 2.0 and 2.0 micron. Further, BOTMET and TOPMET should not cross the active area of a device except in the case of BOTMET making contact to the ohmic drain and source regions. Topmet may be run over the gate tab but only if it *completely* covers the VIA1 contact. Ohmic and gate metal must not be used for interconnect since they lie directly on the GaAs surface.

6. INTERLEVEL VIA AND INTERCONNECT DESIGN RULES

Figure 4.6 shows the via and metalization design rules between TOPMET and BOTMET. The minimum spacing between VIA1 and VIA2 is 2.0 microns. The minimum spacing between parallel TOPMET and BOTMET lines is 0.5 micron. TOPMET is allowed to run over BOTMET only if there is no offset between the two lines. Otherwise TOPMET and BOTMET should be separated by at least 0.5 micron. Several geometries are not allowed such as partially overlapping or abutting TOPMET and BOTMET lines.

7. CAPACITOR DESIGN RULES

Figure 4.7 shows the metal-insulator-metal capacitor design rules. The second dielectric layer serves as the capacitor insulating layer. The minimum capacitor area is 2 x 2 square microns. BOTMET extends 1.0 micron beyond TOPMET. Connecting wires should overlap the capacitor edge by 2.0 microns.

8. IMPLANT RESISTOR DESIGN RULES

Figure 4.8 illustrates the layout of an N^+ implanted resistor. The resistor length should be greater than 20 microns to prevent contact resistance from dominating the implant resistor value. The minimum contact areas at the ends of the resistor are 2 x 2 square microns. The N^+ isolation is extended beyond the edge of the resistor by 0.25 micron. The sheet resistance of N^+ is typically 370 ohm/sq but can vary widely.

9. BONDING PAD DESIGN RULES

Figure 4.9 shows the PASSIVATION design rules as applied to bonding pad layout. Pads should be 100 x 100 square microns defined by TOPMET with a 2.5 micron extension beyond PASSIVATION opening. Spacing between pads, referenced to TOPMET, is 25 microns. Dicing lanes should be 120 microns with a minimum pad edge to dicing lane spacing of 25 microns.

10. GENERAL LAYOUT DETAILS

Figure 4.10 illustrates general layout rules that should be followed. All layers should overlap individual elements by 1.0 µm to prevent pull aparts during premask compensation.

TABLE 4.1

GaAs SARGIC/SDHT 2.0 MICRON DESIGN RULES

1.	HFET DEVICE GEOMETRY DESIGN RULES	Figure 4.1
A.	Minimum Device Width	3.0 μm
B.	Minimum Source and Drain	2.0 μm
C.	Minimum Gate Length	1.0 μm
D.	Minimum Gate Extension Beyond Device	1.0 μm
E.	Minimum Ohmic to Gate Metal Spacing	1.0 μm
F.	Minimum N$^+$ Extension Beyond Device	0.25 μm
G.	All Gates Must be Oriented In A Single Direction	

2.	DEVICE AND GATE SPACING DESIGN RULES	Figure 4.2
A.	Minimum Device to Device Spacing	2.0 μm
B.	Minimum Device to Gate Tab Spacing	1.0 μm
C.	Minimum Gate to Gate Spacing	2.0 μm
D.	Minimum Gate Tab Width	2.0 μm
E.	Minimum Gate Tab Length	2.0 μm

3.	EHFET TUB DESIGN RULES	Figure 4.3
A.	Minimum EHFET Tub Extension	0.75 μm
B.	Minimum EHFET Tub Pull-back	0.75 μm
C.	Minimum Spacing Between E-FET and D-FET Gates with Shared Source	4.0 μm

4.	EHFET TUB DIODE DESIGN RULES	Figure 4.4
A.	Minimum Diode Width	3.0 μm
B.	Minimum Diode Ohmic Contact Length	3.0 μm
C.	Minimum Gate to Ohmic Spacing	1.0 μm
D.	Minimum N$^+$ Extension Beyond Device	0.25 μm
E.	Minimum Botmet Pull-Back From Ohmic	1.0 μm
F.	Minimum Gate Contact Width	3.0 μm
G.	Minimum Gate Contact Length	2.0 μm
H.	Minimum EHFET Tub Extension Beyond Diode Edge	0.75 μm

Table 4.1 Con't.

5. INTRALEVEL VIA AND INTERCONNECT DESIGN RULES	Figure 4.5
A. Via Contact Area	1.5 x 1.5 µm
B. Minimum Contact Spacing	1.5 µm
C. Minimum Metal Extension Beyond Contact	0.25 µm
D. Minimum Metal Width	2.0 µm
E. Minimum Metal Spacing	2.0 µm
F. Minimum Botmet to Device Channel Spacing	1.0 µm
G. Minimum Topmet to Device Spacing	1.0 µm
H. Gate and Ohmic Should Not be Used for Interconnect	
I. No Botmet or Topmet Allowed over Device Gate.	
J. All Interconnect Must Be Oriented 0, 45 or 90 Degrees with Respect to Gate.	

6. INTERLEVEL VIA AND INTERCONNECT DESIGN RULES	Figure 4.6
A. Minimum Spacing Between VIA1 and VIA2	2.0 µm
B. Minimum Spacing Between Parallel TOPMET and BOTMET Runners	0.5 µm
C. Parallel runners may overlap only when there is no lateral offset.	
D. Unacceptable Geometries.	

7. CAPACITOR DESIGN RULES	Figure 4.7
A. Minimum Capacitor Length	2.0 µm
B. Minimum Capacitor Width	2.0 µm
C. Minimum Botmet Extension Beyond Topmet	1.0 µm
D. Minimum Topmet and Botmet Extension Beyond Botmet	2.0 µm

8. IMPLANT RESISTOR DESIGN RULES	Figure 4.8
A. Minimum Overall Resistor Length	20 µm
B. Minimum Resistor Width	2.0 µm
C. Minimum Contact Area (C x C)	2 µm x 2 µm
D. Minimum N^+ Extension Beyond Resistor	0.25 µm

Table 4.1 Con't.

9. BONDING PAD DESIGN RULES		Figure 4.9
A.	Minimum Pad Size (A x A)	100 µm
B.	Minimum Pad to Metal Spacing	25 µm
C.	Minimum Pad to Pad Spacing	25 µm
D.	Minimum Metal Extension Beyond Via2 Passivation	2.5 µm
E.	Minimum Dicing Lane Width	120 µm
F.	Minimum Spacing from Pad to Edge of Dicing Lane	25 µm

10. LAYOUT DETAILS		Figure 4.10
A.	Minimum Layer Overlap Any Connecting Layers	1.0 µm

Figure 4.1. HFET DEVICE GEOMETRY DESIGN RULES

A. Minimum Device Width 3.0 µm

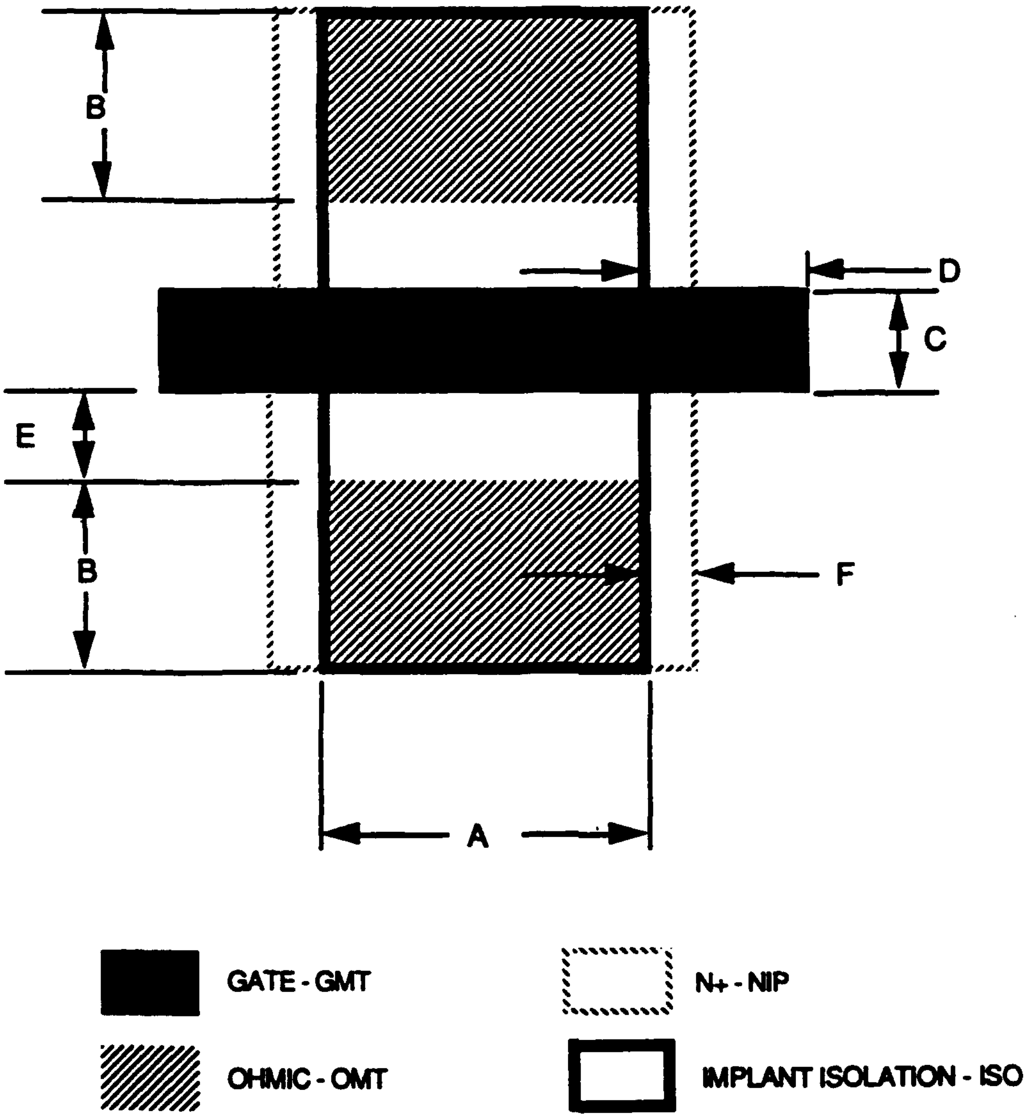

B
D
C
E
B
F
A
GATE - GMT
N+ - NIP
OHMIC - OMT
IMPLANT ISOLATION - ISO

Figure 4.2. DEVICE AND GATE SPACING DESIGN RULES

A.	Minimum Device to Device Spacing	2.0 µm
B.	Minimum Device to Gate Tab Spacing	1.0 µm
C.	Minimum Gate to Gate Spacing	2.0 µm
D.	Minimum Gate Tab Width	2.0 µm
E.	Minimum Gate Tab Length	2.0 µm

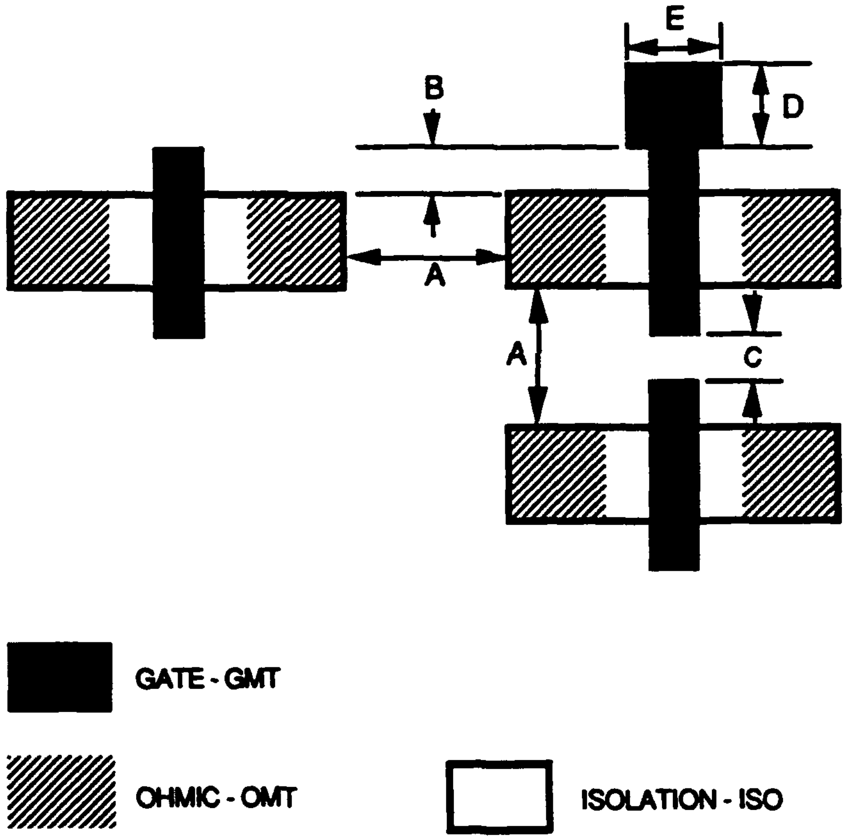

E
B
D
A
A
C
GATE - GMT
OHMIC - OMT
ISOLATION - ISO

Figure 4.3. EHFET TUB DESIGN RULES

A.	Minimum EHFET Tub Extension	0.75 µm
B.	Minimum EHFET Tub Pull-back	0.75 µm
C.	Minimum Spacing Between E-FET and D-FET Gates with Shared Source	4.0 µm

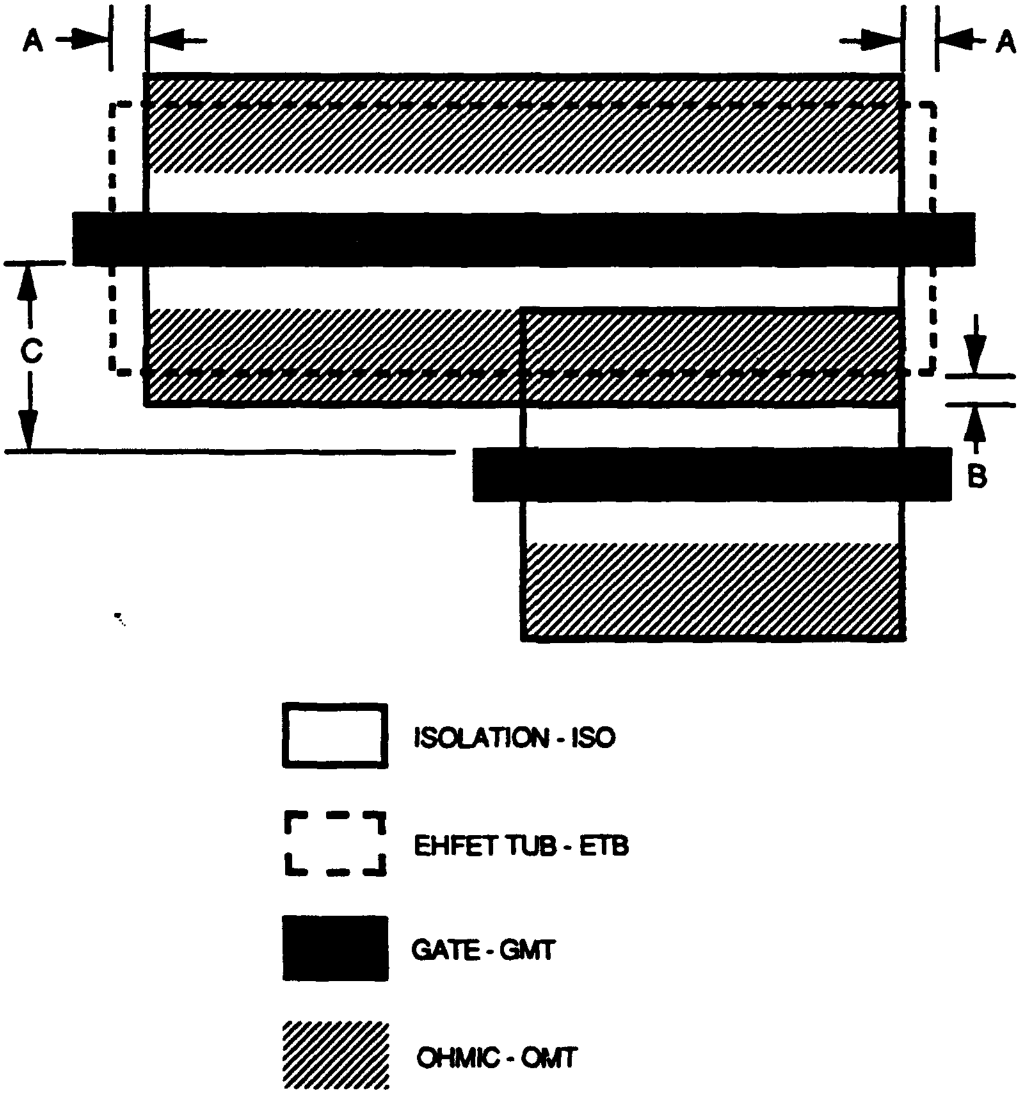

A
A
C
B
ISOLATION - ISO
EHFET TUB - ETB
GATE - GMT
OHMIC - OMT

Figure 4.4. EHFET TUB DIODE DESIGN RULES

A.	Minimum Diode Width	3.0 µm
B.	Minimum Diode Ohmic Contact Length	3.0 µm
C.	Minimum Gate to Ohmic Spacing	1.0 µm
D.	Minimum N^+ Extension Beyond Device	0.25 µm
E.	Minimum Botmet Pull-Back From Ohmic	1.0 µm
F.	Minimum Gate Contact Width	3.0 µm
G.	Minimum Gate Contact Length	2.0 µm
H.	Minimum EHFET Tub Extension Beyond Diode Edge	0.75 µm

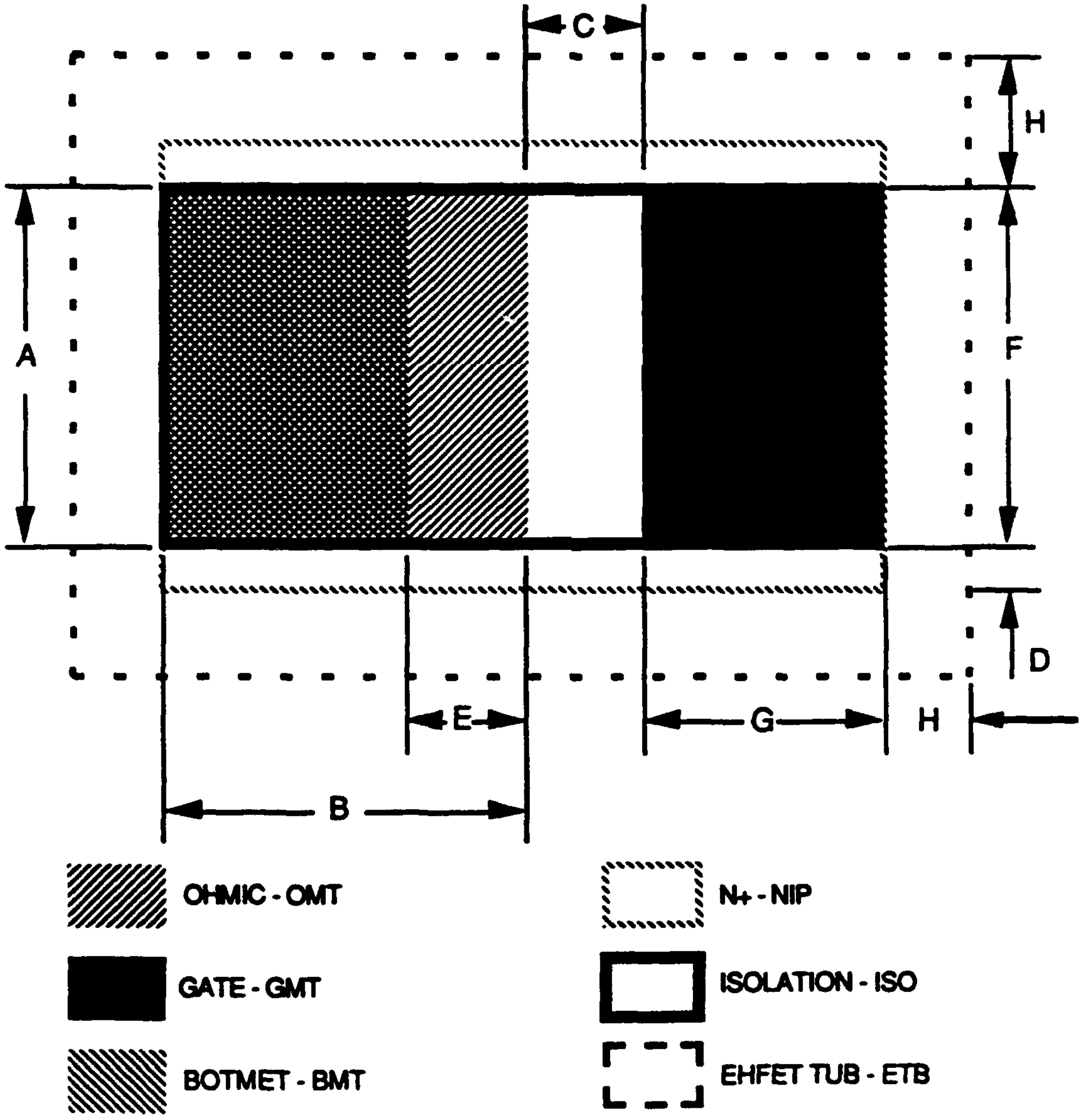

C
H
A
F
D
E
G
H
B
OHMIC - OMT
GATE - GMT
BOTMET - BMT
N+ - NIP
ISOLATION - ISO
EHFET TUB - ETB

Figure 4.5. INTRALEVEL VIA AND INTERCONNECT DESIGN RULES

A.	Via Contact Area	1.5 x 1.5 µm
B.	Minimum Contact Spacing	1.5 µm
C.	Minimum Metal Extension Beyond Contact	0.25 µm
D.	Minimum Metal Width	2.0 µm
E.	Minimum Metal Spacing	2.0 µm
F.	Minimum Botmet to Device Channel Spacing	1.0 µm
G.	Minimum Topmet to Device Spacing	1.0 µm
H.	Gate and ohmic should not be used for interconnect	
I.	No Botmet or Topmet Allowed over Device Gate.	
J.	All Interconnect Must Be Oriented 0, 45 or 90 Degrees with Respect to Gate.	

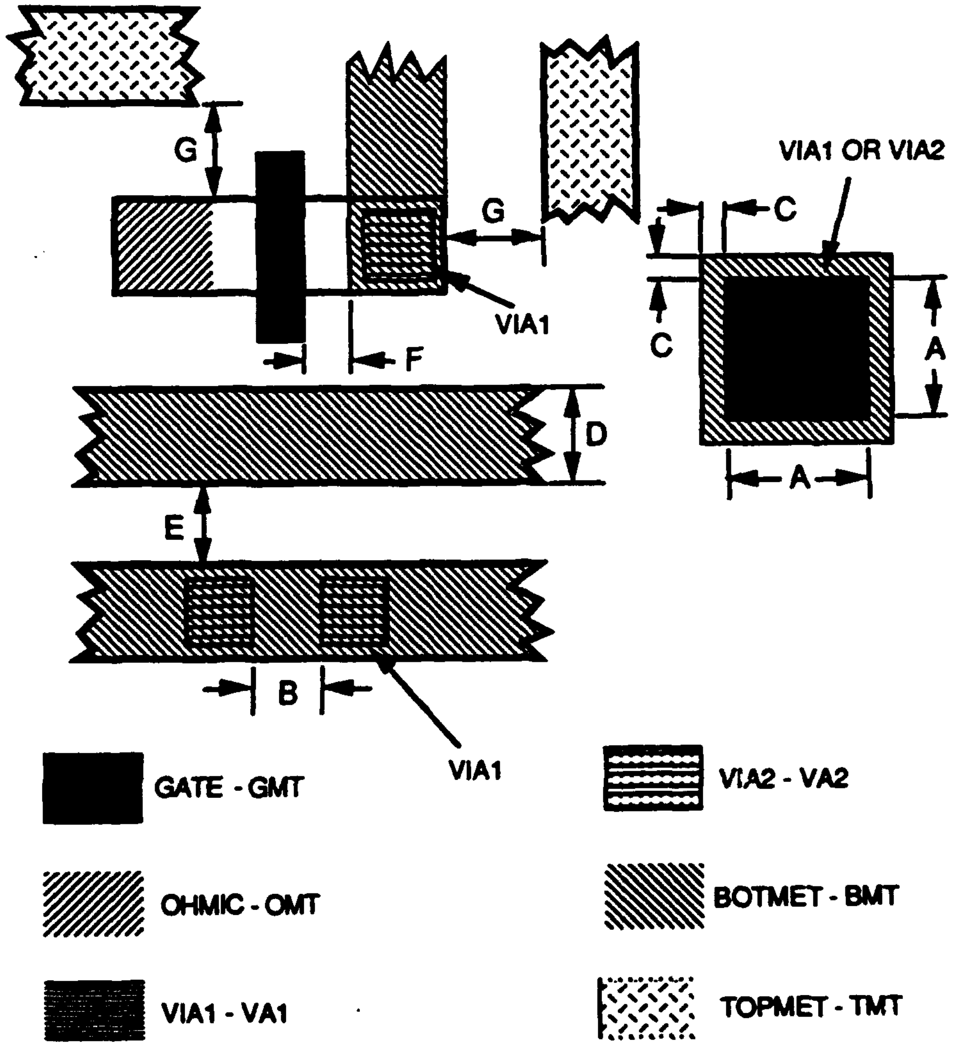

G
G
VIA1 OR VIA2
C
C
VIA1
F
A
D
A
E
B
VIA1
GATE - GMT
VIA2 - VA2
OHMIC - OMT
BOTMET - BMT
VIA1 - VA1
TOPMET - TMT

Figure 4.6. INTERLEVEL VIA AND INTERCONNECT DESIGN RULES

A.	Minimum Spacing Between VIA1 and VIA2	2.0 µm
B.	Minimum Spacing Between Parallel TOPMET and BOTMET Runners	0.5 µm

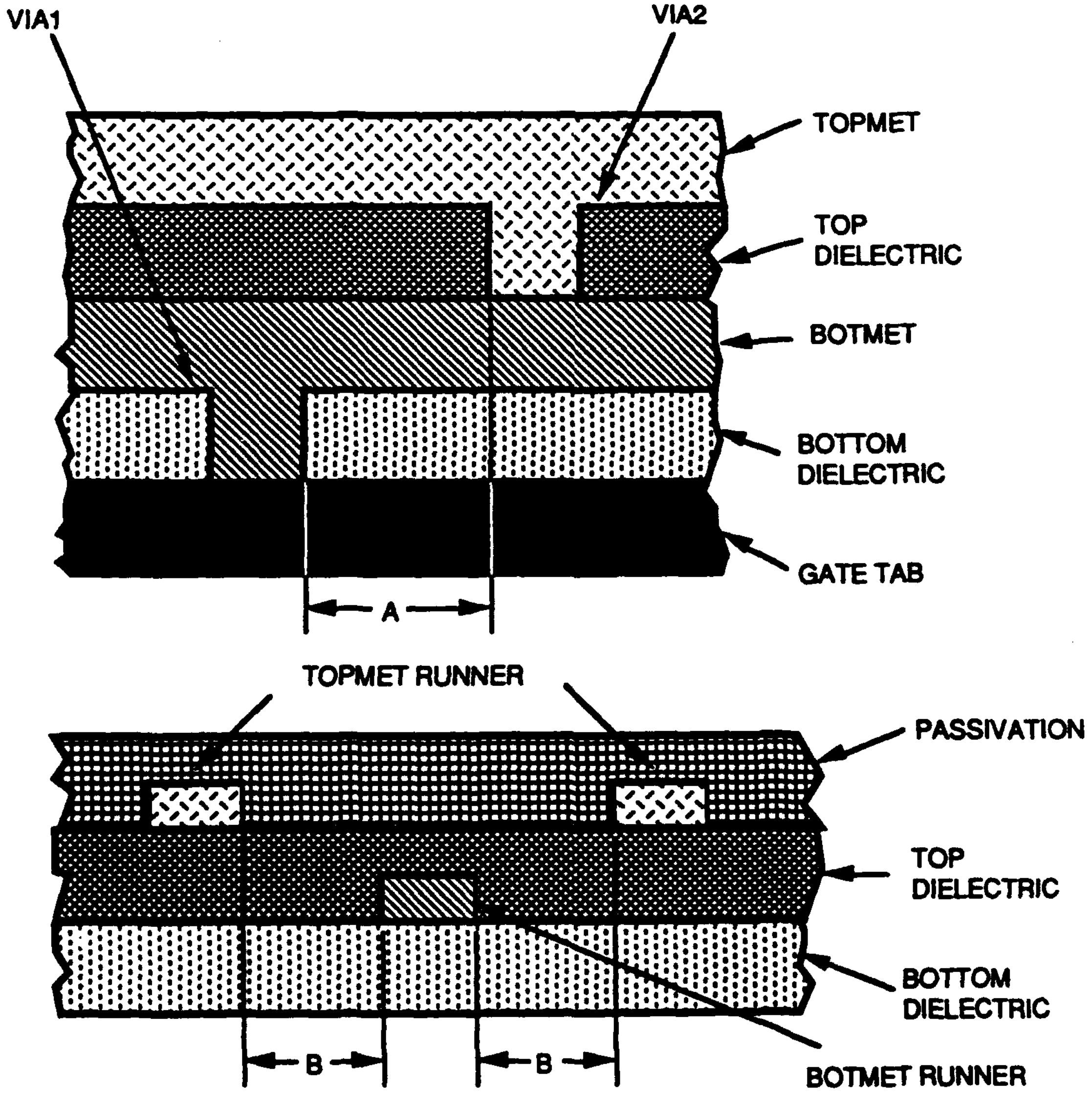
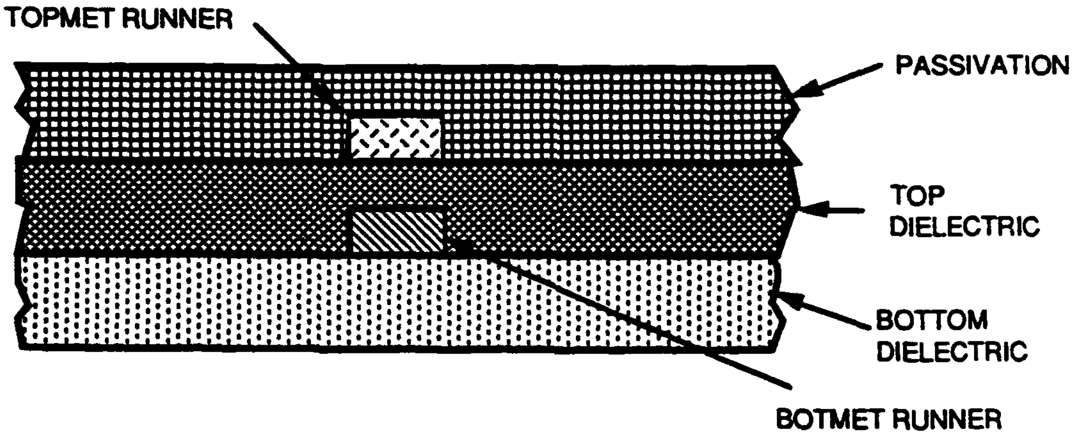

VIA1
VIA2
TOPMET
TOP DIELECTRIC
BOTMET
BOTTOM DIELECTRIC
GATE TAB
A
TOPMET RUNNER
PASSIVATION
TOP DIELECTRIC
BOTTOM DIELECTRIC
B
B
BOTMET RUNNER

Figure 4.6. Con't.

C. Parallel runners may overlap only when there is no lateral offset.
D. Unacceptable Geometries.

C. Acceptable Geometries


TOPMET RUNNER
PASSIVATION
TOP DIELECTRIC
BOTTOM DIELECTRIC
BOTMET RUNNER

D. Unacceptable Geometries

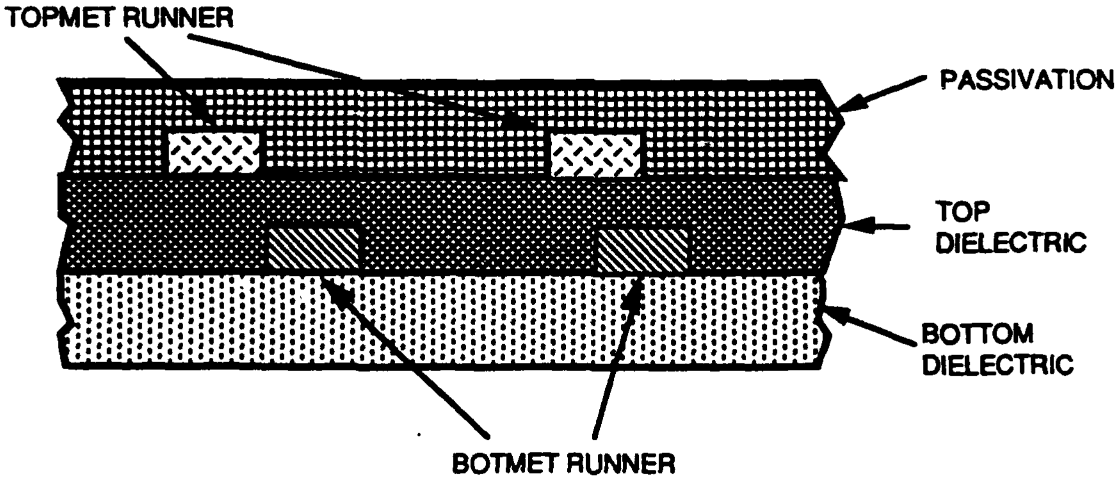

TOPMET RUNNER
PASSIVATION
TOP DIELECTRIC
BOTTOM DIELECTRIC
BOTMET RUNNER

Figure 4.7. CAPACITOR DESIGN RULES

A.	Minimum Capacitor Length	2.0 µm
B.	Minimum Capacitor Width	2.0 µm
C.	Minimum Botmet Extension Beyond Topmet	1.0 µm
D.	Minimum Topmet and Botmet Extension Beyond Botmet	2.0 µm

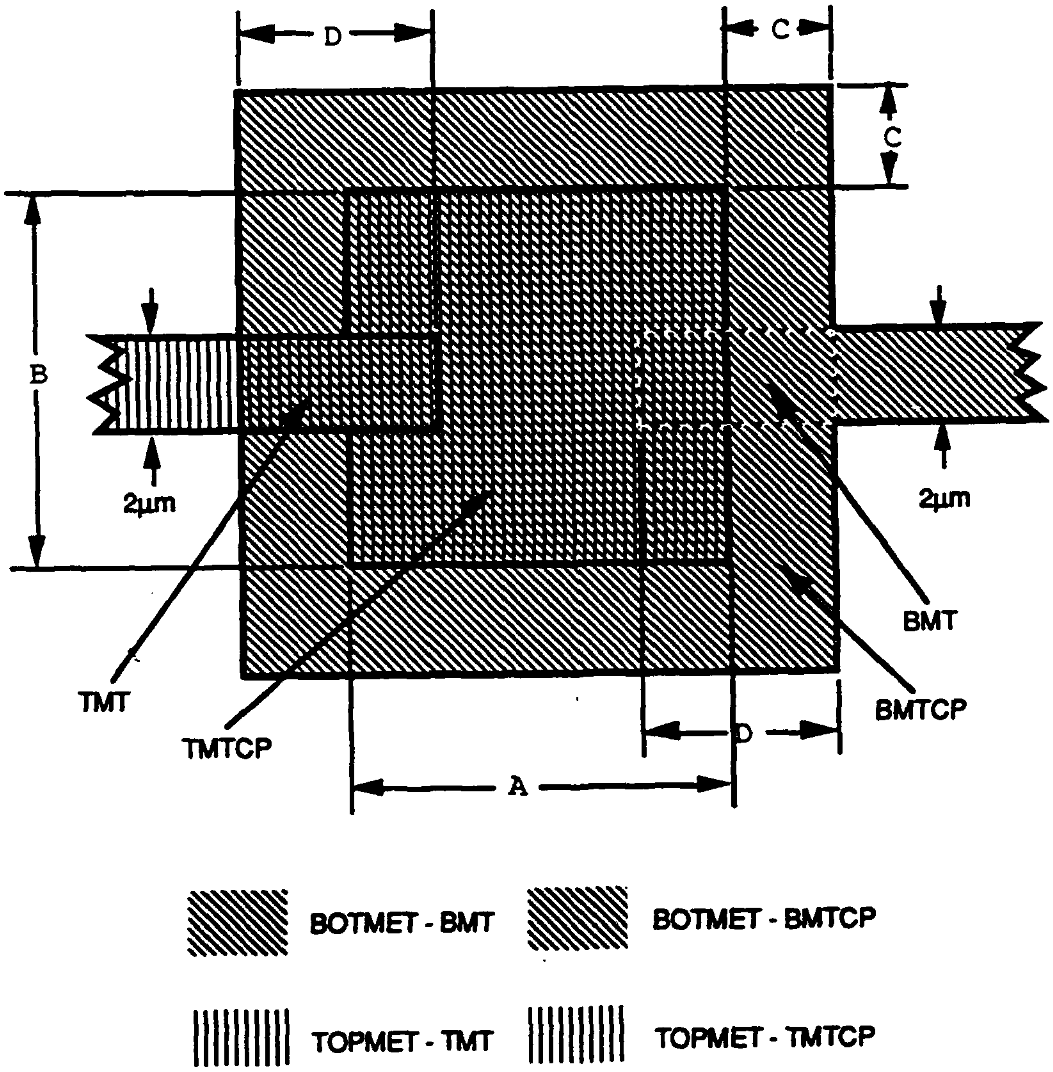

D
C
C
B
2µm
2µm
BMT
TMT
BMTCP
TMTCP
D
A
BOTMET - BMT
BOTMET - BMTCP
TOPMET - TMT
TOPMET - TMTCP

Figure 4.8. *IMPLANT RESISTOR DESIGN RULES*

A.	Minimum Overall Resistor Length	20 μm
B.	Minimum Resistor Width	2.0 μm
C.	Minimum Contact Area (C x C)	2 μm x 2 μm
D.	Minimum N^+ Extension Beyond Resistor	0.25 μm

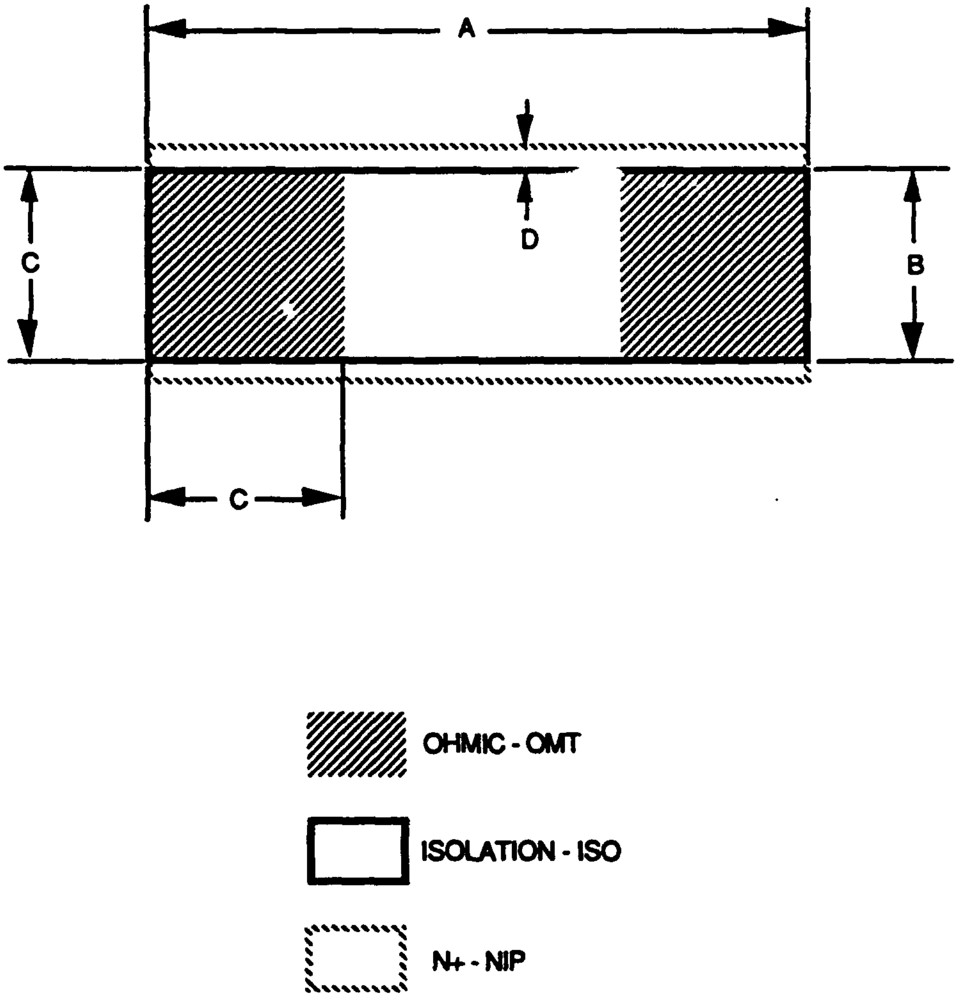

A
D
C
B
C
OHMIC - OMT
ISOLATION - ISO
N+ - NIP

Figure 4.9. BONDING PAD DESIGN RULES

A.	Minimum Pad Size (A x A)	100 µm x 100 µm
B.	Minimum Pad to Metal Spacing	25 µm
C.	Minimum Pad to Pad Spacing	25 µm
D.	Minimum Metal Extension Beyond Via2 and Passivation	2.5 µm
E.	Minimum Dicing Lane Width	120 µm
F.	Minimum Spacing from Pad to Edge of Dicing Lane	25 µm

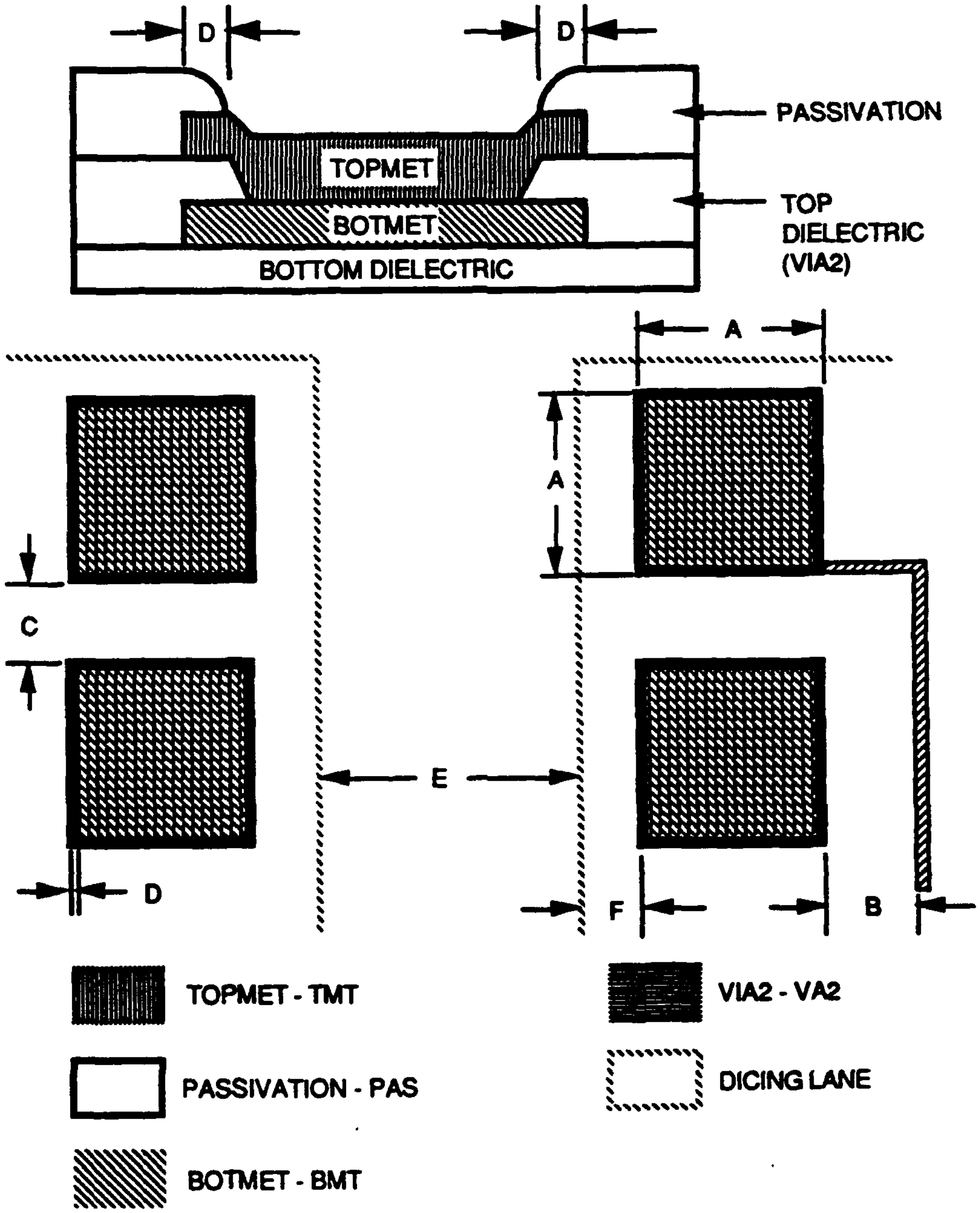
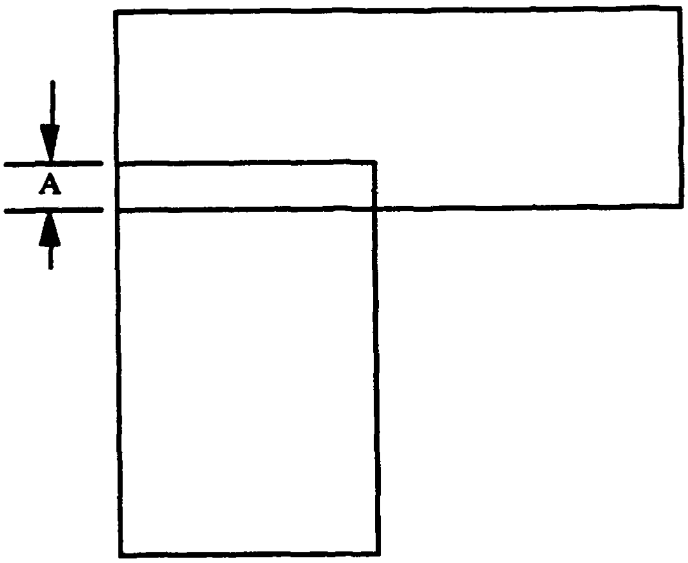

D
D
PASSIVATION
TOPMET
BOTMET
TOP DIELECTRIC (VIA2)
BOTTOM DIELECTRIC
A
A
C
E
D
F
B
TOPMET - TMT
VIA2 - VA2
PASSIVATION - PAS
DICING LANE
BOTMET - BMT

Figure 4.10. GENERAL LAYOUT RULES

A. Minimum Overlap Any Connecting Layers 1.0 µm



Section V.
Device Terminal Characteristics

Introduction

This section contains the nominal terminal characteristics of HFETs and Schottky diodes at 25 and 125°C. The characteristics are modeled using AT&T's GADVICE circuit simulator and given in graphical format. They include current/voltage (I/V) and capacitance/voltage (C/V) data. The GADVICE models parameters were extracted from measured HFET and diode characteristics and fitted to the measurements.

Presently all integrated circuits including the DARPA standard and AT&T macrocell libraries are designed in the SARGIC/HFET process. Circuit functionality is verified using ADVICE. The DC and transient response of circuits is simulated using the ADVICE circuit simulator and correlated with the measured response.

All simulations at present use the nominal (c25 and c125), high enhancement/depletion (E/D) current ratio (h25 and h125) and low E/D current ratio (l25 and l125) device models. These models have been extracted for enhancement and depletion HFETs and Schottky diodes. The model is named "SargicS.15." Other parameters will be added to cover temperatures other than 25°C and 125°C.

HSPICE circuit simulator model parameters for the SARGIC/HFET process are available as part of the HCAD/Cadence Design Environment.

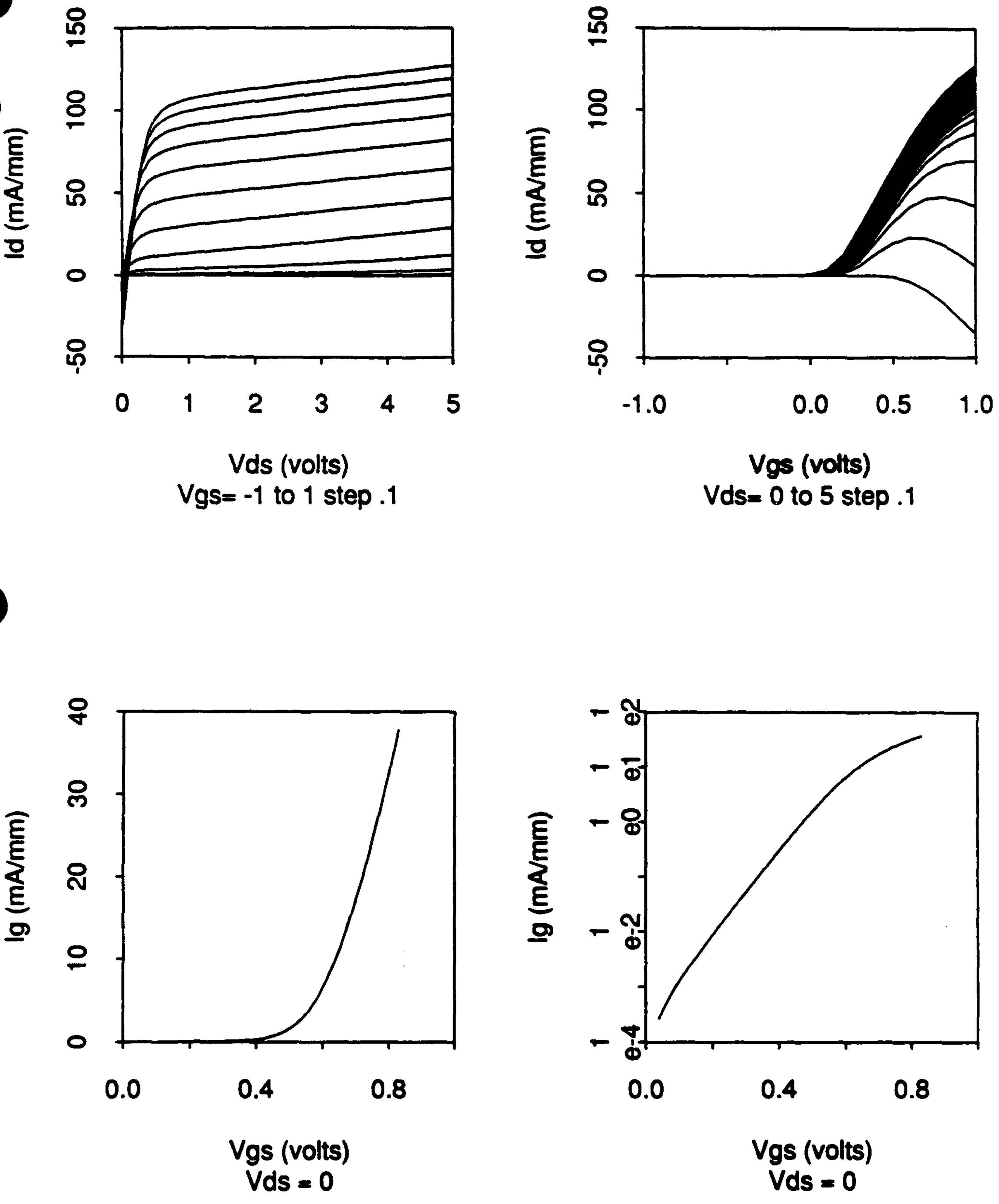


Figure 5.1. DC Characteristics of Nominal 20 μm EHFET at 25°C.

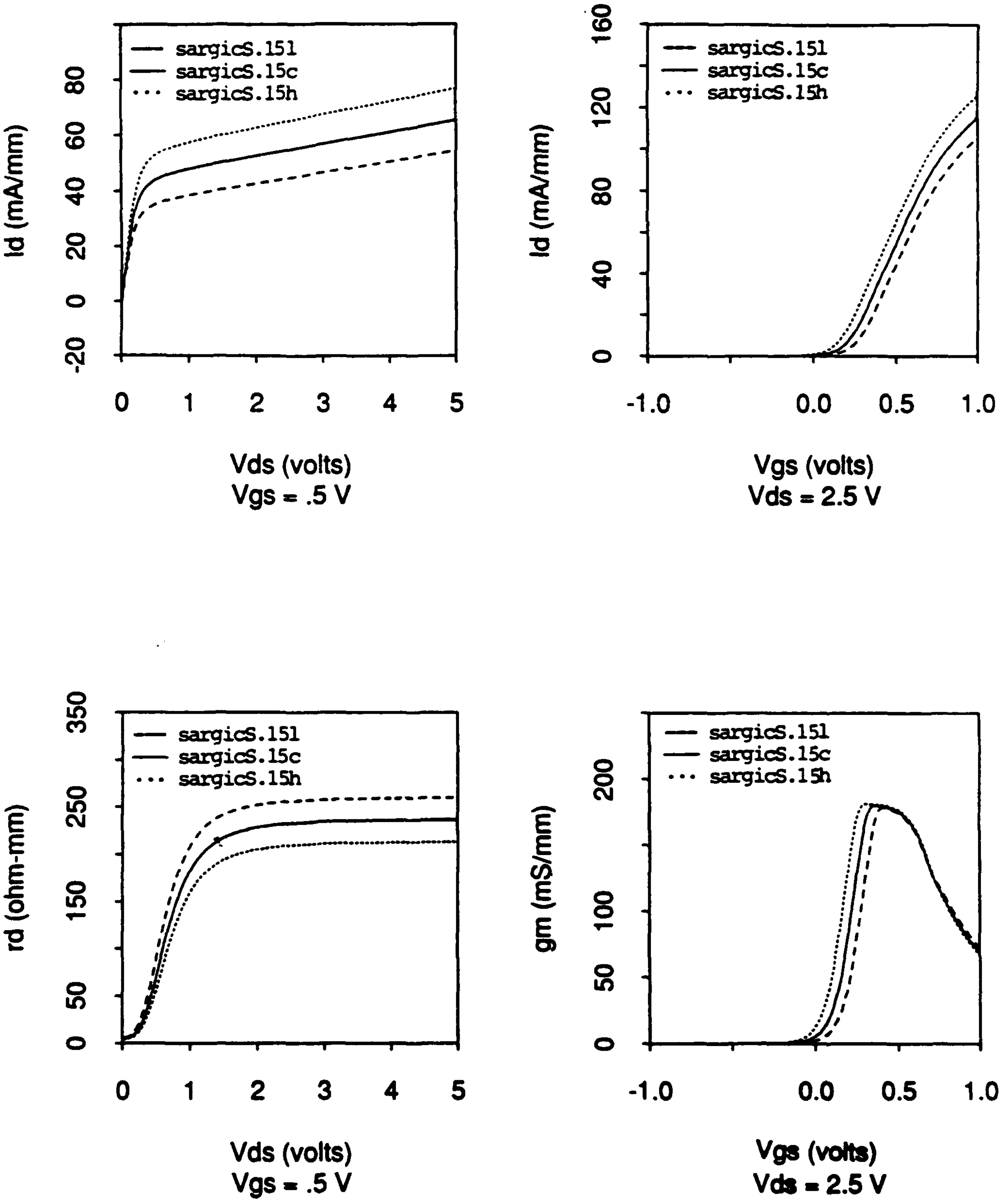


Figure 5.2. DC Characteristics of Nominal, High and Low Current 20 μm EHFET at 25°C.

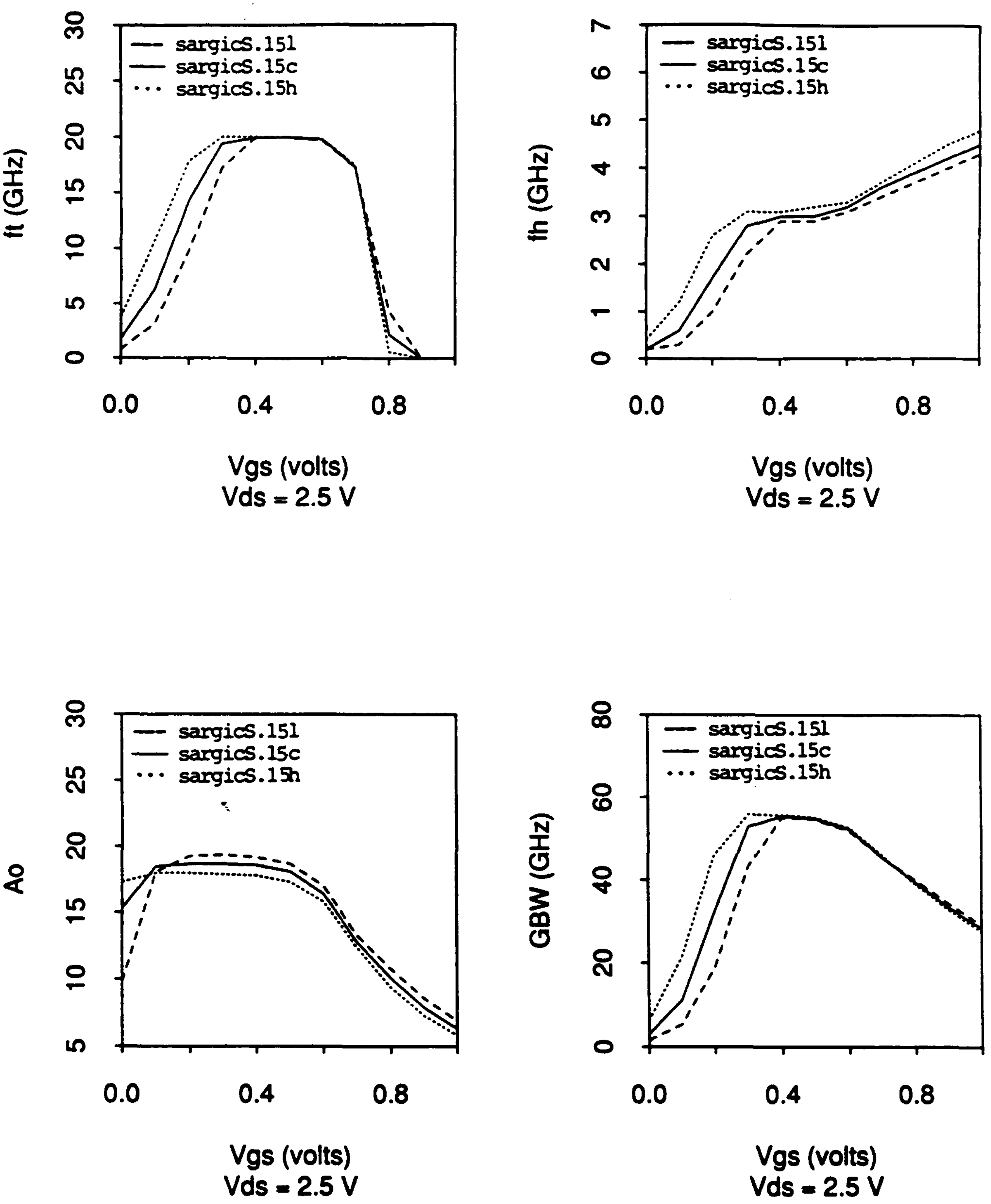


Figure 5.3. RF Characteristics of Nominal, High and Low Current 20 μm EHFET at 25°C.

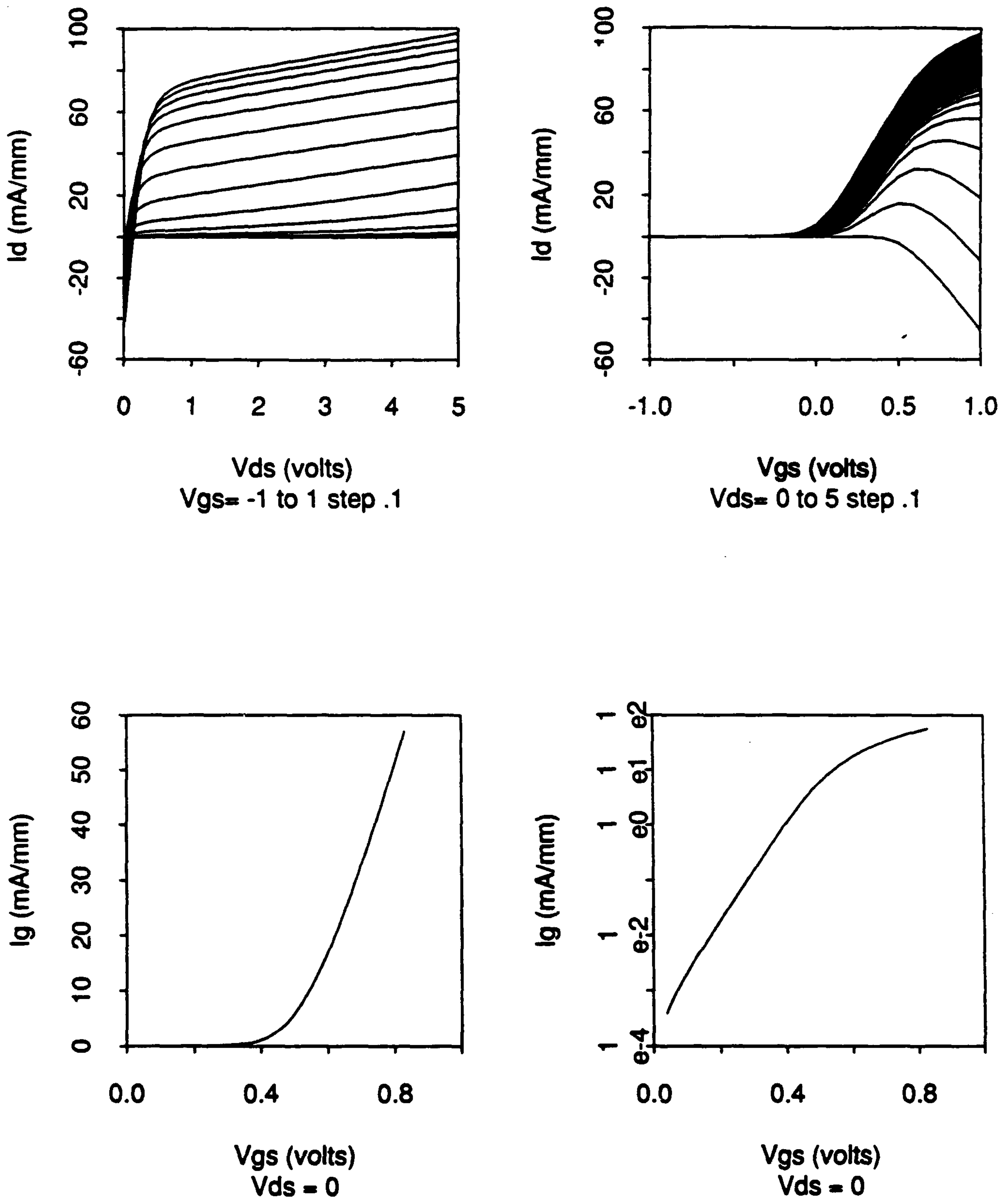


Figure 5.4. DC Characteristics of Nominal 20 µm EHFET at 125°C.

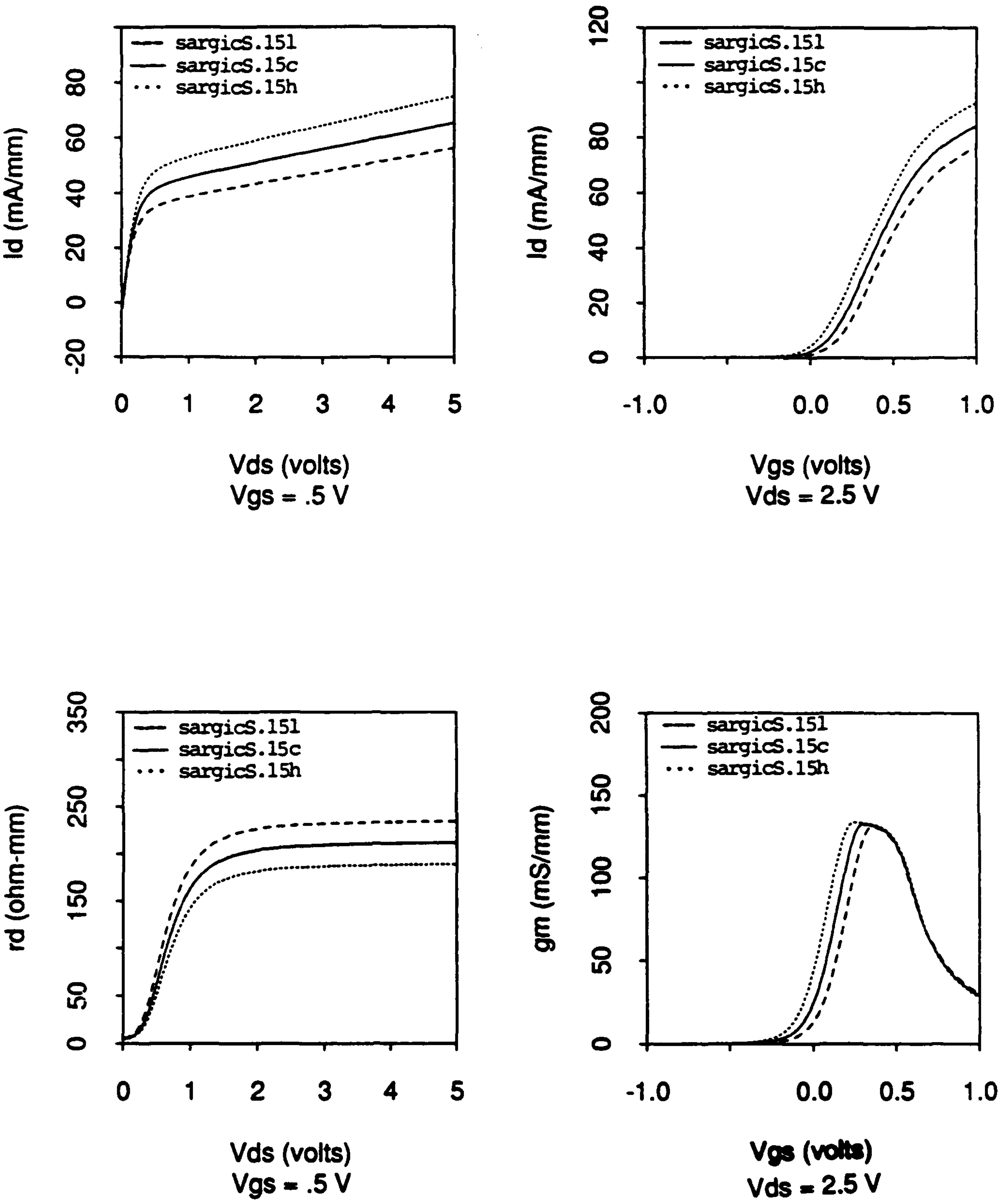


Figure 5.5. DC Characteristics of Nominal, High and Low Current 20 μm EHFET at 125°C.

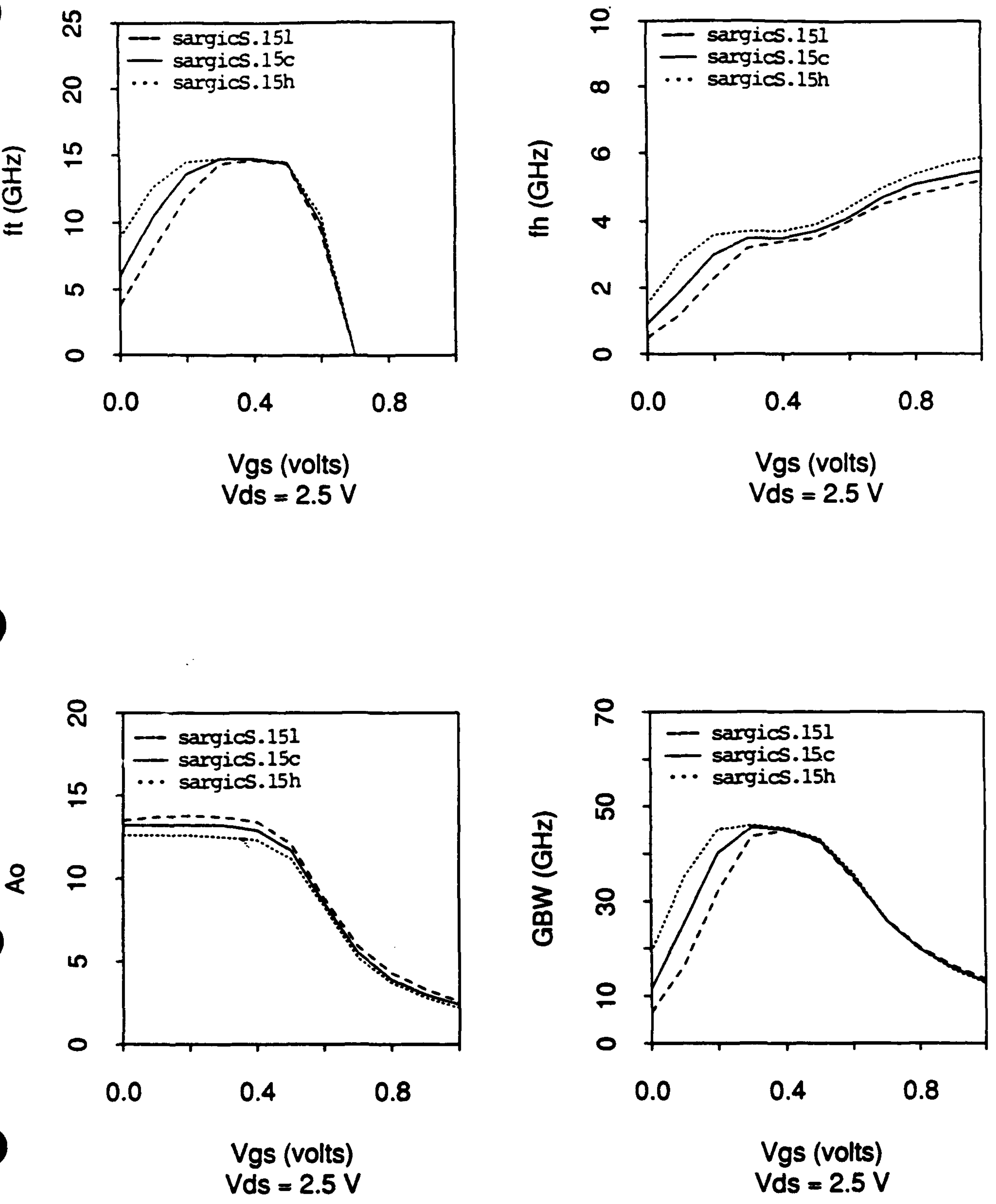


Figure 5.6. RF Characteristics of Nominal, High and Low Current 20 μm EHFET at 125°C.

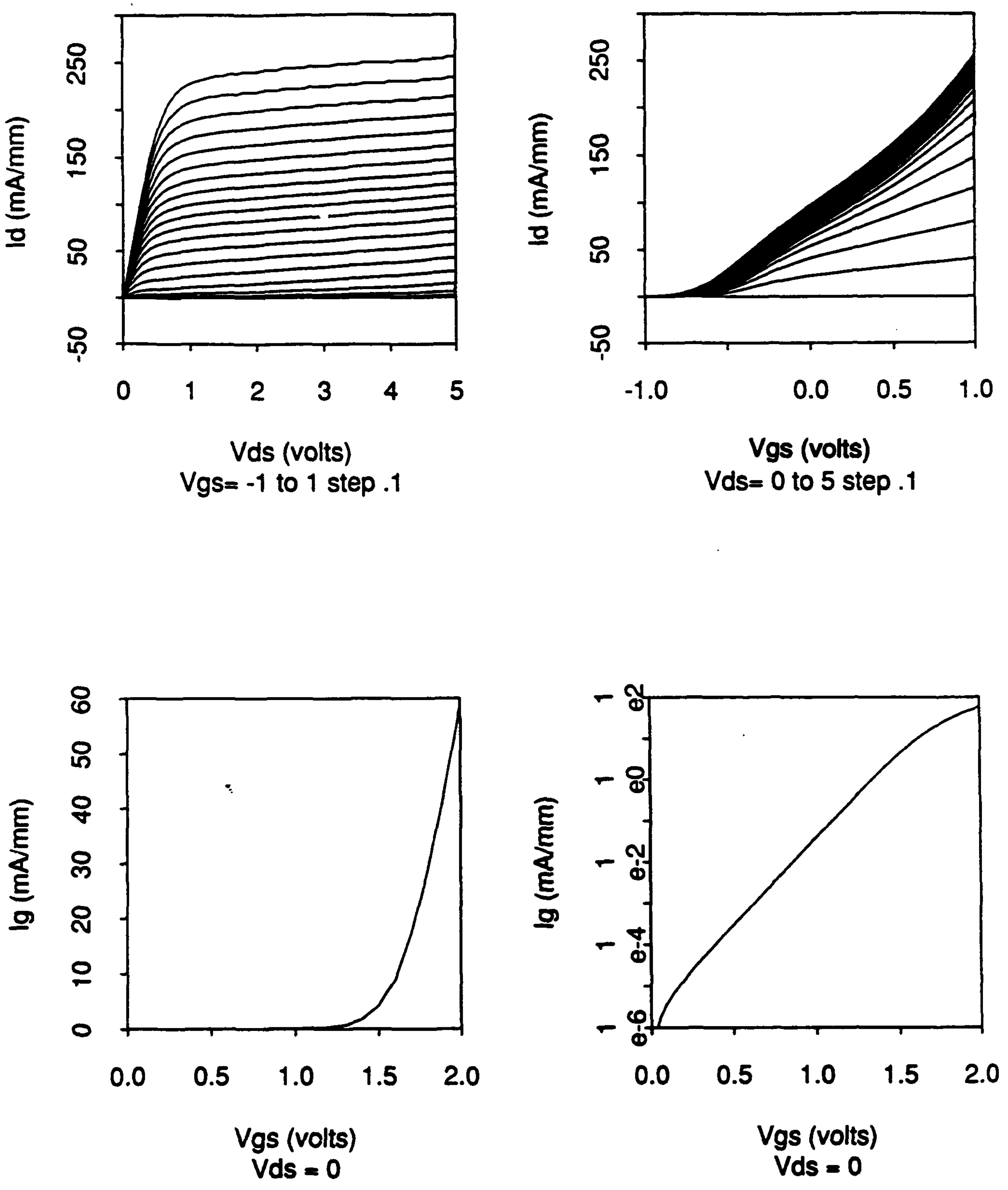


Figure 5.7. DC Characteristics of Nominal 20 μm DHFET at 25°C.

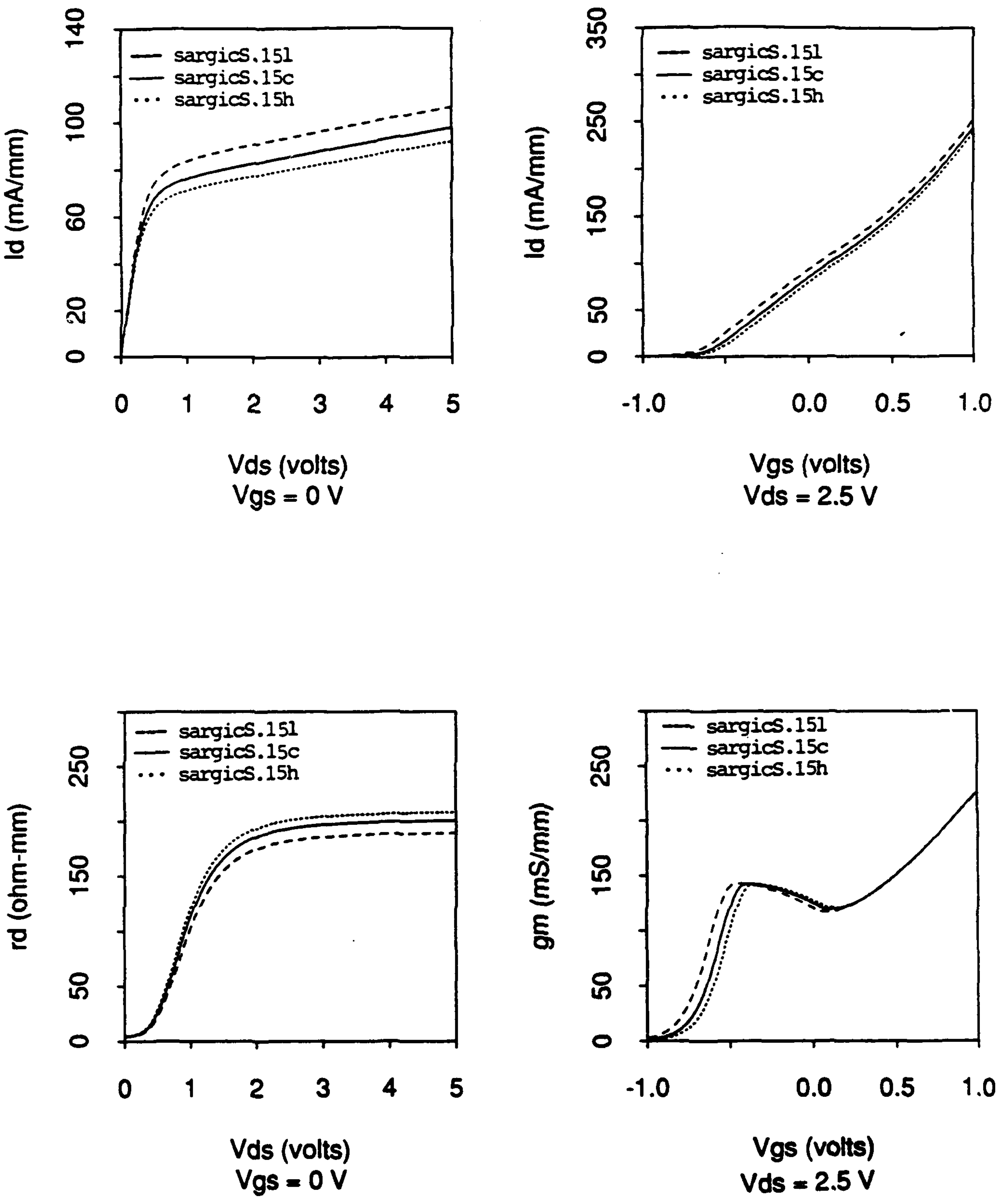


Figure 5.8. DC Characteristics of Nominal, High and Low Current 20 μm DHFET at 25°C.

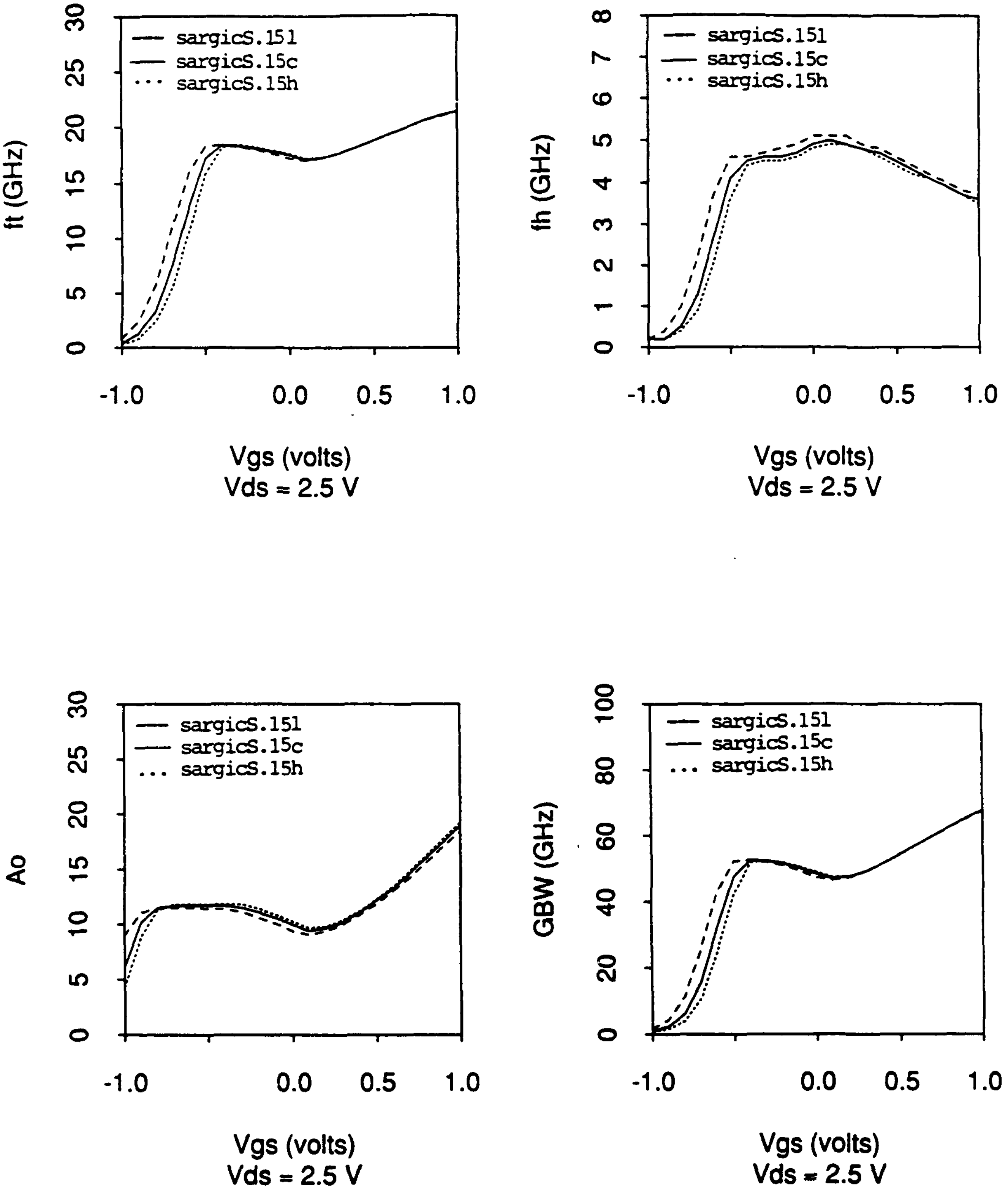


Figure 5.9. RF Characteristics of Nominal, High and Low Current 20 μm DHFET at 25°C.

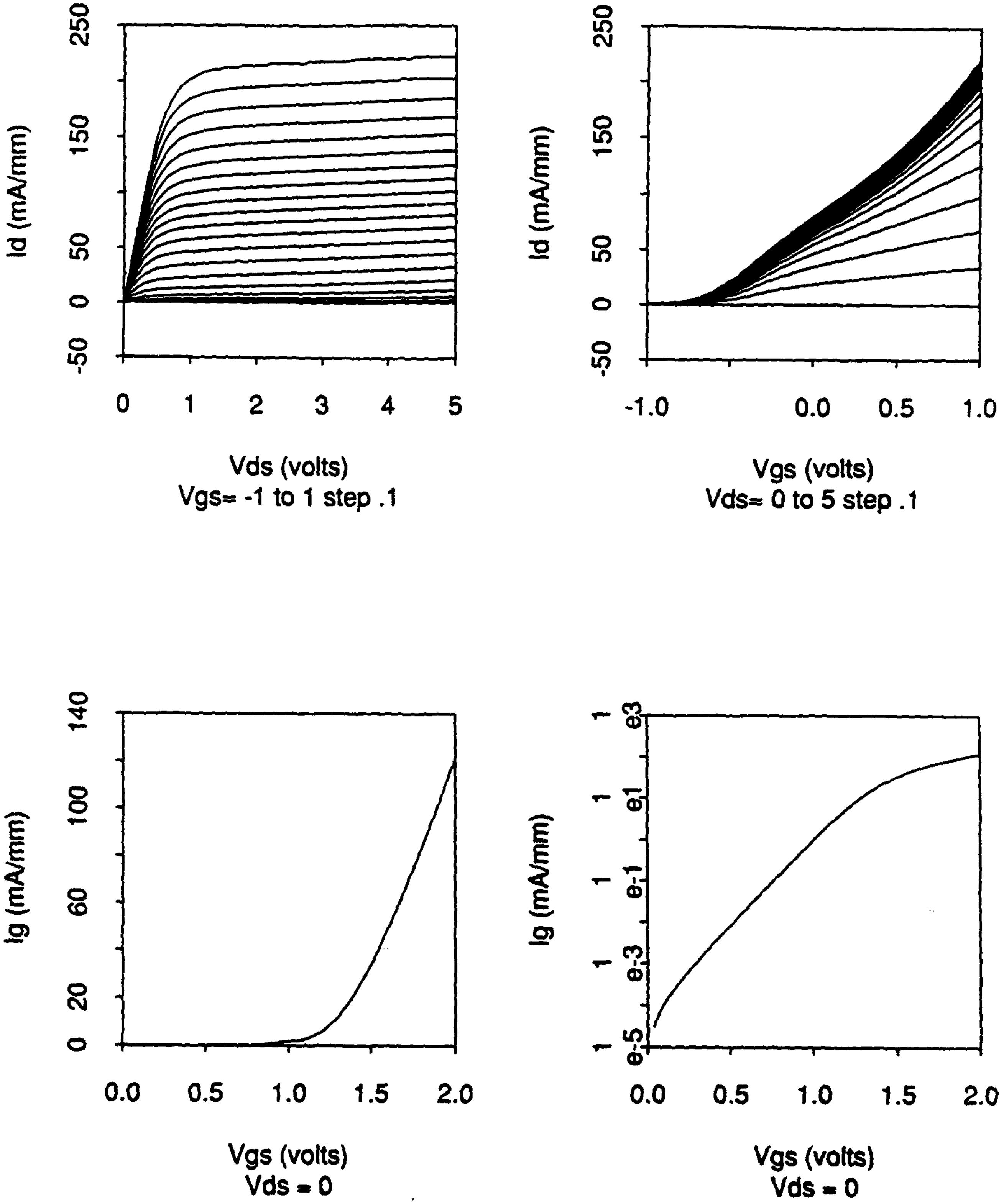


Figure 5.10. DC Characteristics of Nominal 20 μm DHFET at 125°C.

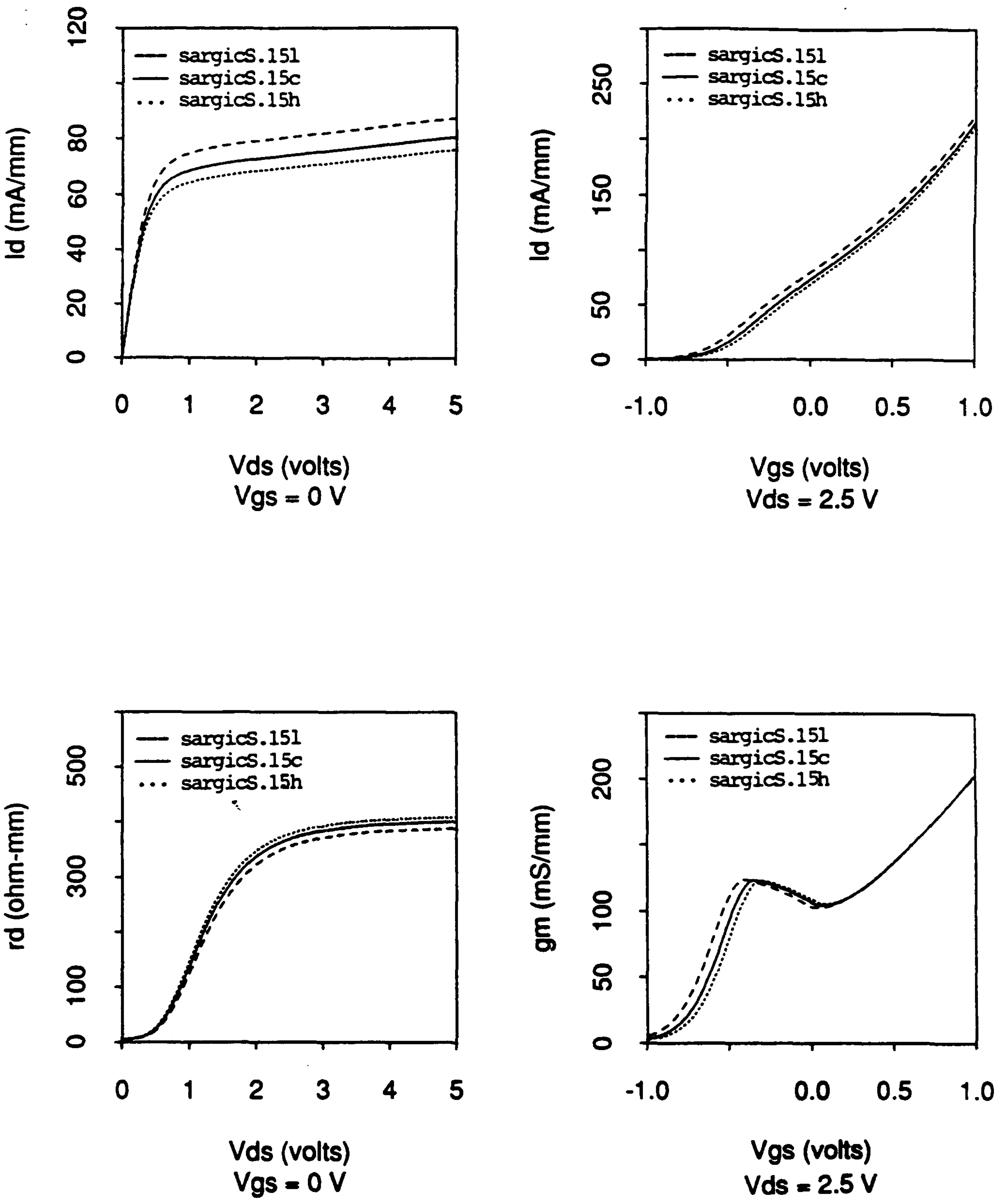


Figure 5.11.DC Characteristics of Nominal, High and Low Current 20 μm DHFET at 125°C.

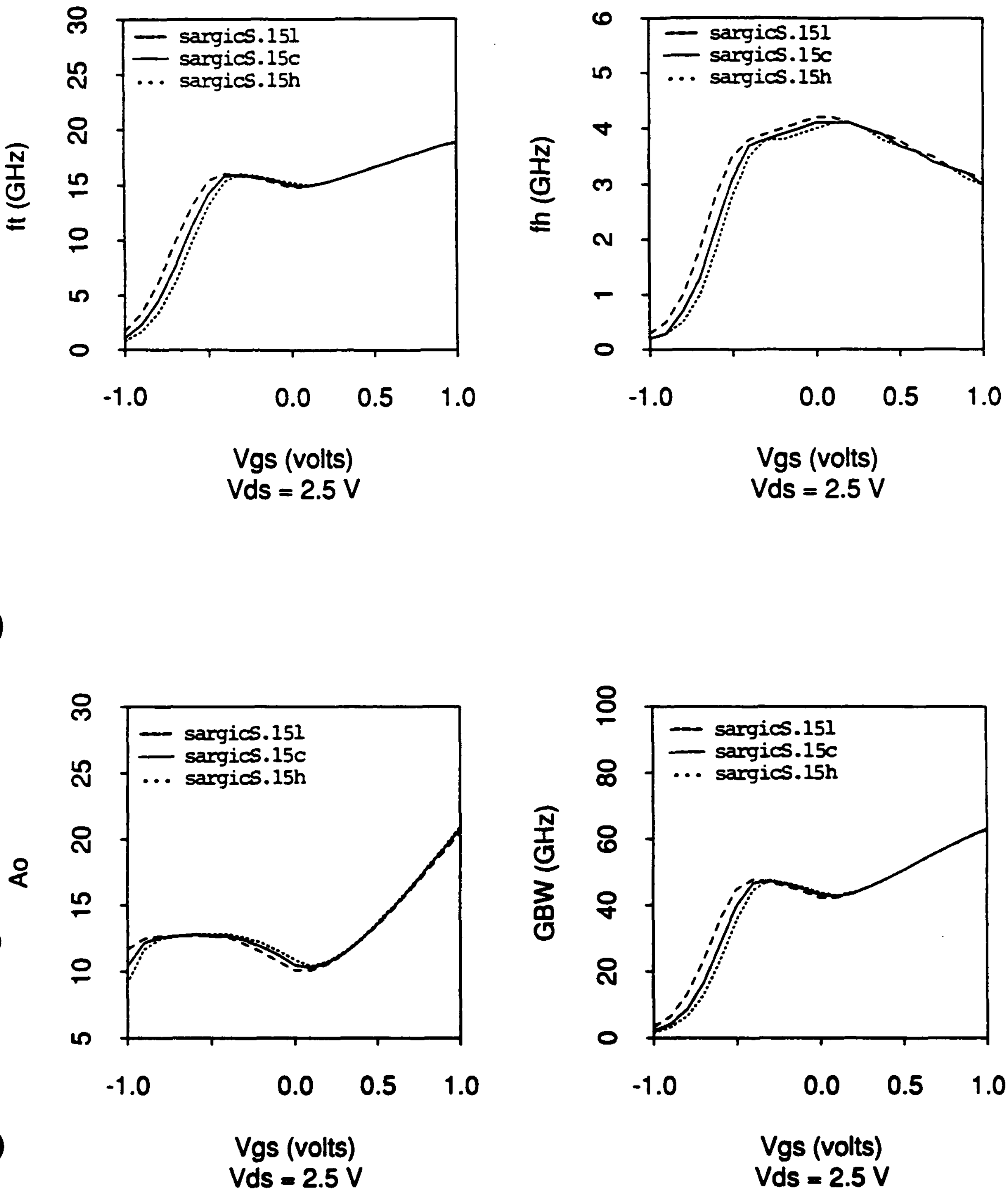


Figure 5.12.RF Characteristics of Nominal, High and Low Current 20 µm DHFET at 125°C.

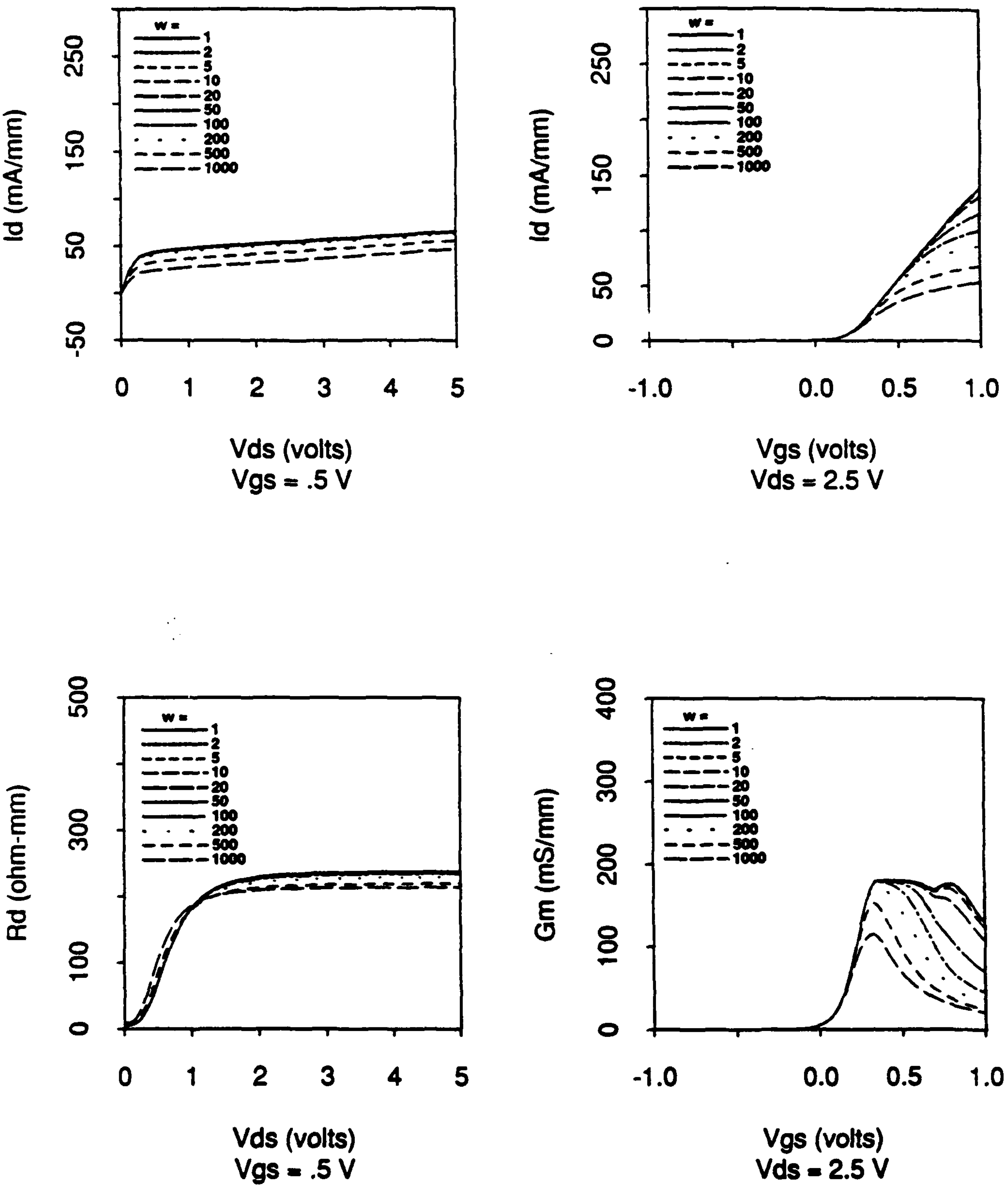


Figure 5.13. DC Characteristics Versus Device Scaling of EHFET at 25°C.

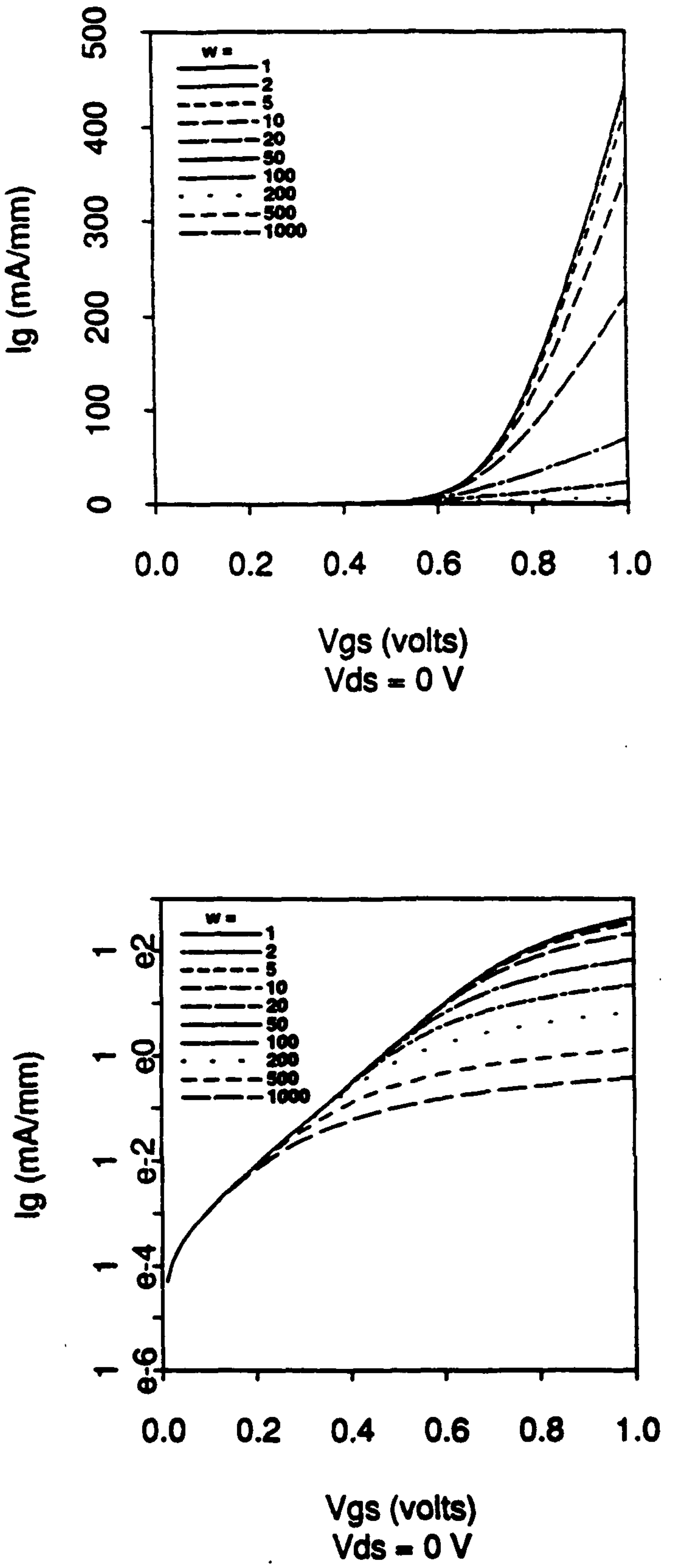


Figure 5.14.DC Characteristics Versus Device Scaling of EHFET Schottky Diode at 25°C.

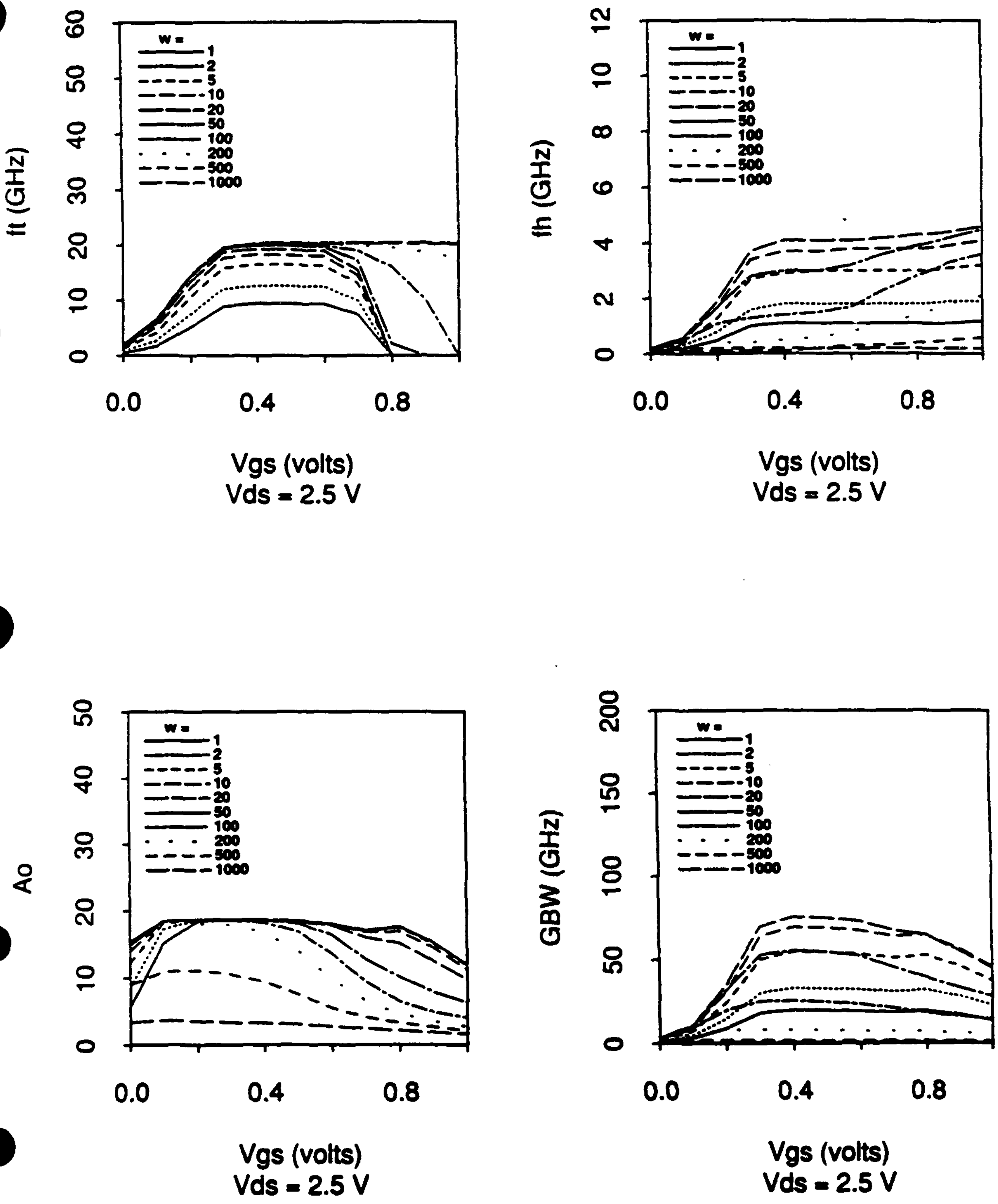


Figure 5.15. RF Characteristics Versus Device Scaling of EHFET at 25°C.

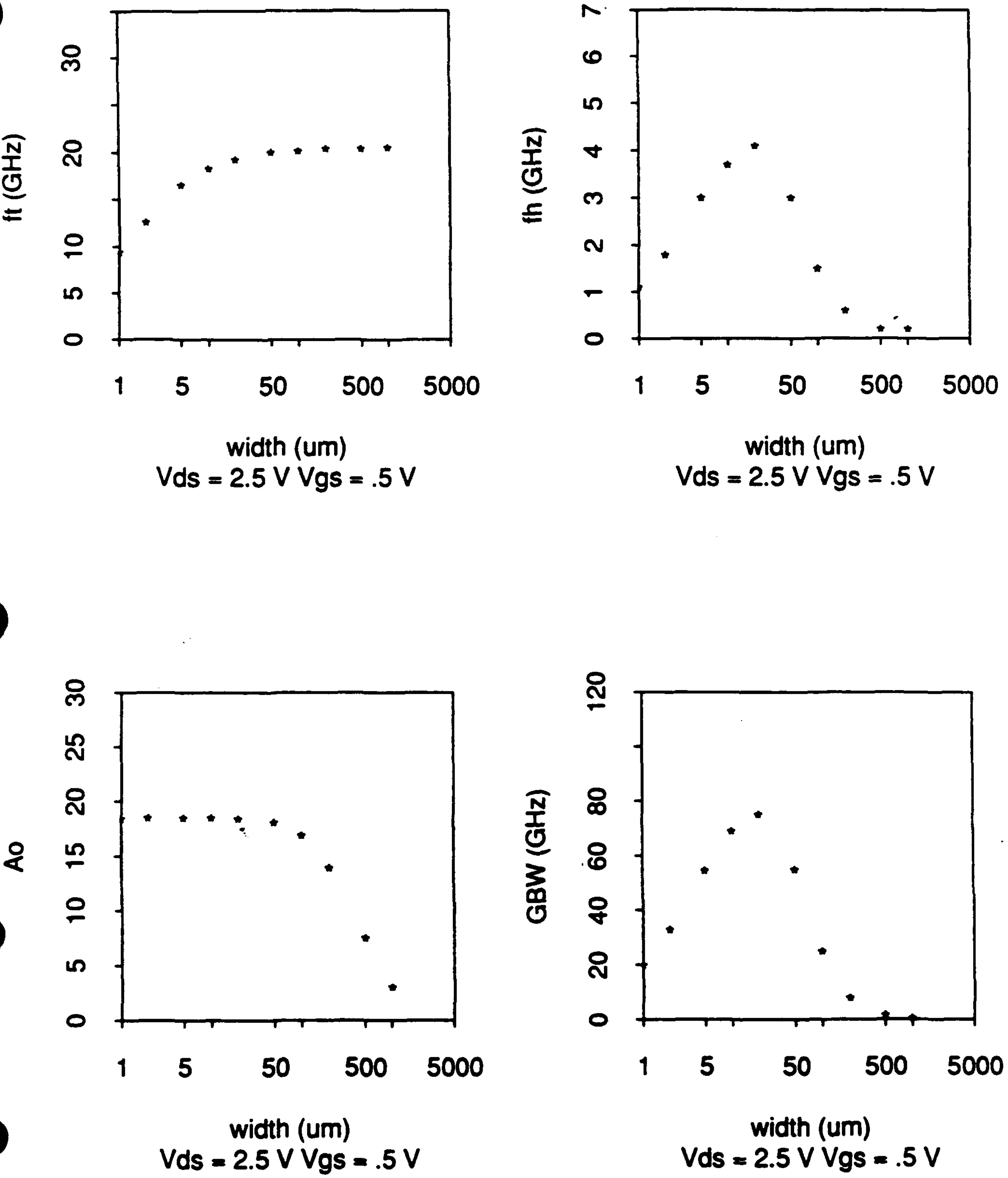


Figure 5.16.RF Characteristics Versus Device Scaling of EHFET with Vds = 2.5 volts and Vgs = 0.5 volts at 25°C.

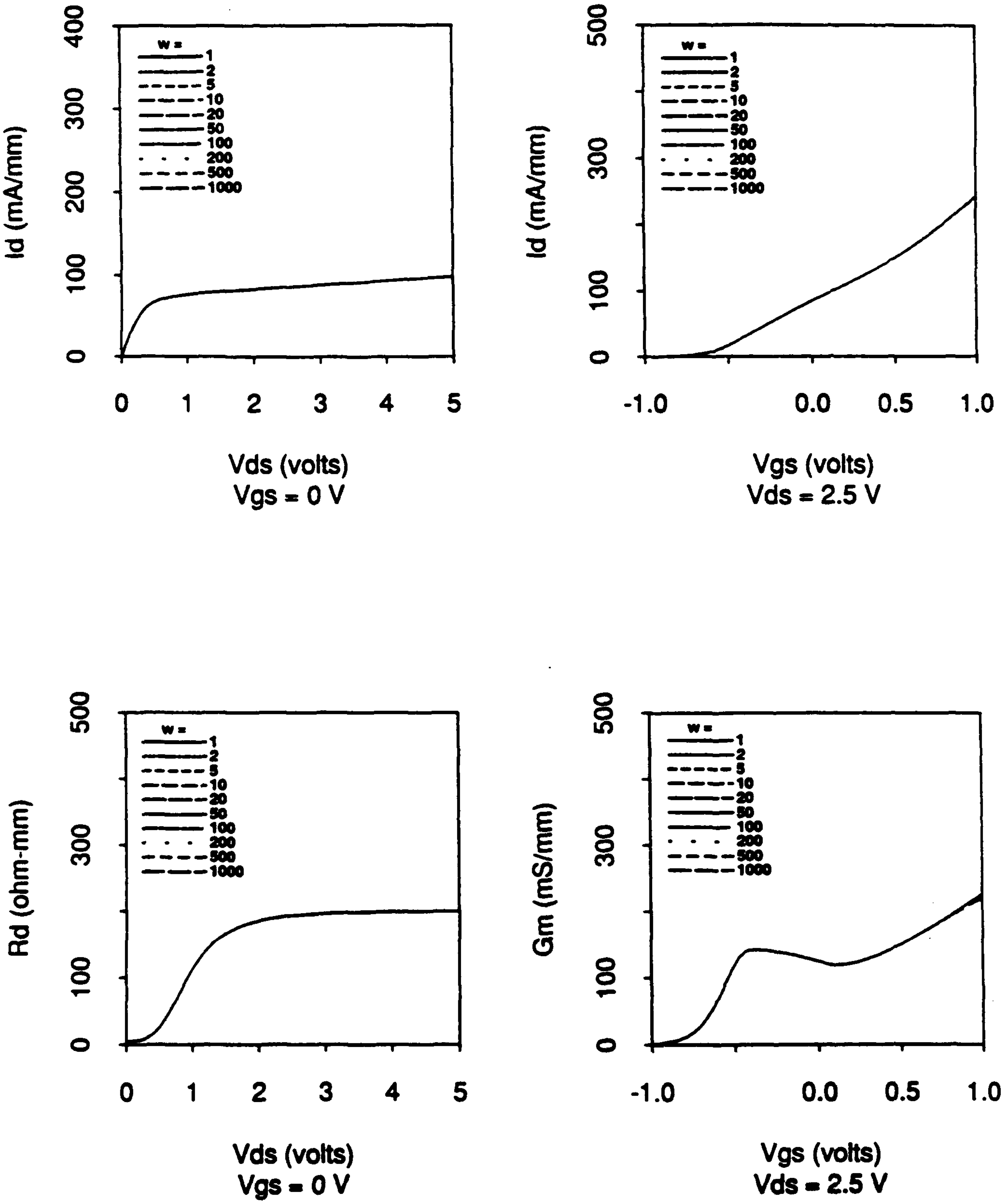
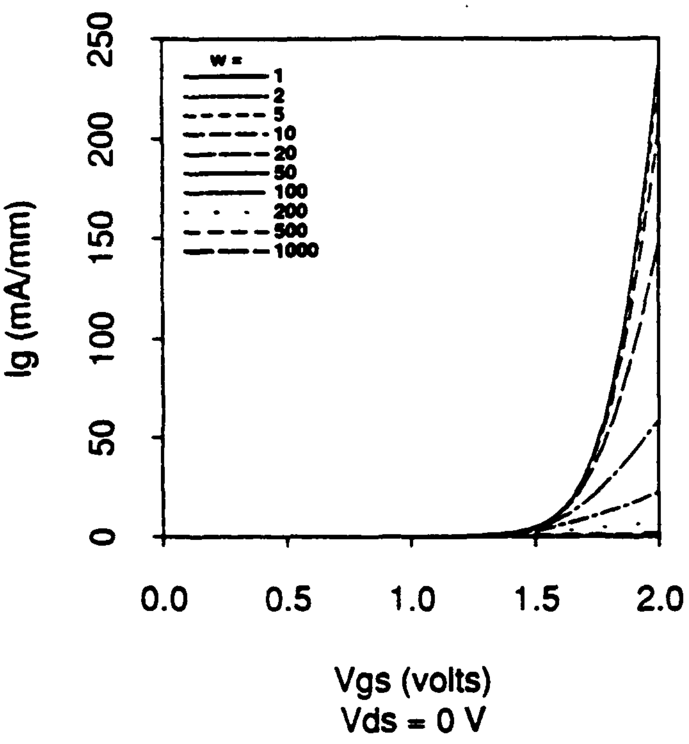


Figure 5.17. DC Characteristics Versus Device Scaling of DHFET at 25°C.



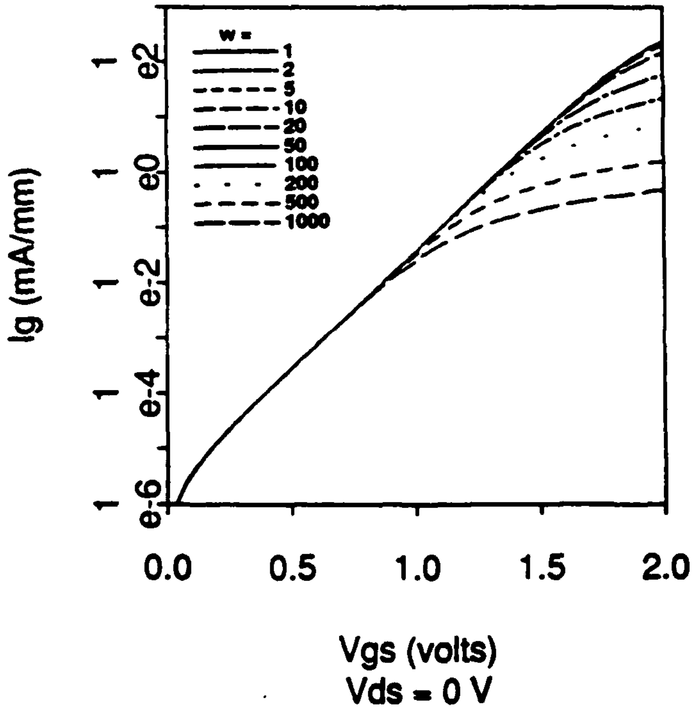


Figure 5.18.DC Characteristics Versus Device Scaling of DHFET Schottky Diode at 25°C.

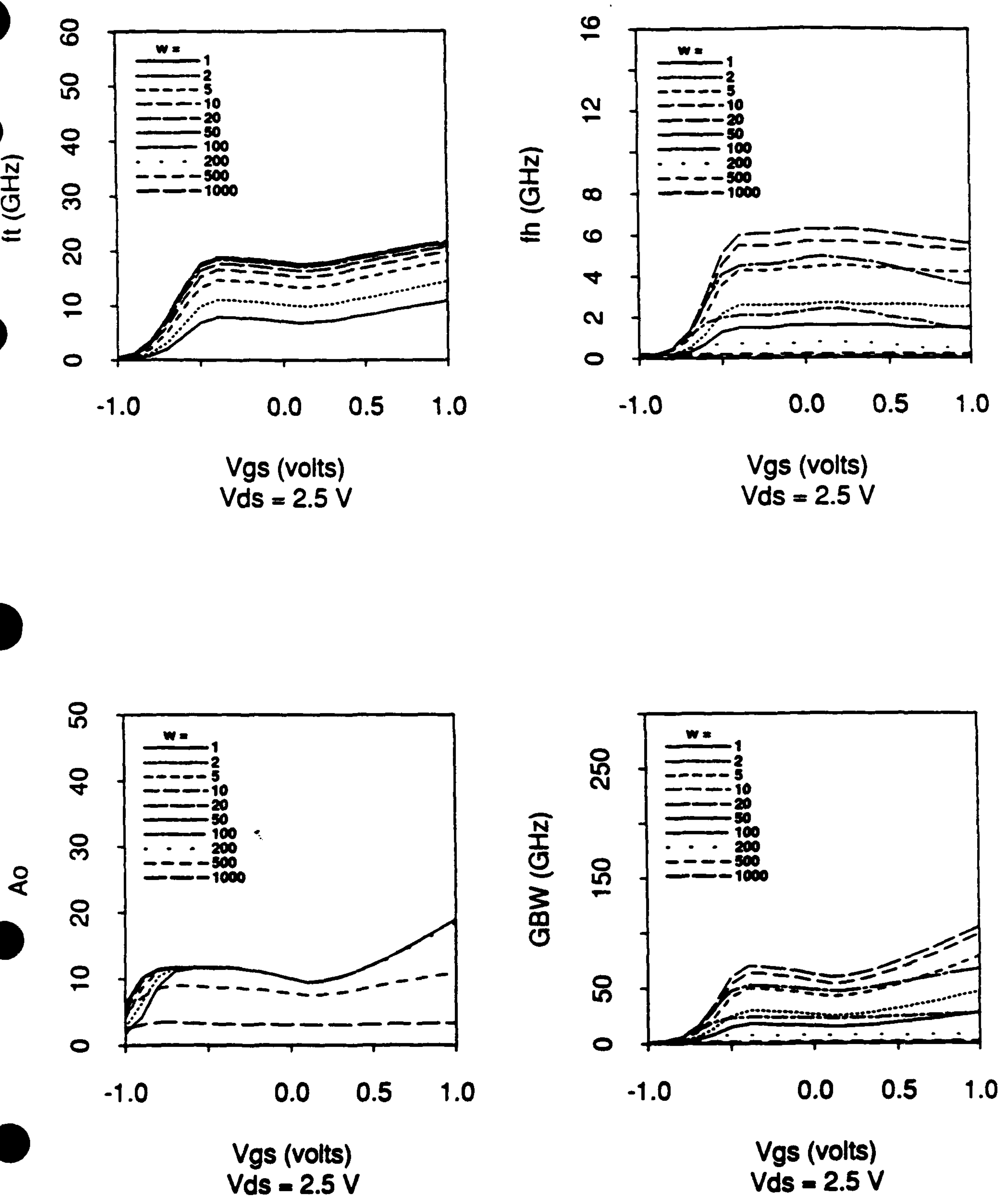


Figure 5.19. RF Characteristics Versus Device Scaling of DHFET at 25°C.

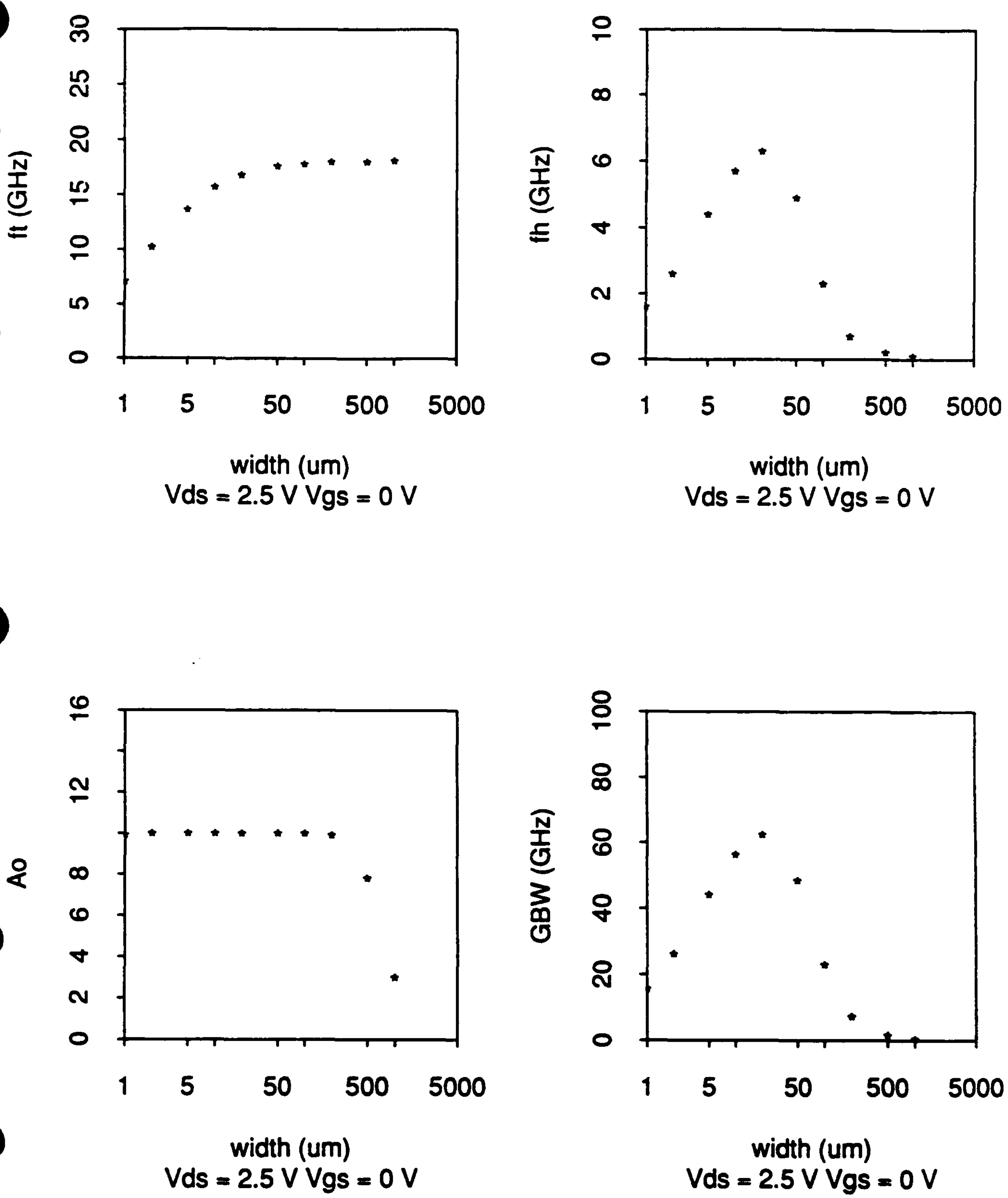
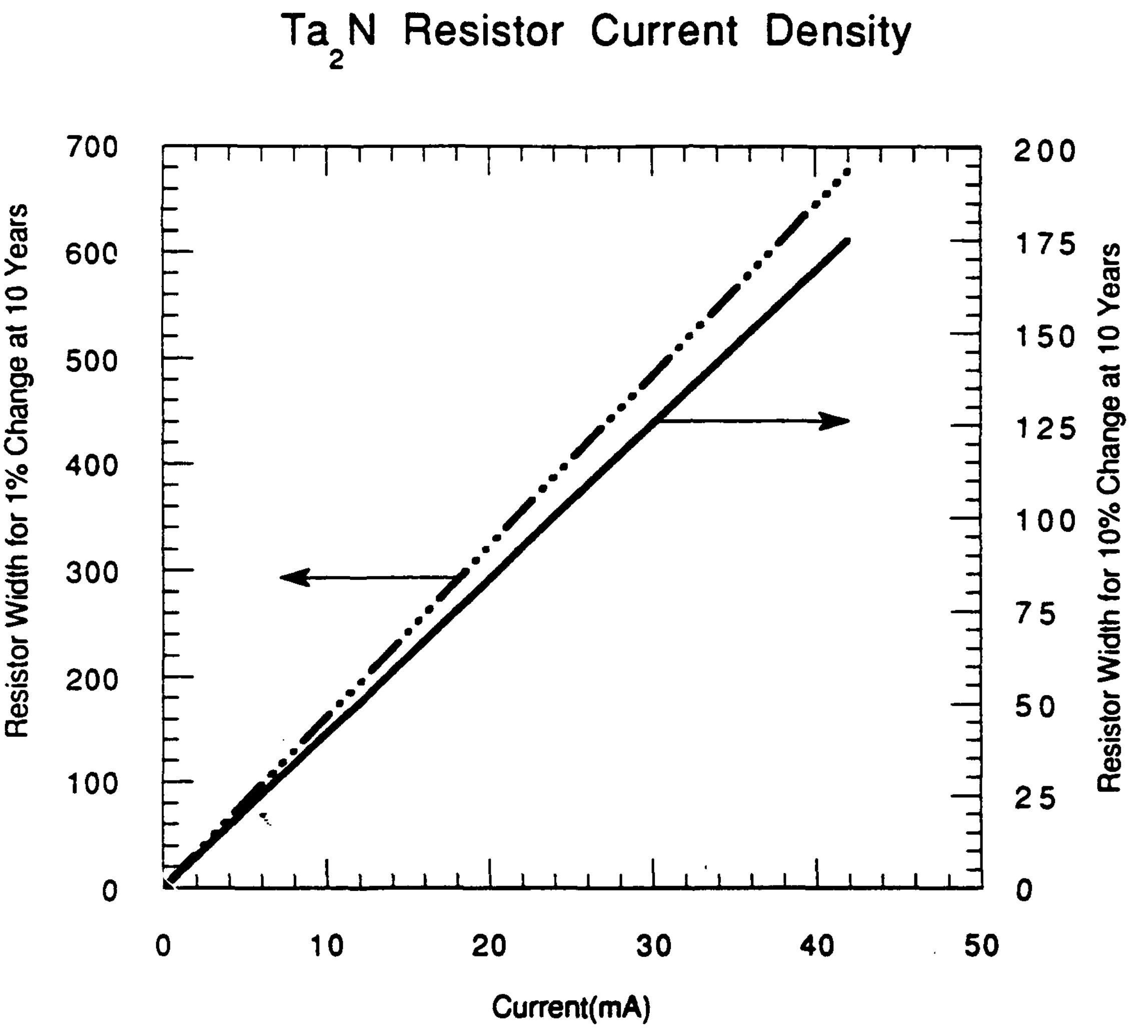


Figure 5.20.RF Characteristics Versus Device Scaling of DHFET with Vds = 2.5 volts and Vgs = 0 volts at 25°C.

Section VI.
Electromigration

Introduction

The electromigration design rules for the gold metalization and TaN resistors used in the SargicS process are described in the graphs and table contained in the following section.



Maximum operating temperature: 100°C
For 1% resistance change at 10 years: i* = 0.062mA/µm
For 10% resistance change at 10 years: i* = 0.24mA/µm

Figure 6.1. TaN Resistor Electromigration Design Rules.

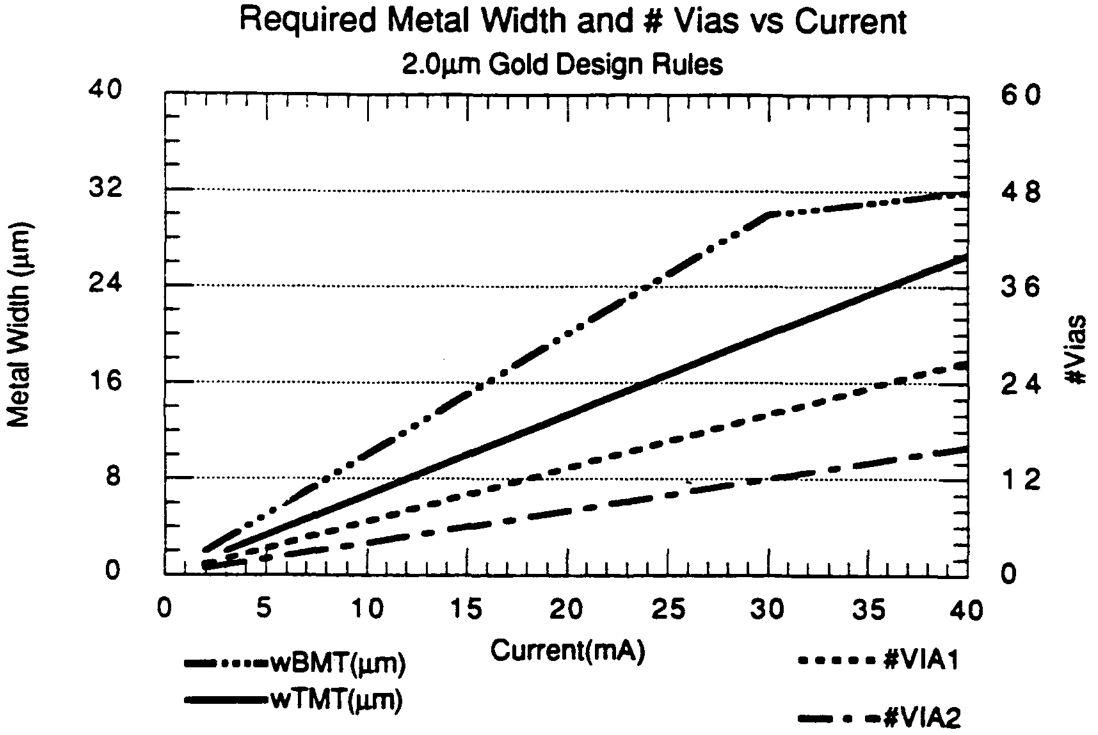


Figure 6.2. Gold Metalization Electromigration Design Rules for Metal Widths from 0 to 40 µm.

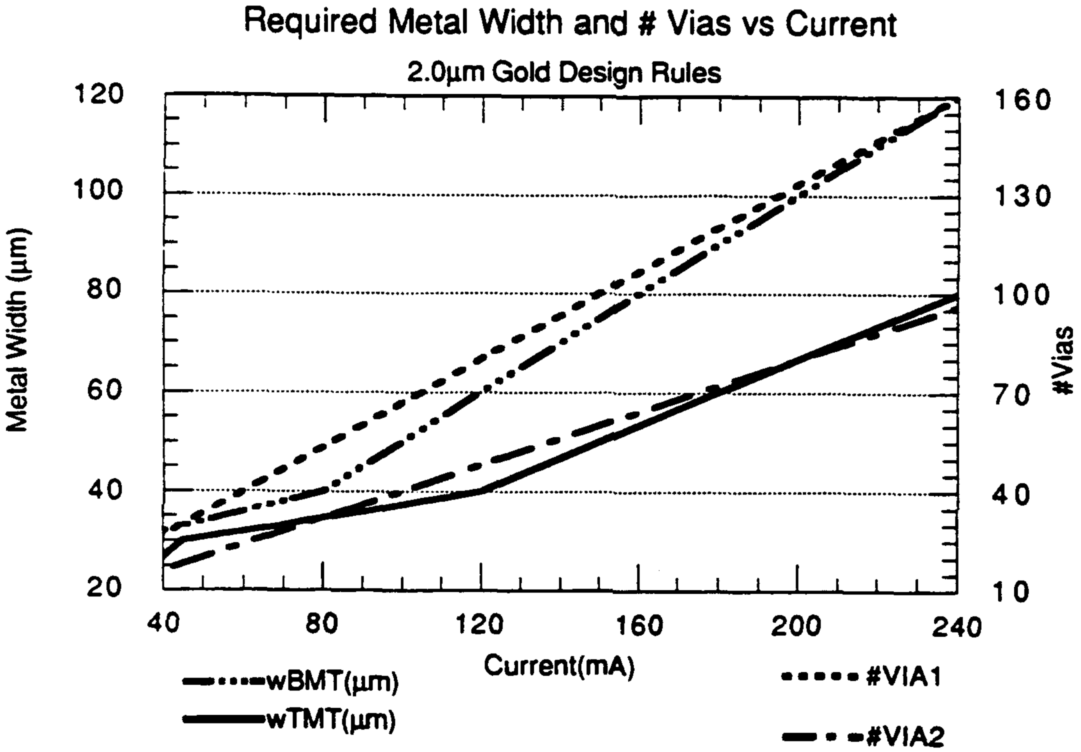


Figure 6.3. Gold Metalization Electromigration Design Rules for Widths from 20 to 40 µm.

SARGIC Gold Design Guidelines

Structure	Width, w or diameter, d (μm)	Current density, j (10^5 A/cm^2)	Current, i (mA)	Current/ unit width,i* (mA/μm)
BOTMET	$w<30\mu m$	2.0	$1.0*w$	1.0
	$30\mu m \leq w \leq 40\mu m$	2.0-4.0	$w*(0.3*w-8)^{0.5}$	1.0-2.0
	$w>40\mu m$	4.0	$2.0*w$	2.0
TOPMET	$w<30\mu m$	2.0	$1.5*w$	1.5
	$30\mu m \leq w \leq 40\mu m$	2.0-4.0	$1.5*w*(0.3*w-8)^{0.5}$	1.5-3.0
	$w>40\mu m$	4.0	$3.0*w$	3.0
Vias (VIA2)	$d=1.5$	2.0	2.5	
Contacts (VIA1)				
Gate	$d=1.5$	2.0	1.5	
Ohmic	$d=1.5$	2.0	1.5	

Metal parameters:
BMT thickness: 0.5μm
TMT thickness: 1.0μm

Operating conditions

85° C ambient
10 year life
100 FIT maximum electromigration failure rate
40°C maximum temperature rise above ambient

Table 6.1. Gold Metalization Electromigration Design Rules.

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Section VIII.
Appendices

Appendix A.

PROCESSED LEVELS:

LEVEL NAME	DESCRIPTION
ALM	Alignment Mark, all levels aligned to this feature
ETB	EHFET TUB
ETBLITHO	EHFET TUB Lithography Evaluation Features
ETBNOGS	EHFET TUB Uncompensated Features
ISO	ISOLATION
ISODI	ISOLATION for diodes
ISORES	ISOLATION for resistors
ISOLITHO	ISOLATION Lithography Evaluation Features
ISONOGS	ISOLATION Uncompensated Features
GMT	GATE METAL for Interconnect Runners
GMTE	GATE METAL for Enhancement FETs
GMTD	GATE METAL for Depletion FETs
GMTLITHO	GATE METAL Lithography Evaluation Features
GMTNOGS	GATE METAL Uncompensated Features
NIP	N+ Implant
NIPLITHO	N+ Implant Lithography Evaluation Features
NIPNOGS	N+ Implant Uncompensated Features
OMT	OHMIC METAL
OMTLITHO	OHMIC METAL Lithography Evaluation Features
OMTNOGS	OHMIC METAL Uncompensated Features
VA1	VIA1
VA1LITHO	VIA1 Lithography Evaluation Features
VAINOGS	VIA1 Uncompensated Features
BMT	BOTTOM METAL
BMTCP	BOTTOM METAL for capacitors
BMTBP	BOTTOM METAL for bond pads
BMTLITHO	BOTTOM METAL Lithography Evaluation Features
BMTNOGS	BOTTOM METAL Uncompensated Features
VA2	VIA2
VA2BP	VIA2 for bond pads
VA2LITHO	VIA2 Lithography Evaluation Features
VA2NOGS	VIA2 Uncompensated Features
TMT	TOP METAL
TMTCP	TOP METAL for capacitors
TMTBP	TOP METAL for bond pads
TMTLITHO	TOP METAL Lithography Evaluation Features
TMTNOGS	TOP METAL Uncompensated Features
TAN	TaN Resistor
PAS	PASSIVATION
PASNOGS	PASSIVATION Uncompensated Features

NON-PROCESSED LEVELS:

LEVEL NAME	DESCRIPTION
CELLOUT	CELL OUTLINE
LABOMT	OHMIC METAL LABEL
LABGMT	GATE METAL LABEL
LABBMTP	BOTTOM METAL POWER BUS LABEL
LABBMT	BOTTOM METAL LABEL
LABTMTP	TOP METAL POWER BUS LABEL
LABTMT	TOP METAL LABEL
OUT	MISCELLANEOUS OUTLINES
TEXT	MISCELLANEOUS TEXT
PIN	MISCELLANEOUS ROUTING CHANNELS
LABGM1	GATE MATRIX LABEL 1
LABGM2	GATE MATRIX LABEL 2
LABGM3	GATE MATRIX LABEL 3

APPENDIX B

PROCESS CONTROL MONITORS

Process Control Monitors

Two Process Control Modules are available for use with the SARGIC-HFET processing used in the GaAs Pilot Line III. The first module, SE2V1, is mandatory. The second module contains processing features arrayed in a way that is suitable for analysis in a transmission electron microscope (TEM); this module is optional. AT&T adds Process Controls Modules to all circuit designs when the designs are prepared for mask fabrication.

1. DC and RF Process Control Module, SE2V1

Figure 1 shows the layout of Process Control Module (PCM) SE2V1. Figure 2 shows the same module, this time with an identifying number for each feature. Unused portions are labeled "NU."

1. DFET transmission line and 2μm isolation tester. The transmission line measures the N^+ sheet resistance for the DFET structure and the contact resistance between ohmic metal and the DFET semiconductor material. Isolation current across a 2μm gap is measured at 5 V.
2. EFET transmission line and 2μm isolation tester. The transmission line measures the N^+ sheet resistance for the EFET structure and the contact resistance between ohmic metal and the EFET semiconductor material. Isolation current across a 2μm gap is measured at 5 V.
3. Split Cross Bridge for Ohmic Metal. Measurements give sheet resistance of the metal, linewidth, and pitch of split lines.
4. Split Cross Bridge for BOTMET. Measurements give sheet resistance of the metal, linewidth, and pitch of split lines.
5. Sidegate and isolation tester for 25μm DFETs. Measurements give isolation currents between FETs separated by different distances. They also give the change in DFET current as voltages are varied on nearby FETs.
6. 25μm diodes on DFET sites. We measure 7 different diode characteristics.
7. Split Cross Bridge for TOPMET. Measurements give sheet resistance of the metal, linewidth, and pitch of split lines.
8. Sidegate and isolation tester for 25μm EFETs. Measurements give isolation currents between FETs separated by different distances. They also give the change in EFET current as voltages are varied on nearby FETs.
9. 25μm diodes on EFET sites. We measure 7 different diode characteristics.
10. Split Cross Bridge for gate metal. Measurements give sheet resistance of the metal, linewidth, and pitch of split lines.
11. Van der Pauw tester for N^+ implanted layers.
12. Van der Pauw tester for N layers.

13. Capacitor.We measure leakage current and capacitance.

14. 25µm EFETs. We measure 16 different FET characteristics.

15. 25µm DFETs. We measure 16 different FET characteristics.

16. Six-terminal contact resistance tester for ohmic metal to N^+ implant interface. The tested contact is 2µm x 2µm.

17. Six-terminal contact resistance tester for ohmic metal to N^+ implant interface. The tested contact is 3µm x 3µm.

18. 3µm diode on DFET material. Not presently used.

19. 3µm diode on EFET material. Not presently used.

20. Four-terminal contact resistance testers for interface resistance between TOPMET and BOTMET. A comparison with data from feature #25 checks for alignment effects.

21. Four-terminal contact resistance testers for interface resistance between BOTMET and gate metal. A comparison with data from feature #22 checks for alignment effects.

22. Four-terminal contact resistance testers for interface resistance between gate metal and BOTMET. A comparison with data from feature #21 checks for alignment effects.

23. Four-terminal contact resistance testers for interface resistance between BOTMET and ohmic metal. A comparison with data from feature #24 checks for alignment effects.

24. Four-terminal contact resistance testers for interface resistance between ohmic metal and BOTMET. A comparison with data from feature #23 checks for alignment effects.

25. Four-terminal contact resistance testers for interface resistance between BOTMET and TOPMET. A comparison with data from feature #20 checks for alignment effects.

26. Four-terminal contact resistance testers for interface resistance between TOPMET and TaN.

27. Split Cross Bridge for TaN. Measurements give sheet resistance of the metal, linewidth, and pitch of split lines.

28. 3µm EFET for comparison to 25µm EFET.

29. 3µm DFET for comparison to 25µm DFET.

30. Orthogonal combs separated by dielectric. We measure leakage current to test dielectric integrity. There are 1720 crossovers between ohmic metal and BOTMET, and an additional 1680 crossovers between BOTMET and TOPMET. Besides the crossovers, each pair of metals has a 320 x 2 µm runner over a large pad of underlying metal.

31. Chain of 1.0μm via connections between various metal layers. A conductivity measurement assesses via integrity. The conducting path goes from TOPMET to BOTMET to gate metal to BOTMET to TOPMET to BOTMET to ohmic metal to BOTMET to TOPMET, using a via for each connection from one metal layer to the next. The pattern repeats until there are a total of 4000 vias.
32. Chain of 1.5μm via connections between various metal layers. A conductivity measurement assesses via integrity. The conducting path goes from TOPMET to BOTMET to gate metal to BOTMET to TOPMET to BOTMET to ohmic metal to BOTMET to TOPMET, using a via for each connection from one metal layer to the next. The pattern repeats until there are a total of 4000 vias.
33. Photolithographic patterns for characterizing linewidth.
34. Large area DFET to evaluate doping, barrier height, ideality, and mobility.
35. Large area EFET to evaluate doping, barrier height, ideality, and mobility.
36. Patterns for measuring etch-step height.
37. Open circuit pads and metallization for measuring parasitics so that they can be de-embedded from S-parameter measurements.
38. DFET S-parameter tester. This is a two-fingered FET with a total gate width of 50μm.
39. EFET S-parameter tester. This is a two-fingered FET with a total gate width of 50μm.

2. TEM Module

Figure 3 shows a cross section of the TEM Module. The figure is drawn to scale. A cross-section of this module can be examined in a TEM to characterize the details of the semiconductor, metal, and dielectric layers.

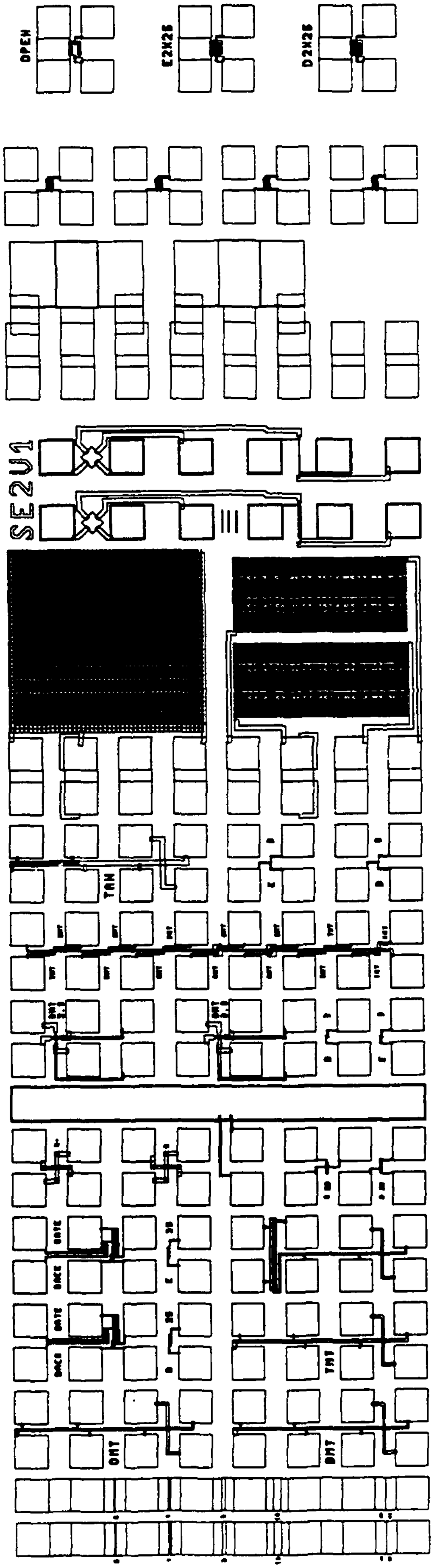
OPEN
E2X2S
D2X2S
SE2U1
TAN
OMT
GATE
BACK

Figure 1

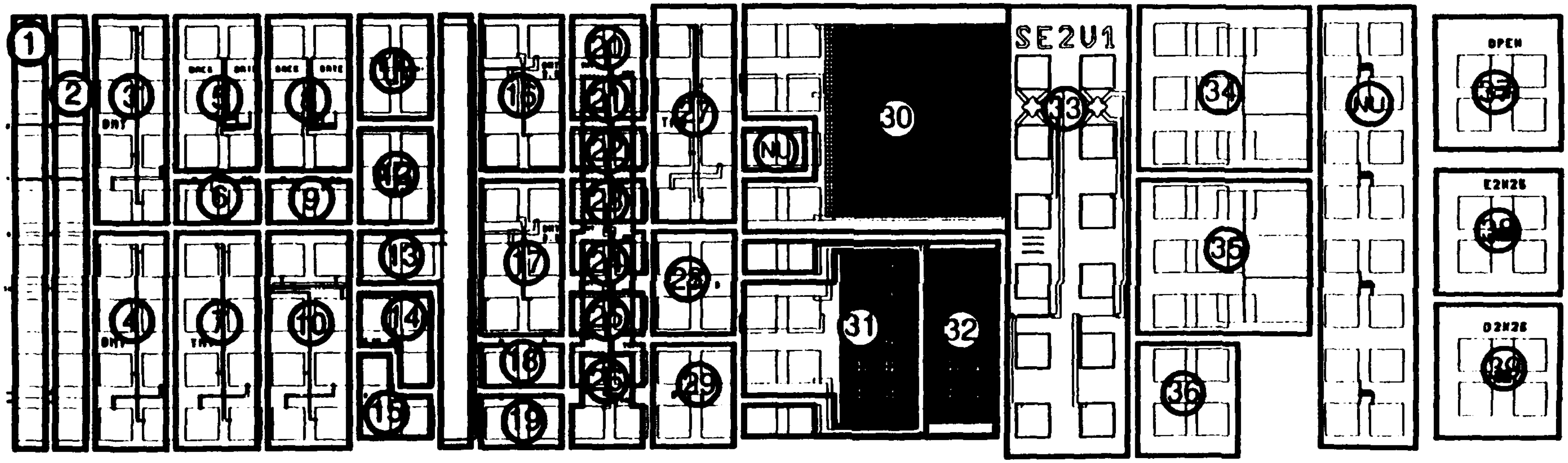
NU
SE2U1
NU
OPEN
E2N2B
D2N2B

Figure 2

TEM Module

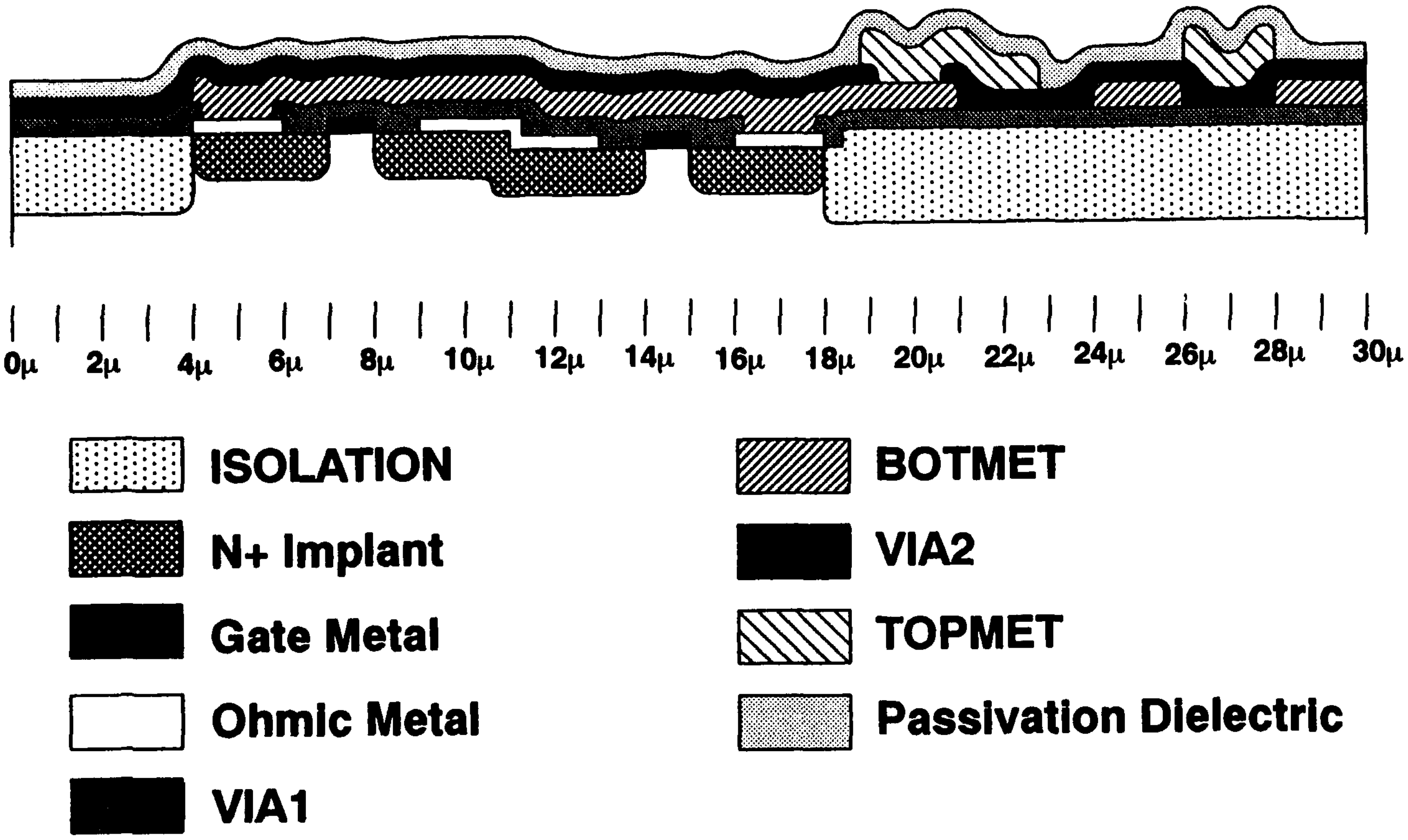
0μ
2μ
4μ
6μ
8μ
10μ
12μ
14μ
16μ
18μ
20μ
22μ
24μ
26μ
28μ
30μ
ISOLATION
N+ Implant
Gate Metal
Ohmic Metal
VIA1
BOTMET
VIA2
TOPMET
Passivation Dielectric

Figure 3

APPENDIX C

ADVANCED TECHNOLOGY
FINAL REPORT

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Figure 20. Total dose effects in Advanced Technology HFETs (Gamma Radiation). C-31

Figure 21. Total Dose Irradiation of Advanced Technology Ring Oscillator. C-32

1. INTRODUCTION (A. G. Baca, S. F. Nygren)

Under our contract for a Gallium Arsenide Pilot Line for High Performance Components (F29601-87-C-0202), DARPA asked us to "investigate (the) manufacturing feasibility of technology that is capable of achieving higher performance (at least a factor of two increase in speed or an order of magnitude in power) for the selected circuits ... picked for the main program." We chose to seek a factor of two increase in speed through two changes: 1) decreasing interconnect design rules to 1.5 μm lines and spaces (gate length is decreased from 1.0 μm to 0.75 μm), and 2) using an improved (faster) implementation of the SFFL logic gate. To provide a more robust wafer fabrication process for the decreased interconnect design rules, we developed an aluminum metallization process to replace the existing gold-based Baseline Technology.

As this report describes in detail, we believe we accomplished the goals of this program. By demonstrating 400 MHz operation with 20 gate delays, we achieved a factor of two increase in speed. Simultaneously, by examining yield data from process testers and actual circuits, we believe this Advanced Technology will have 30% of the manufacturing yield of the Baseline Process, thereby meeting the goals for manufacturing feasibility.

We developed our Advanced Process in two parallel paths. On one path, we developed a process for aluminum interconnect metallization. In comparison to our standard liftoff-patterned evaporated TiPtAu interconnects, we believe subtractively-patterned sputtered aluminum will provide better step coverage and superior metal definition, especially for the reduced line and space dimensions. As discussed in detail in Section 2, some key developments used in our aluminum process include a barrier to isolate aluminum from the gold-based ohmic contacts, thereby preventing "purple plague," and a dielectric planarization process to eliminate shorts. We processed both gold-interconnect wafers and aluminum-interconnect wafers using 1.5 μm lines and spaces. The gold interconnect wafers had via, crossover and serpentine yields comparable to our standard 2.0 μm line and space metallization process. Process testers with aluminum interconnects gave somewhat lower yields, but the planarization process had not been fully implemented when the evaluation was done.

On the parallel path, we confirmed that the Advanced Process would achieve the electrical performance goals (400 MHz for 20 gate delays, or 125 ps/gate). First, using ring oscillators, we demonstrated performance up to 926 MHz with 20 gate delays. Second, we fabricated 8x8 multiplier circuits with a total of 889 gates. Half the functional devices had gate delays equal to or shorter than 125 ps. Third, we examined the intrawafer and wafer-to-wafer variations in FET threshold using the Advanced Technology. These variations are two to three times as large as standard product from the same era. While we could expect to reduce variation somewhat as we refine our Advanced Technology, we believe further process development will be necessary to eliminate all the excess variation. All of these electrical tests were done with gold interconnects before the aluminum process development was complete.

Since our goal was to investigate manufacturing feasibility, we limited our work to developing a 1.5 μm aluminum interconnect process, measuring performance of circuits fabricated with 1.5 μm design rules, and making an initial characterization of reliability and radiation hardness. Overall, we're very pleased with the outcome of this study: we successfully demonstrated a factor of two increase in circuit speed without increasing circuit power consumption, and we demonstrated a potential for very high wafer fab processing yields with aluminum metallization. We also found that our diffusion barrier adequately prevents "purple plague" and that total dose radiation hardness is unchanged from the Baseline Technology.

If there were plans to place this Advanced Technology into production, we found two remaining problems that need to be solved. First, the present aluminum interconnects have an unacceptably short life due to electromigration failures. This can probably be improved by altering the metal deposition conditions. Second, the transient dose radiation hardness is inferior to the Baseline Technology. This may be due to the smaller dimensions of the Advanced Technology and may be inherent to the process.

The remainder of this report describes the details of the development and characterization of this Advanced Technology in three sections:

- Process Technology
- Test Circuits
- Reliability and Radiation Testing

2. PROCESSING TECHNOLOGY

2.1 Aluminum Interconnects (R. J. Shul, A. G. Baca, R. M. Havrilla, S. E. Lengle)

The aluminum interconnect metallization process requires applying WSi as a barrier between the gold-based ohmic contacts and the aluminum interconnects, sputter depositing aluminum, patterning it into 1.5 µm lines and spaces, using sidewalls to eliminate aluminum stringers, and planarizing the structure to eliminate shorts due to aluminum left in troughs. We favor sputter-deposited aluminum over our standard evaporated TiPtAu interconnects because it provides better step coverage over vias. In addition, the subtractive patterning used with aluminum gives superior metal definition and fewer shorts compared to liftoff of TiPtAu interconnects.

Deposition

Aluminum is deposited in an MRC 943 sputtering system from a composite target consisting of 0.5% Cu and 99.5% Al. The Cu is included to minimize electromigration. The thickness is chosen to match the sheet resistance of the baseline technology TiPtAu interconnects; we use 8000Å for aluminum bottom metal and 10,600Å for aluminum top metal.

Lithography

Due to the reflective nature of aluminum, conventional fine line lithography is not possible. To reduce reflection by about 50%, we use a WSi_x coating over the aluminum. Then we can routinely pattern 1.5 µm lines and spaces with a 5x stepper.

Reactive Ion Etching

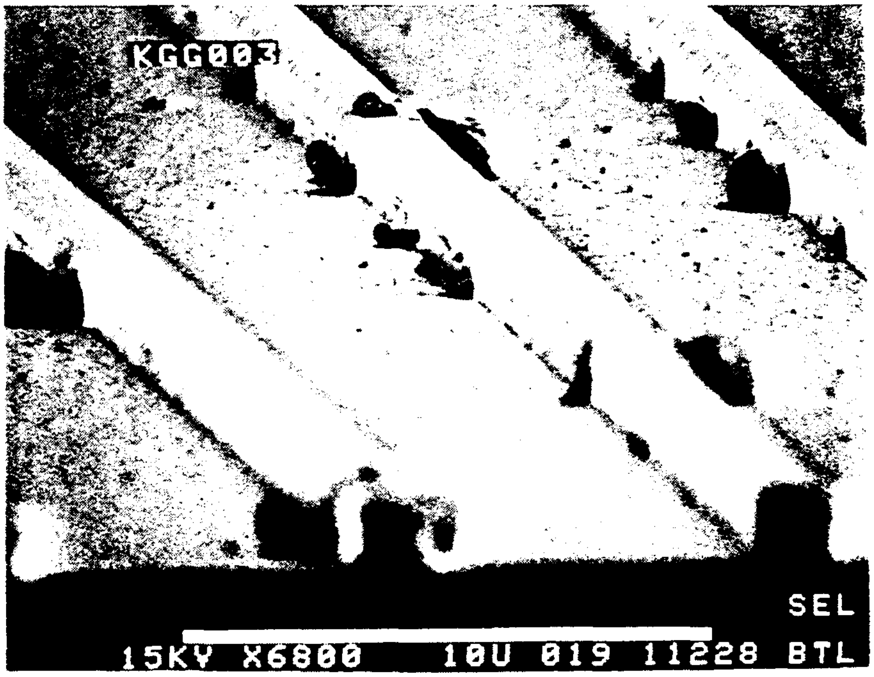
Etch

Aluminum is patterned in a BCl_3/Cl_2 plasma operating in a reactive ion etch mode. Including BCl_3 in the etch chemistry helps expose aluminum to the plasma by removing oxide and minimizes the incubation time for etching. The reactive ion etch mode promotes a more physical, anistropic etch with vertical Al sidewalls; without the reactive ion etch mode, there would be severe undercutting.

Corrosion

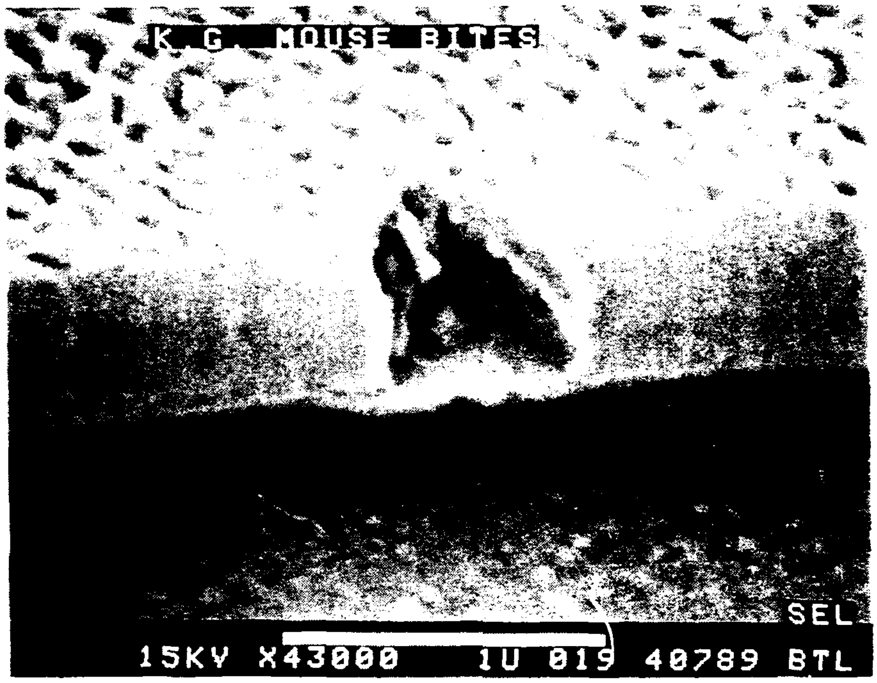
Post etch corrosion is one of the major considerations in the subtractive patterning of Al (see Figure 1). The presence of residual Cl catalyzes the corrosion of Al in the presence of moisture. This can be overcome by introducing an in-situ fluorine passivation. The patterned Al sample is exposed to an SF_6 plasma, which exchanges F with residual Cl, forming involatile products and eliminating corrosion. The use of BCl_3 also helps eliminate water from the chamber, which is held at approximately 58°C to reduce water absorption.

After the wafers are removed from the chamber, they are rinsed in water to remove any remaining Cl. Use of a water rinse often results in a phenomenon referred to as "mouse bites . Mouse bites are localized regions of missing metal usually seen at the edges of lines or pads (see Figure 2). This can result in open interconnect lines or areas of excessively high resistance which might result in premature failures. Altering the pH of the deionized water slightly eliminates mouse bites.


KGG003
SEL
15KV X6800 10U 019 11228 BTL

Corrosion of Al lines over GaAs. The Al was not exposed to a passivation step following the BCl_3/Cl_2 etch.

Figure 1.


K. G. MOUSE BITES
SEL
15KV X43000 1U 019 40789 BTL

Mouse bites are missing pieces of metal which are often observed at the edge of features. This is observed following the water rinse to remove residual Cl.

Figure 2.

Barrier

The use of Al interconnects our technology introduces a complication due to the interaction of Al interconnects and Au from the ohmic contacts. Interdiffusion of Al and Au can lead to the formation of high resistivity intermetallics often referred to as "purple plague." We developed a conductive diffusion barrier to separate Au from Al because these high resistivity intermetallics can cause premature circuit failures.

The barrier is a multi-layer WSi_x structure (see Figure 3). Following the evaporation of ohmic metal, 1000Å of WSi_x is sputter deposited over the substrate and defined by the ohmic liftoff process. The ohmic metal feature is therefore encapsulated by WSi_x. The sputter deposition of WSi_x decreases the reliability of the liftoff process, increasing the likelihood of burrs. Burrs have been observed for the 1.5μ design rules, but we saw no evidence of shorts.

To further prevent interdiffusion of Au and Al, an additional layer of WSi_x, 2000Å, is sputter-deposited in-situ, just prior to Al deposition. This layer of WSi_x is patterned with the same lithography as the Al interconnect lines and is etched in-situ following the Al etch. Thus the WSi_x barrier is patterned by the Al lines. Step coverage is still an issue with this technique, and we may require a plug process.

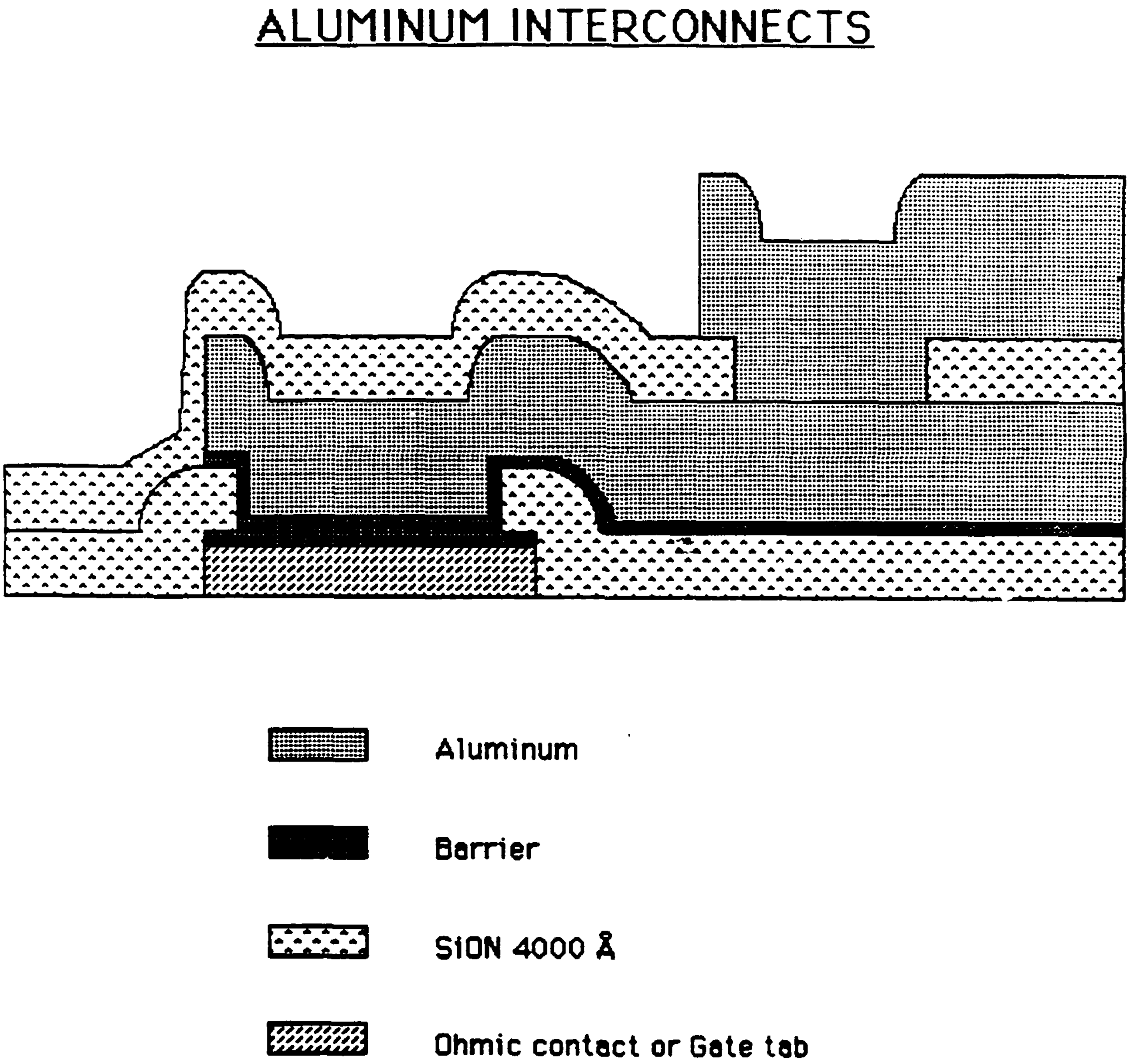
First Level Aluminum Interconnects

A multi-step, in-situ etch is incorporated to remove the thin anti-reflective WSi_x layer (SF_6 etchant), pattern Al (BCl_3/Cl_2 etchant), passivate residual Cl and pattern the WSi_x barrier layer (SF_6/O_2 etchant), and initiate photoresist removal (O_2). The wafers are then removed from the chamber and rinsed in deionized water.

Preliminary etch experiments for Al interconnects were on PT-Y samples. (See Section 2.2 for an expanded description of PT-Y.) Al etching over ohmic metal pads (AuGeNi) reproducibly yields anisotropic lines and shows no sign of corrosion (see Figure 4). However, shorts were observed in via chain test patterns of Al interconnects etched over gate metal (WSi_x). Figure 5 shows filaments or stringers of Al remaining in the via chain patterns where dielectric (4000Å) covers gate metal. Significant overetching did not remove the Al stringers. With the aid of SEM photographs, we saw cusping of dielectric over gate metal (see Figure 6).

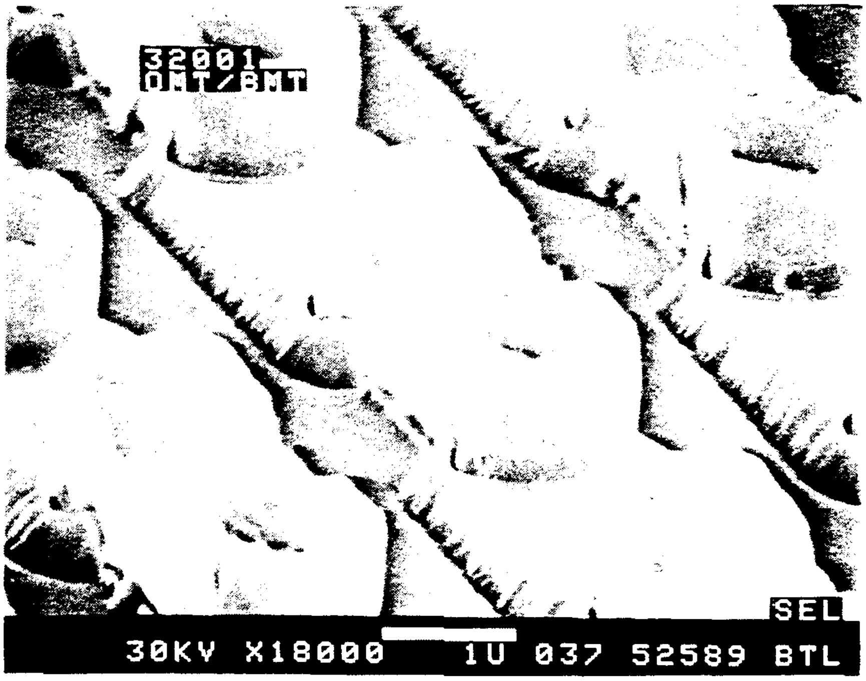
Gate metal is patterned by reactive ion etching, creating a sidewall profile which is concave (see Figure 7). The dielectric covers the features conformally and cusps around the gate. Cusping is not observed over ohmic, which is patterned with a liftoff process and has a smooth rounded profile which the dielectric covers smoothly. Since the FET characteristics are very sensitive to the gate process, steps were taken to change the dielectric coverage without changing the gate profile.

We developed a sidewall process, based on a thick dielectric deposition and etchback. Deposition of 6000Å of SiON followed by reactive ion etching in CF_4 resulted in a smooth profile of dielectric over the gate with no cusping (see Figure 8). Since the sidewall etch is endpointed over GaAs and requires an overetch for uniformity, damage to the substrate was observed. Preliminary experiments show that annealing at 390°C for 30 seconds removes the majority of damage observed in threshold voltage and current. Al is then deposited and etched with no sign of stringers or shorts.


ALUMINUM INTERCONNECTS
Aluminum
Barrier
SiON 4000 Å
Ohmic contact or Gate tab

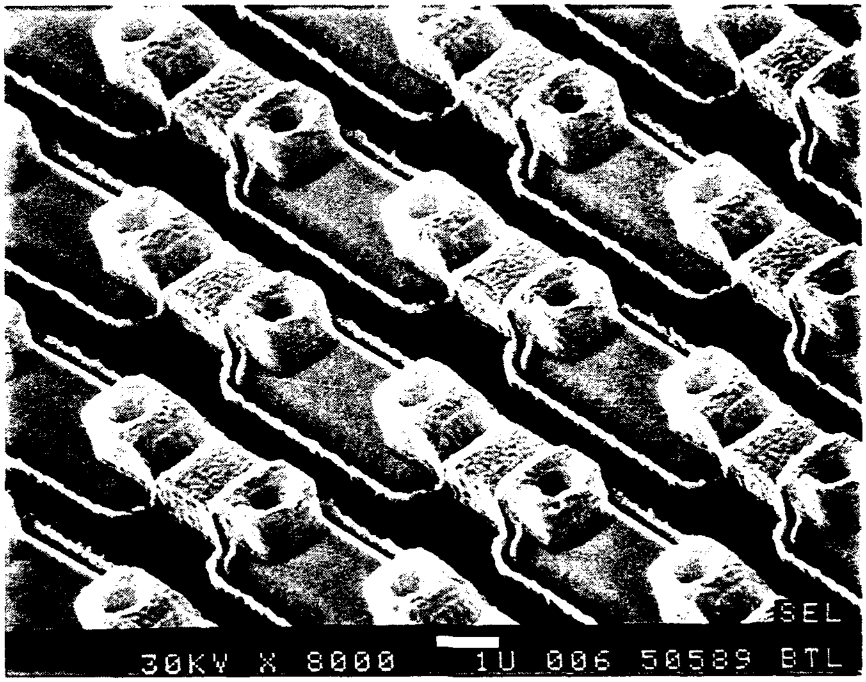
Schematic diagram of Al interconnect with the WSi_x diffusion barrier.

Figure 3.


32001
OMT/BMT
SEL
30KV X18000 1U 037 52589 BTL

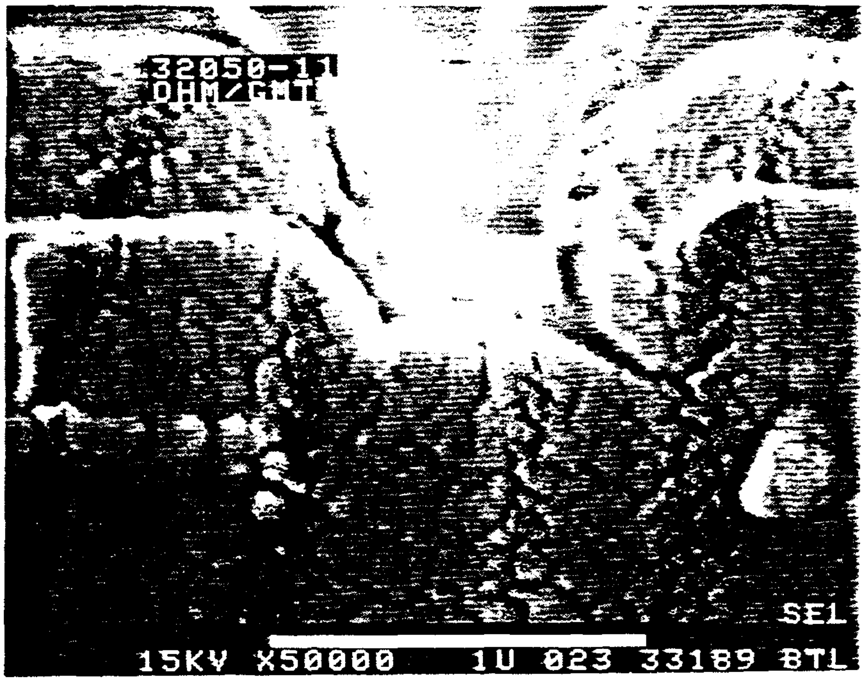
SEM of patterned Al lines over ohmic metal features.
The ohmic metal is covered with 4000Å of SiON.

Figure 4.


SEL
30KV X 8000 1U 006 50589 BTL

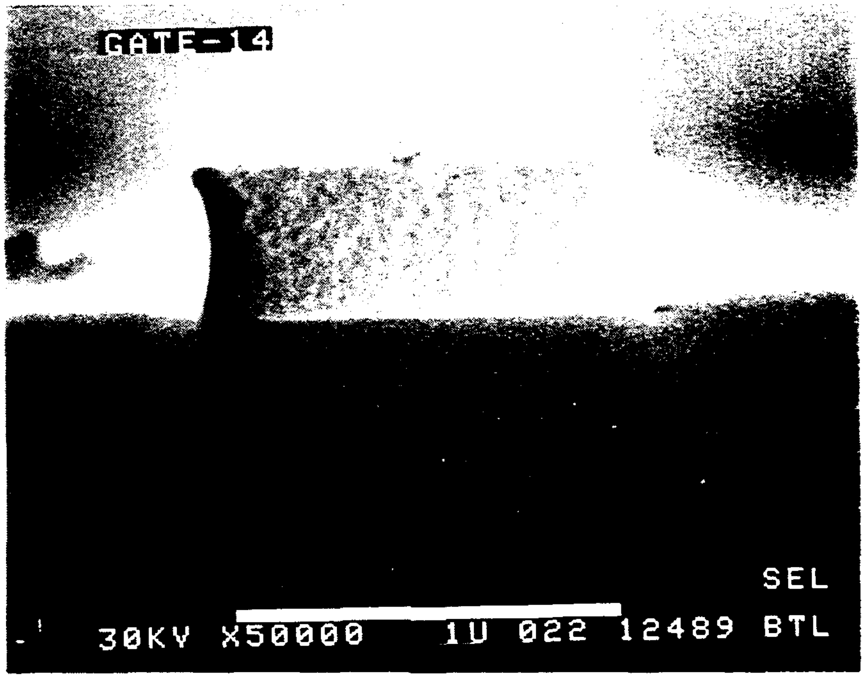
SEM of patterned Al lines over gate metal.
Notice the remaining Al (stringers) around the SiON
which covers the gate feature.

Figure 5.


32050-11
OHM/GMT
SE1
15KV X50000 1U 023 33189 BTL

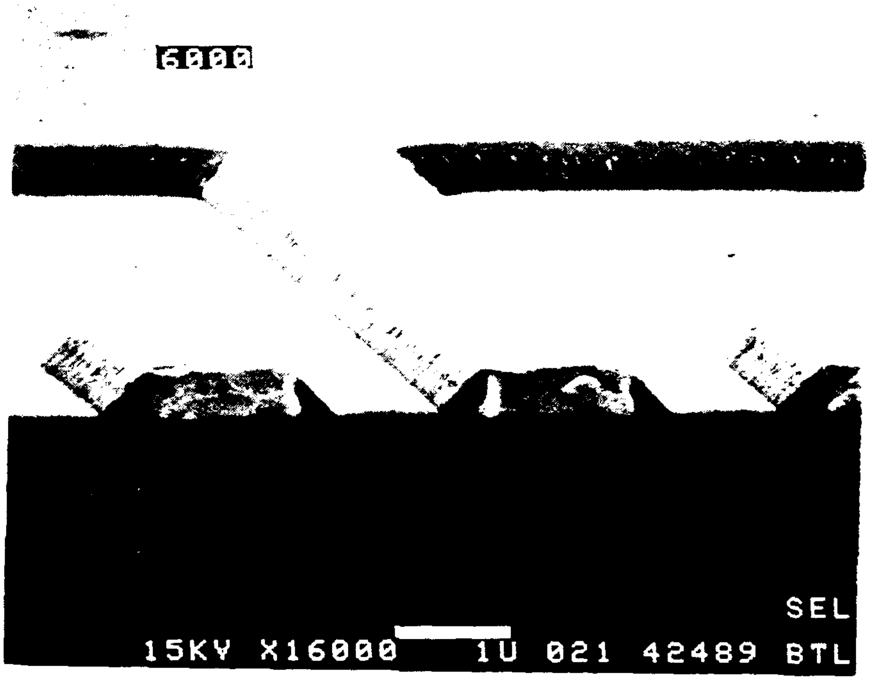
SEM which shows the dielectric (SiON) coverage over ohmic and gate metal. The ohmic is patterned with a liftoff process and has a rounded profile which the SiON covers smoothly. The gate is patterned with a subtractive etch process and is concave creating a cusp in the dielectric profile resulting in Al stringers.

Figure 6.


GATE-14
SEL
30KV X50000 1U 022 12489 BTL

SEM showing the WSi_x gate profile.

Figure 7.


6000
SEL
15KV X16000 1U 021 42489 BTL

The profile of the gate is changed with the integration of a sidewall to prevent cusping.

Figure 8.

Second Level Aluminum

Design rules specify that second level interconnect is only allowed to contact first level interconnect, so that a barrier for Au/Al diffusion is not required. Following via 2 formation, second level Al is deposited and etched. Preliminary work showed Al filaments over first level Al due to the vertical profile of the Al lines. To circumvent this problem the sidewall process was also introduced following first level Al. Successful integration of this step has been achieved with no observation of Al stringers or shorts.

An aspect ratio of approximately 1:1 (width to depth of the trough) following second level dielectric and sidewall deposition is observed prior to second level Al metallization. Complete removal of Al in the trough is necessary to prevent premature failures due to shorts. The process described so far shows mixed results as observed by SEM pictures and comb/serpentine electrical testers, with some samples showing complete Al removal, and others showing severe shorting. These results indicate the necessity for a more robust process utilizing planarization.

Planarization

The process of choice for aluminum metallization includes fully planarized interlevel dielectric. Following first level metallization (ohmic and gate), a 10,000Å thick layer of SiON is deposited. The SiON contours to the features of the ohmic and gate metals leaving a non-planar surface. Photoresist (10,250Å) is then spun-on to achieve a planar profile (see Figure 9). A CF_4/O_2 etch is used to etch the photoresist and the SiON at comparable rates (2300 to 2400Å/min.). This leaves a planar profile of SiON (4000Å) over the ohmic and gate metal. This process works over 1.0μ gate and ohmic features (see Figure 10) and can be incorporated for multi-level metal schemes.

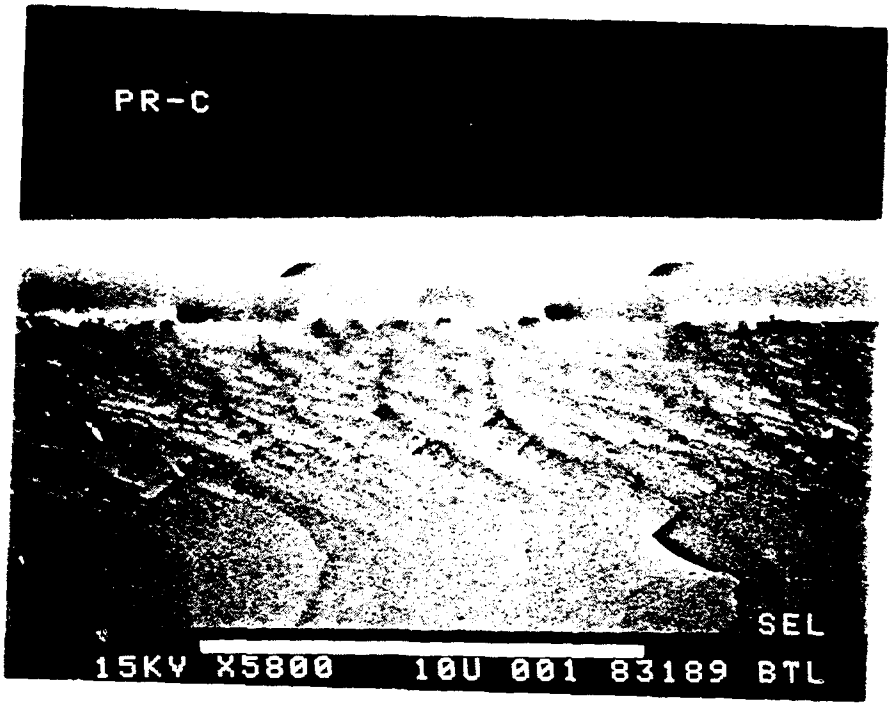
Future Work

At this stage, we have demonstrated all the steps of aluminum processing needed for the Advanced Technology. Since our goal was to investigate feasibility, there is no need to proceed further. If this process were placed into production, two further steps would be needed. First, the interlevel dielectric planarization process must be integrated with the rest of the process. Second, we saw intermittent burrs in the liftoff of the thin WSi used as a barrier between gold and aluminum. We need to develop a via plug process that will function as a barrier to diffusion and purple plague, eliminate liftoff of sputtered metal, and improve topography.

2.2 Process Tester Characterization (A. G. Baca, D. D. Manchon, R. J. Shul)

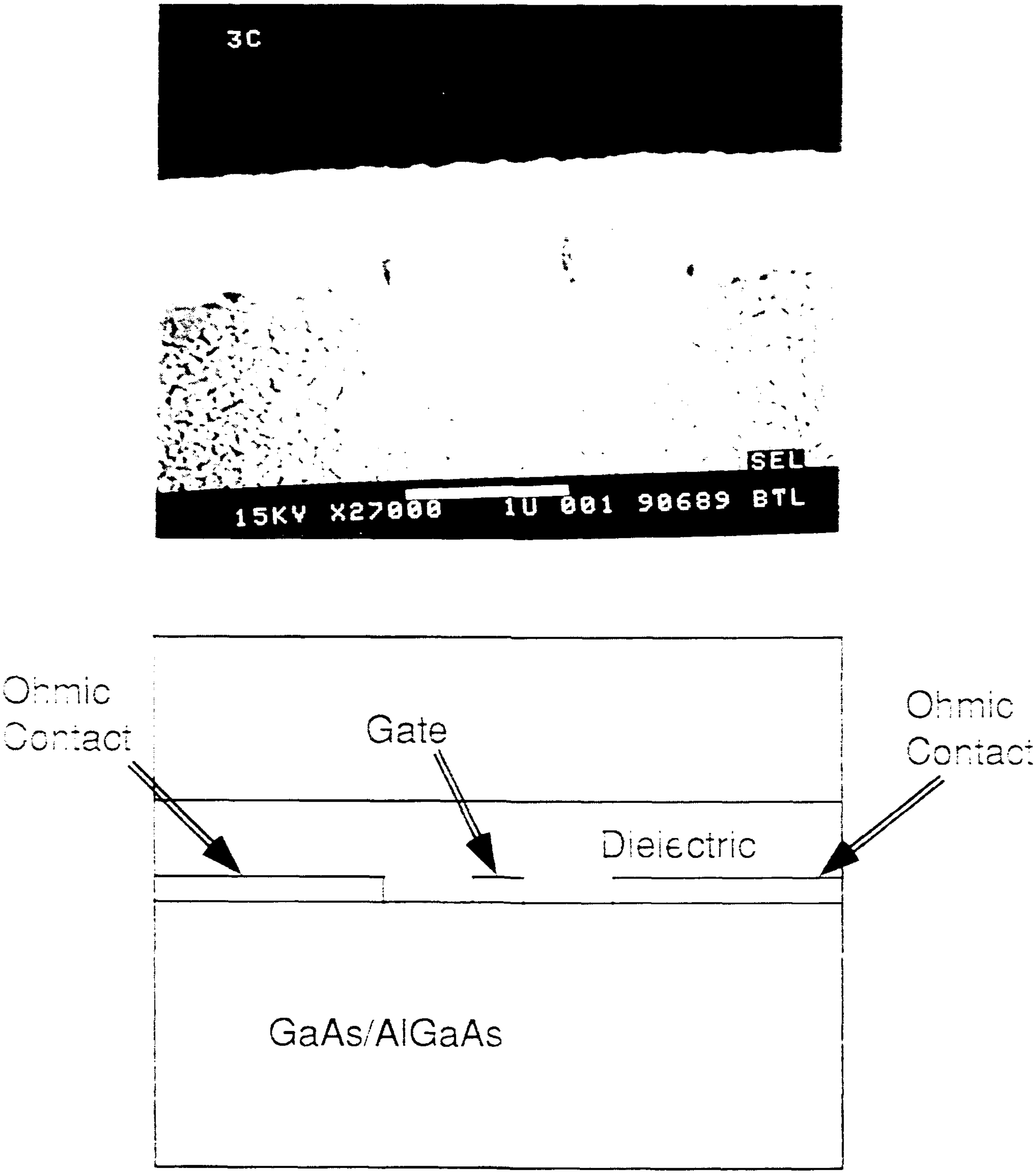
Compared to our Baseline Technology, the Advanced Technology process consists of HFETs and interconnect metallization shrunk by 25% (except for vias which are shrunk from 1.5 μm to 1.0 μm). We use the same MBE substrate as in the Baseline Technology. Process characterization falls into two categories: assessing expected yield based on our ability to fabricate the smaller features, and assessing our ability to maintain parametric control with the short channel HFET. We characterized the Advanced Technology using both gold-based and aluminum interconnects to separately show the effects of shrinking the size and of changing to aluminum.

Threshold voltage control was monitored for 21 wafers from five lots with 0.75 μm nominal gates (actual gate length measured 0.65 μm compared to 0.90 μm for the Baseline Technology). Figures 11 and 12 show inter- and intra-wafer variation. The variability is 2-3x greater than the


PR-C
SEL
15KV X5800 10U 001 83189 BTL

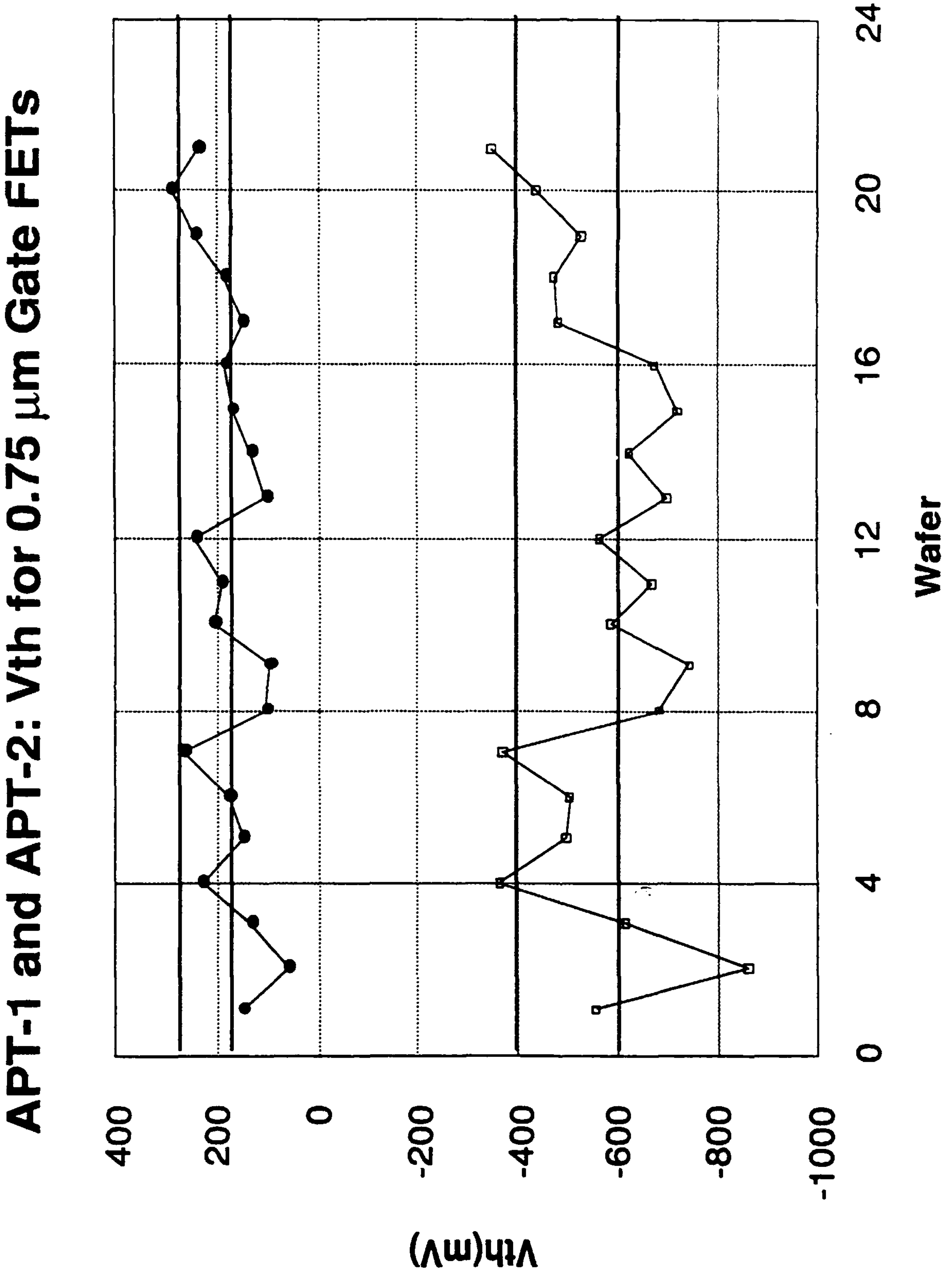
A nearly planar profile is achieved by thick deposition of dielectric followed by spinning on a thick layer of photoresist.

Figure 9.


3C
SEL
15KV X27000 1U 001 90689 BTL
Ohmic Contact
Gate
Ohmic Contact
Dielectric
GaAs/AlGaAs

A planar profile can be obtained if the etch rate of the photoresist and dielectric are comparable.

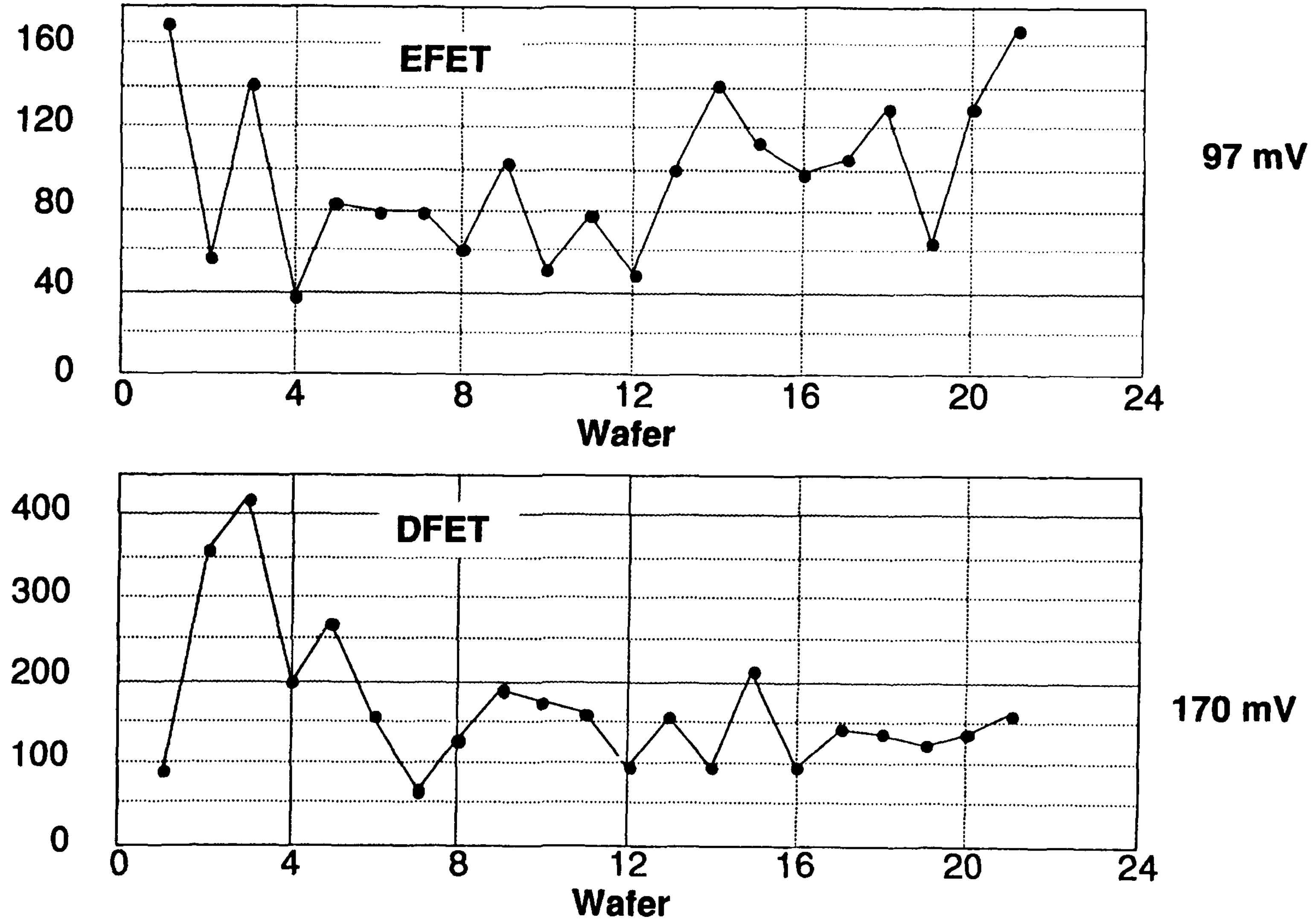
Figure 10.



Wafer-to-wafer threshold variations for EFETs and DFETs in the Advanced Technology.

Figure 11.

APT-1, APT-2 Intra Wafer Variation for 0.75 μm FETs



Intrawafer standard deviations of thresholds for EFETs and DFETs in the Advanced Technology.

Figure 12.

Baseline Technology of the same era. We expect that some of this variation can be reduced through using process Failure Mode Analysis (FMA) to uncover and eliminate sources of variation, as has been done in the Baseline Technology. However, short channel effects are responsible for a major part of this variation, and it is expected that a process enhancement such a lightly-doped drain structure will be required to further reduce the variation.

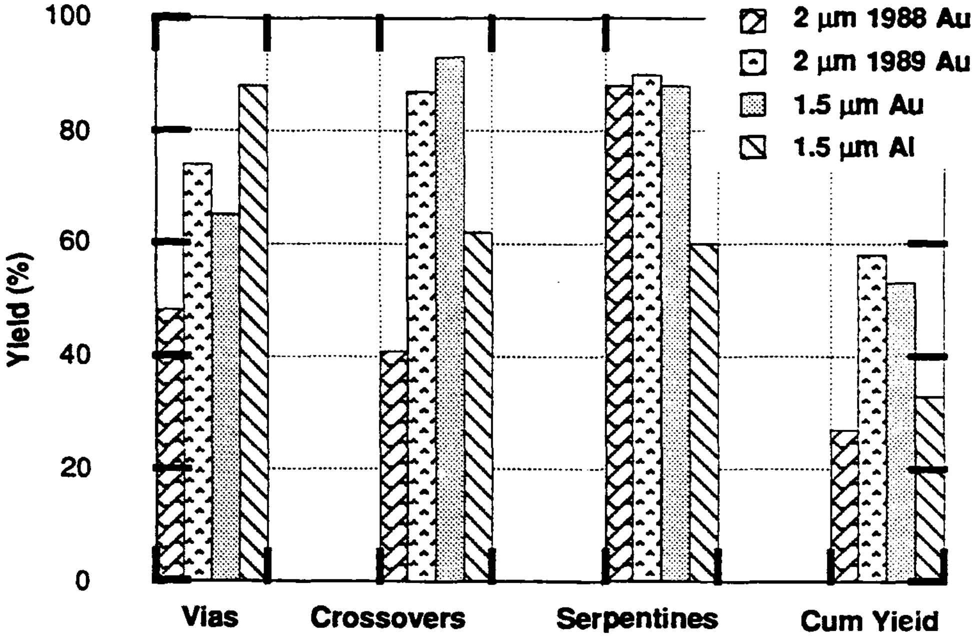
A three level metal tester, one FET level and two interconnect levels, was designed and used to characterize the Advanced Technology metallizations with 1.5 μm design rules. This new tester, called PT-Y, was used to compare the Al process with the Au-based liftoff process, as well as to compare 2.0 and 1.5 μm design rules. Metal shorts within a process level are tested by means of serpentine/comb testers (serpentines interleaved with combs) of up to 19 cm of adjacent metal. Dielectric integrity and shorts between metal levels are tested by means of combs and/or serpentine testers on different levels with up to 250,000 crossovers in 1.5 μm design rules and up to 181,500 crossovers in 2.0 μm design rules. Vias are tested by serpentines connecting different metal levels with up to 250,000 vias in 1.5 μm design rules and up to 181,500 vias in 2.0 μm design rules. A via tester is labeled "good" when the entire via serpentine is continuous with the proper resistance. A serpentine/comb metal crossover tester is "good" when the entire site shows no shorts between metals tested. Data are presented as actual or extrapolated to 250,000 for vias and crossovers.

A summary of the results is shown in Figure 13. The 1988 Au data comes from PT-X in early 1988. The Au data for 1989 comes from 20 wafers processed in four PT-Y lots. The figure shows that the baseline 2.0 μm technology showed major improvement from the early 1988 results. Compared to the 1989 2 μm Au, the 1.5 μm Au yielded somewhat lower for vias and serpentines and slightly higher for crossovers. For 1.5 μm gold, both the area and feature size are smaller. The smaller area tends to increase the yield, and the smaller feature size decreases the fatal defect size and thus lowers the yield. The net effect is a slightly lower yield for the 1.5 μm design rules. No lots had catastrophic failures with 1.5 μm design rules using liftoff processing; however, this technology is expected to be much more difficult to control in production. Compared to 1989 2 μm Au, the cum yield (the product of the via, crossover, and serpentine yield) is 10% less for 1.5 μm design rules using Au.

The aluminum data comes from ten wafers from two PT-Y lots. The Al process with 1.5 μm design rules yielded greater for the via process because of the better metal coverage into the via. However the crossover and serpentine yields are lower. As noted in the previous section, incomplete removal of Al in the high aspect ratio troughs is responsible for the lower serpentine yields. This problem will be eliminated by planarization. The extremely vertical Al profile and resultant sharp metal edges put more stress on the dielectric and are probably responsible for the lower crossover yields; planarization should improve this yield, also. The cum yield for the advanced Al process is 38% less than for the advanced Au process. However, the higher via yields demonstrate the promise of an Al process.

We conclude that very acceptable metallization yields have been achieved with 1.5 μm design rules. We believe that the process of choice is a fully planarized Al process using the methods described in the previous section.

Interconnect Comparisons



	Baseline		Advanced	
	Au PTX	Au PTY	Au	Al
Via Yield*	48%	74%	65%	88%
Crossover Yield*	41%	87%	93%	62%
Serpentine Yield**	88%	90%	88%	60%
Cumulative Yield	17%	58%	53%	33%
Via Do (cm-2)	17.8	7.2	20.1	5.3
Crossover Do	22	3.5	2.7	21
Serpentine Do	8.2	8.6	18.8	75

* Yield for 250,000 via (crossover) testers

** Yield for 19 cm of metal - metal runners at minimum space

Comparison of interconnect yields in the Advanced Technology

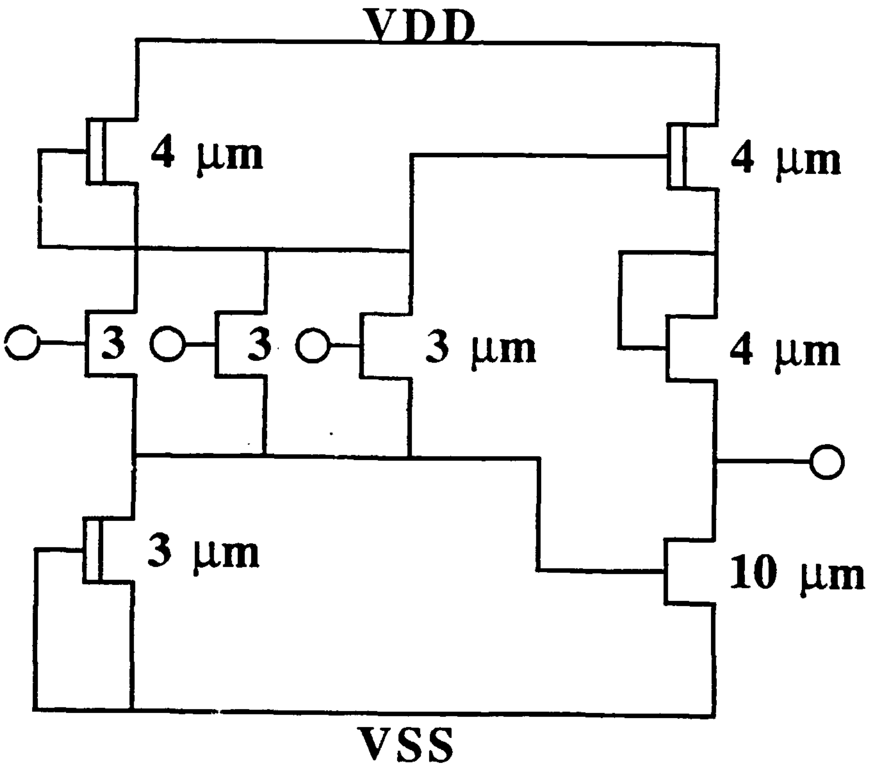
Figure 13.

3. TEST CIRCUITS

Two mask sets were designed to test the performance of the Advanced Technology: APT-1 tests characteristics of FETs and the logic family. APT-2 tests multiplier performance. Both mask sets could be fabricated with either gold or aluminum interconnect metallization. Since development of the aluminum process proceeded in parallel with circuit testing, we often used gold interconnects to test concepts before the aluminum process was ready.

3.1 Ring Oscillator (P. J. Robertson, A. I. Faris, A. G. Baca)

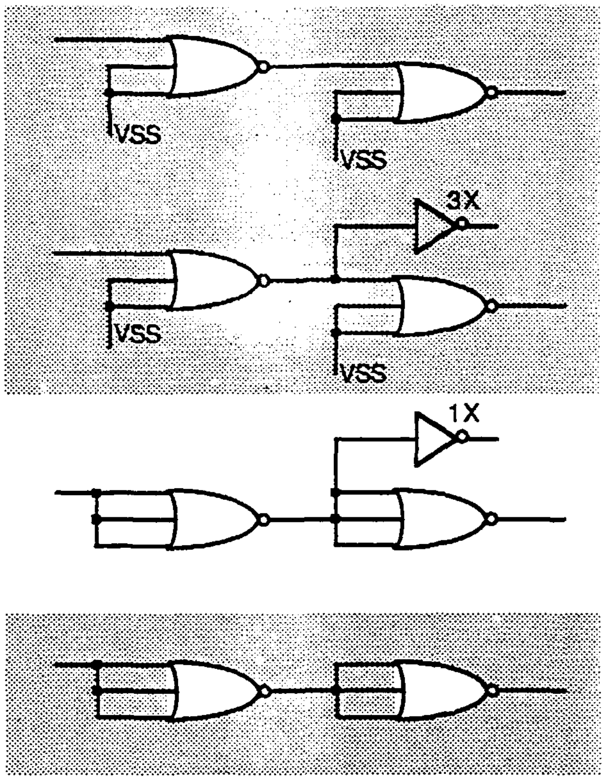
The APT-1 mask set consisted of 31-stage ring oscillators with logic elements that used the Low power Source Follower FET Logic (L-SFFL) logic family. A schematic of a typical 3-input nor gate is shown in Figure 14. The logic stages used in the ring oscillators were of four basic types varying in the number of fanins and fanouts as shown in Figure 15. We used gold interconnect metallization to fabricate wafers using the APT-1 mask set. (At this early stage of development, aluminum wasn't ready.)



L-SFFL 3-Input NOR Gate

Figure 14.

The L-SFFL logic gates were designed and simulated using the SargicS.11 models to operate with a E/D current ratio of 0.71. The actual as-processed wafers had E/D current ratios that were as small as 0.29. This resulted from negative threshold shifts in the transistor characteristics brought about by the shorter gate lengths[1] used for the Advanced Process.



Circuit variations for APT-1 Ring Oscillators.
Fanin = 3 and Fanout = 4 was chosen for comparison since FET characteristics were shifted off-target by the short gates.

Figure 15.

Table 1 shows Process Control Module (PCM) data for the FETs on APT-1, where EFET currents are measured at $V_{gs} = 0.5$ V and $V_{ds} = 2.0$ V, and DFET currents are measured with $V_{gs} = 0.0$ V and $V_{ds} = 2.0$ V.

---

[1] The standard Sargic process has a nominal gate length of 1.0 μm. The Advanced Process used nominal gate lengths of 0.75 μm.

TABLE 1 — FET Current Characteristics for PCM Measurements vs. the Nominal SargicS.11 Model Values. The SargicS.11 models were used to design the APT-1 circuits.

	EFET (V_{gs} = 0.5 V)	DFET (V_{gs} = 0.0 V)	E/D Current Ratio
SargicS.11	50 mA/mm	70 mA/mm	0.71
Lot 31710	50 mA/mm	170 mA/mm	0.29
Lot 31920	75 mA/mm	125 mA/mm	0.60

Since the current ratios did not match the design specifications, it was necessary to drive all three inputs of a 3-input NOR gate in order to get proper logic levels. Thus, we evaluated the data from ring oscillators with fanin = 3 and fanout = 4. Comparisons were made between three wire load lengths (0, 200 and 500 µm). The power supply voltage was 2.0 volts.

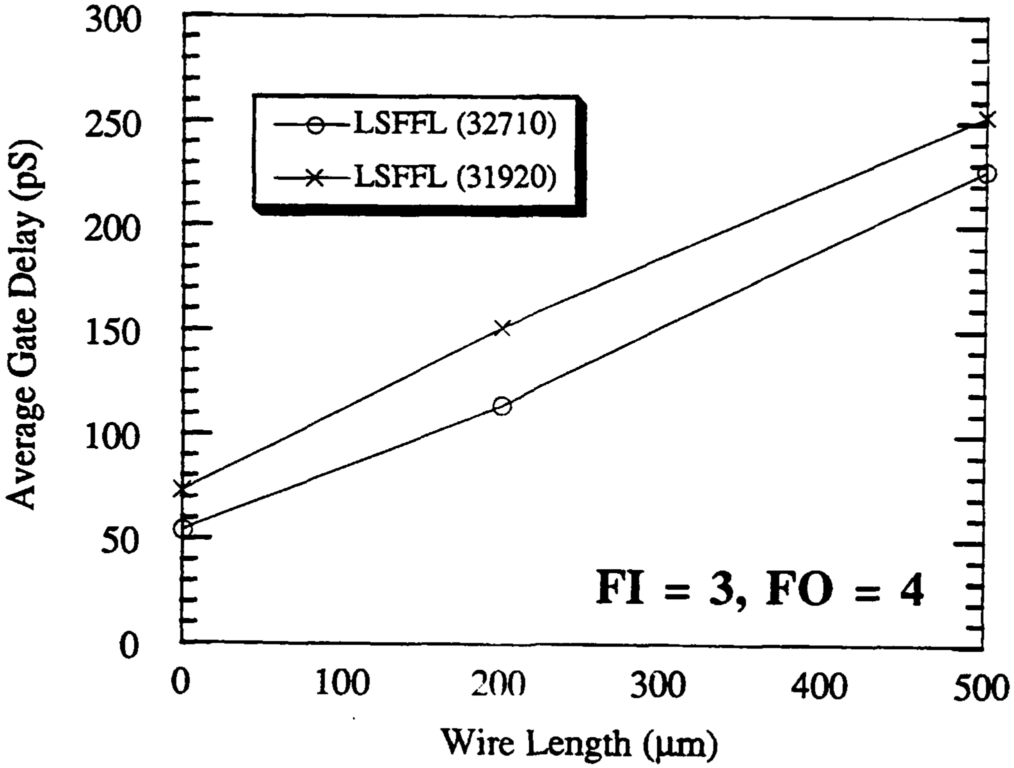
Measurements from Lots 31710 and 31920 are summarized in Table 2. The speed of operation of circuits in lot 31710 would be slightly less than 1GHz with 20 gate delays.[2] These results indicate that the Advanced Technology circuits surpass the Advanced Technology objective of 400 MHz operation with 20 gate delays. The power*delay product for the Advanced Technology circuits is excellent. Lot 31710 has a power*delay product of 49 fJ and lot 31920 had 42 fJ. The data in Table 2 is shown in graphical form in Figure 16.

TABLE 2 — Summary of the Average Gate Delay Measurements for APT-1.

	Average Gate Delay	
Length	Lot 31710	Lot 31920
0 µm	54 pS	73 pS
200 µm	114 pS	151 pS
500 µm	227 pS	253 pS

---

[2] Maximum frequency with 20 gate delays: Lot 31710 = 926 MHz; Lot 31920 = 685 MHz.



Plot of Average Gate Delay Versus Wire Length

Figure 16.

3.2 8 x 8 Multiplier (R. J. Niescier)

To demonstrate the capability of the Advanced Technology in a meaningful circuit, we chose a standard cell design that was previously fabricated in the Baseline Technology 2.0 µm AT&T HFET process. The two's complement 8x8 integer multiplier from PT-2L was chosen because it contained eleven unique standard cells which were grouped into only five macrocells. Because it was a standard cell design, only the macrocells had to be redesigned and our standard cell router would place the power busing and interconnect. The placement of the macrocells was already determined by the previous design. We could therefore investigate the Advanced Technology performance with a minimal investment in design and layout resources.

The function of this multiplier is to accept two eight bit two's complement integer numbers and produce a sixteen bit two's complement result. The partial product reduction is accomplished with a simple carry-save array and the final summation is performed by a carry propagate adder. The gate count in the critical path is 46 and the total gate count of one multiplier is 889.

The ease with which this circuit could be redone allowed the addition of two more modifications to the multiplier. Two more primary sites, in addition to the control site and the standard Advanced Technology site, were designed as experiments for side-gating and scaling. The side-gating site was identical to the Advanced Technology site except that the FETs were packed as closely as possible with some even sharing the same isolation area. The scaling site was identical to the control site except that it was linearly shrunk from the 2.0 µm rules to the advanced 1.5 µm rules. This experiment, if successful, would allow the linear shrink of the baseline circuits with only a minimum NRE cost, instead of a large redesign and layout cost. All these designs were placed on the APT-2 mask set, where each reticle field contained four sites:

- Site 1: A direct copy of the PT-2L Multiplier using 2.0 µm design rules.
- Site 2: A linear shrink of all components of the PT-2L multiplier to test scaling effects. In Site 2, a feature is 75% of the size in Site 1.
- Site 3: Like Site 4 (the standard Advanced Technology site), except that the FETs were packed as closely as possible, sometimes sharing the same isolation area.
- Site 4: The standard Advanced Technology design using 1.5 µm lines and spaces. In this case, to try to avoid scaling problems, the minimum gate width was kept the same as the Baseline Technology.

We demonstrated circuit performance in APT-2 with gold metallization and 0.75 µm gates (except for Site 1, which uses 1.0 µm gates). Aluminum metallization was also attempted, but the lots were fabricated before the barrier metal process was fully developed, and they all failed due to gold/aluminum interactions. Because 1.0 µm gates give different FET thresholds than 0.75 µm gates, Site 1 failed to function.

For the required 400 MHz operation with 15 - 20 gate delays, we require operation at 125 ps/gate. Of 312 multipliers tested, 56 functioned at some value of V_{DD}, I/O voltage, and speed; 26 worked at 125 ps/gate or faster. Four circuits repeatably ran at 90 ps/gate at close to the 2.0V target supply voltage. For the functioning sites, circuit performance is given in Table 3.

TABLE 3 — APT-2 YIELDS

Site	Functional	Speed	I/O	Average Current
2	12%	6%	0%	0.561 A
3	24%	11%	8%	0.447 A
4	17%	8%	4%	0.482 A

Functional: passed test vectors at some I/O, speed, and V_{DD}
Speed: faster than 125 ps/gate at some I/O and V_{DD}
I/O: functioned at V_{DD}=2.0 V, V_{ih}<1.0 V, V_{il}>0.3 V, for any speed

These tested devices all came from two wafers, and there was noticeable variation in performance for different areas in the wafers. For example, chips from the tops of the wafers drew twice the current of chips from the bottom. Also, while all input buffers in these three sites were the same, there was considerable I/O performance variation. This makes it hard to draw specific conclusions, but some general trends are clear. First, Site 2 (the linear, or "dumb" shrink) did not perform well. Its characteristics are similar to those seen previously when small FETs show threshold shifts compared to larger EFETs. Because of the dumb shrink, Site 2 contains EFETs with small widths (i.e., 3-5 µm). Second, while Site 3 shows higher yields than Site 4, Site 4 seems to produce more robust circuits. That is, while none of the tested circuits on APT-2 simultaneously meet speed, power supply, and I/O specifications, Site 4 has the most sites with better performance. These are limited data, but we believe that appropriately separated FETs with proper isolation (i.e., Site 4) lead to the best performance.

Extrapolation of Circuit Yield

The objective of the Advanced Technology is to achieve both suitable performance and a predicted 3% DC functional yield. As described above, we developed this process along parallel paths. Along one path, we developed an aluminum metallization process. Simultaneously, along the other path, we used gold interconnects (with 1.5 μm lines and spaces) to demonstrate circuit performance.

For vias, serpentines, and crossovers, we showed above that 1.5 μm gold interconnects have a 10% lower yield than 2.0 μm gold interconnects (see Section 2.2). In addition to that, there are two ways to look at the circuit yield.

- Table 3 shows a 17% functional yield for Site 4. This compares with a 27% yield achieved in prior data with the PT-2L version of the same circuit. This is a 37% yield reduction for the Advanced Technology.
- Alternatively, we can compare PCM yields for the two technologies in comparable time periods. Then the Baseline Technology has a 28% PCM yield, while the Advanced Technology has a 6.4% PCM yield. This is a 77% yield reduction for the Advanced Technology.

Multiplying the interconnect yield times the circuit yield, we find that the Advanced Technology has a 21 - 57% yield compared to the Baseline Technology. That is, when the Baseline Technology achieves a 10% yield, the Advanced Technology is expected to have a 2.1 - 5.7% yield. This compares to the 3% goal.

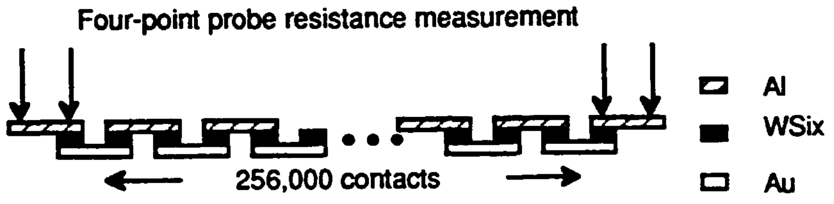
We showed in Section 2.2 that the via, serpentine, and crossover yield is 38% lower for 1.5 μm aluminum than for 1.5 μm gold. However, that yield was obtained with an aluminum process that omitted the desired planarization step. When planarization is integrated into the aluminum metal process, we expected a yield comparable to or better than gold.

4. RELIABILITY AND RADIATION TESTING

4.1 Diffusion Barrier Thermal Aging (P. F. Thompson)

As part of the aluminum metallization process, we introduced a diffusion barrier to prevent gold-aluminum interactions at the ohmic contacts (see Section 2.1). We used thermal aging test wafers to get a preliminary indication of the diffusion barrier performance.

Wafers in the thermal aging study used test structures containing a series connection of ohmic metal (Au) - metal 1 (Al) interfaces (with the intervening WSi_x diffusion barrier) (Figure 17). The test structures are called via chains. Two wafers were aged; one passivated with 4000Å SiON dielectric over the metal, and one with no dielectric. There were 15 test structures measured on the non-passivated wafer, and 24 test structures measured on the passivated wafer. Aging lasted 1000 hours at 200°C. Four point resistance measurements were taken at intervals during the aging process.



Via chain test structures

Figure 17.

After 1000 hours, there were no failed (open) via chains or increases in via chain resistance. In fact, resistance decreased during aging. The decrease closely fit an exponential decay to a constant resistance, suggesting additional annealing of the metal structure. While no quantitative prediction of lifetimes was possible (or intended) from this preliminary study, some indication of the diffusion barrier effectiveness is possible. Since this study consisted of non-biased thermal aging, gold-aluminum interdiffusion (as opposed to aluminum electromigration) would be the likely failure mechanism. Peck & Zierdt (Proc. IEEE, Feb., 1974) presented Al-Au bonding failure data in a review article showing activation energy data and relating temperature to time to fail. From their data, 0.1% failures would be expected after 1000 hours at 200°C. One failure in a via chain would be $3.9 \times 10^{-4}\%$ failures. Even if the first failure in the test patterns occurred at 1000 hours, the cumulative percent failures is 256 times less for the test pattern, based on a single via chain, than for direct gold-aluminum contact. Although we can't say the via lifetime will in fact be 256 times that of gold-aluminum bonds, the results indicate a significant beneficial effect from the WSi_x diffusion barrier.

4.2 Interconnect Reliability (P. F. Thompson)

Electromigration testing was performed on both gold and aluminum interconnects. The goal of the tests was to predict interconnect reliability for AT&T's metallization processes as of February, 1990. No prior electromigration tests had been performed on aluminum, and no recent tests had been performed on gold. The following sections describe the experimental plan, procedure and results, and data analysis.

Experimental Plan

Equation 1 describes metallization electromigration lifetime.

$$L_2=L_1\exp[E_a/R(1/T_1-1/T_2)]X(j_1/j_2)^n \qquad (1)$$

where:

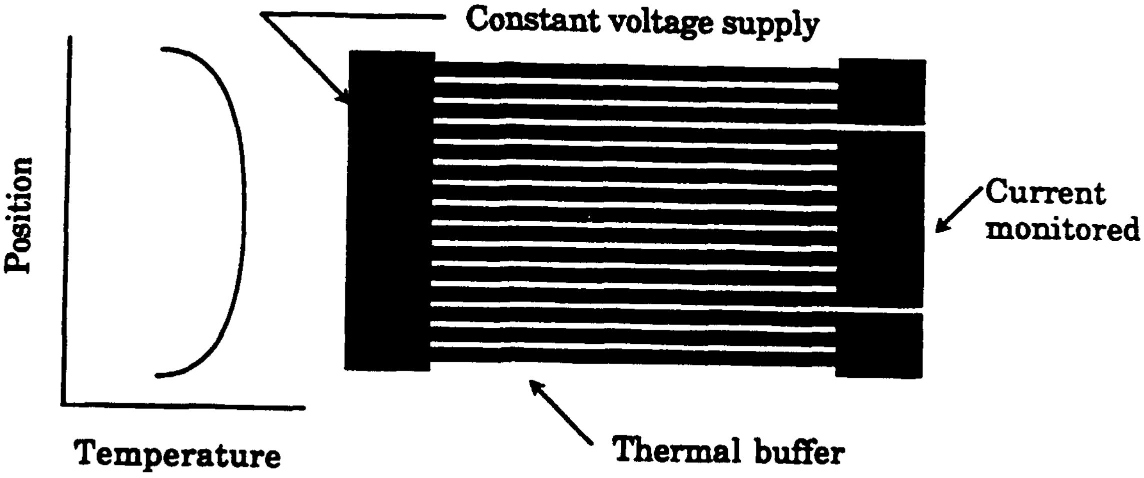
L_i=lifetime at condition i
T_i=temperature at condition i
j_i=current density at condition i
E_a=activation energy
n=current acceleration exponent

By aging test structures at multiple temperature and current density combinations as shown in Table 4, we expected to compute "best fit" values of E_a and n for each metallization (aluminum and gold). The test structure used three groups of parallel lines as shown schematically in Figure 18. The central group was bracketed by smaller side groups intended to serve as temperature buffers. We chose the current densities to span a wide range while minimizing joule heating. Then the temperature of the central group is essentially constant as indicated at the left side of Figure 18.

TABLE 4 — Test conditions for electromigration testing.

ALUMINUM			
T(°C)	$j(10^5 Acm^{-2})$		
	5.21	10.5	16.3
150°C	X		X
175°C		X	
200°C	X		X

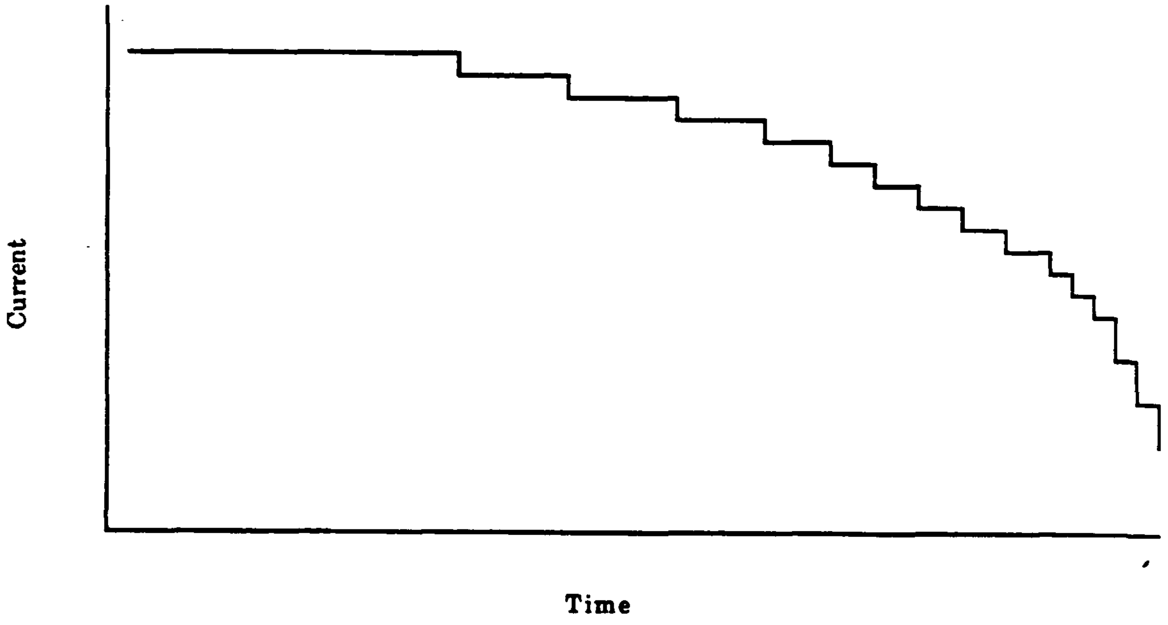
GOLD			
T(°C)	$j(10^5 Acm^{-2})$		
	3.92	10.0	15.7
150°C	X		X
175°C		X	
200°C	X		X



Parallel Line Test Structure

Figure 18.

These test structures were packaged and placed in ovens with automatic data acquisition. Data were recorded essentially continuously (one recording for each 1/100 of the time on test). Approximately 20 testers were used at each combination of temperature and current density. Voltage was maintained constant, and current was monitored. As indicated in Figure 19, failure of a conductor line results in a step decrease in current. We used about 50 lines per tester, so the data for each tester provides a failure time distribution.



Current vs. time curve for a parallel line test structure. Each step change indicates one or more stripe failures. The number of failures can be determined from the step height.

Figure 19.

Experimental Results

Unfortunately, we only obtained failure distributions in 2 of the 10 experimental cells. First, there were no gold failures within the duration of the experiment (2000-2300 hours). Second, a computer crash during the 50-100 hour interval destroyed all data in that interval and also destroyed the initial values of the 150°C aluminum cells. Consequently, median lifetimes were obtained for only aluminum aging at 175°C (10.5 x 10^5 Acm^{-2}) and 200°C (16.3 x 10^5 Acm^{-2}), as shown in Table 5.

TABLE 5 — Median lifetimes in hours at accelerated conditions.

ALUMINUM			
T(°C)	j(10^5Acm^{-2})		
	5.21	10.5	16.3
150°C	(1)		(1)
175°C		91	
200°C	<100(1)		0.65

GOLD			
T(°C)	j(10^5Acm^{-2})		
	3.92	10.0	15.7
150°C	>2295(2)		>2295(2)
175°C		>1950(2)	
200°C	>1950(2)		>1950(2)

1. Data lost in computer crash.
2. No failures.

Despite the experimental difficulties, this experiment clearly shows the status of the two metallizations: Gold from this vintage is consistent with expectations, where aluminum has noticeable short comings. By using information from the literature, we can compute various expected lifetimes based on the data we collected. For aluminum, we use $E_a = 0.5$ eV and $n = 1.5$; for gold we use 0.7 eV and 1.5. (These are the generally accepted values and/or the values in the center of the reported ranges.) Table 6 gives expected lifetimes for aluminum at 2.0 x 10^5 Acm^{-2} (the MILSTD 883C limit) and gold at 4.0 x 10^5 Acm^{-2} (AT&T's limit for GaAs interconnect). As indicted in the footnote to the table, the gold metallization actually has a longer life than given in the table, because (for the purpose of illustration) the table assumes gold failures at the end of the test duration even though there weren't actually any failures.

TABLE 6 — Lifetimes for different use conditions.

Use Temp (°C)	Aluminum (hours)	Minimum Gold (hours)*
100	15000	1.5x10^6
125	5600	3.9x10^5
150	2400	1.2x10^5

*Assumes median gold failure time is the test duration, although no failures had actually occurred at that point.

These relatively short lives for aluminum metallization are disappointing. Visual inspection of the aluminum metallization failures showed voids at random locations. There was no evidence of corrosion or failure at the bus locations, so all failures appear to be electromigration. Before this aluminum process could be used for production, we would require additional development to achieve acceptable reliability. For example, aluminum deposition conditions could be varied to alter the metallization grain size. Since other organizations successfully use aluminum metallization, this problem is clearly not insurmountable. However, since the requirement of this program was simply to demonstration feasibility, we have not undertaken further development at this time.

4.3 Radiation Testing (S. B. Witmer, M. Spector)

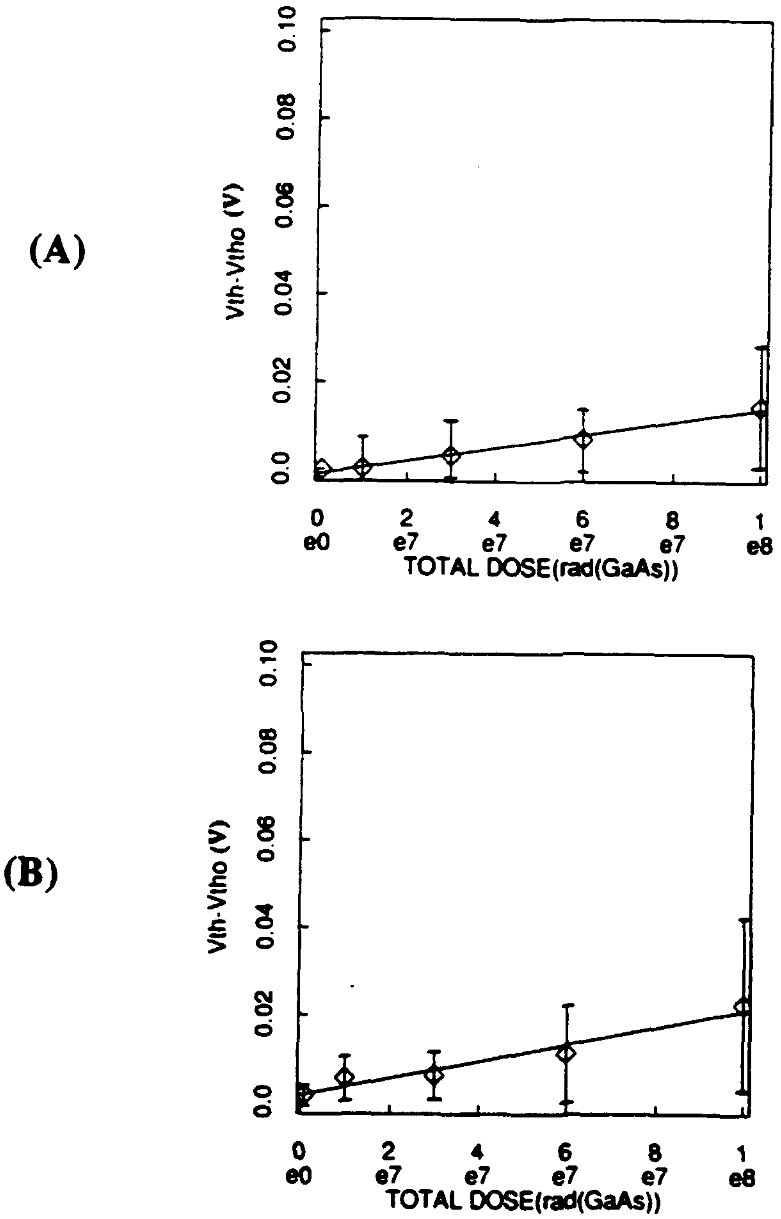
Total Dose

Total dose radiation testing was performed on (gold interconnect) Advanced Technology discrete FETs and ring oscillators. The devices were exposed to gamma radiation up to $1x10^8$rad(GaAs) from a Co^{60} source. The average change in threshold voltage (ΔV_{th}) after $1x10^8$rad(GaAs) was 18 mV and 22 mV in EFETs and DFETs, respectively (see Figure 20). In comparison, ΔV_{th} at 1 x 10^8 rad (GaAs) for the Baseline Technology was 20 mV and 40 mV. A 10% decrease in oscillation frequency in ring oscillators was also observed at $1x10^8$rad(GaAs) (see Figure 21). These results are comparable to the Baseline Technology total dose results.

Transient Ionizing Dose Testing

Transient ionizing dose testing was performed on (gold interconnect) Advanced Technology FETs and ring oscillators from two different lots. The results were lot dependent; but, in general, the radiation-induced drain current during the 30 ns radiation pulses was larger than in Baseline Technology FETs.

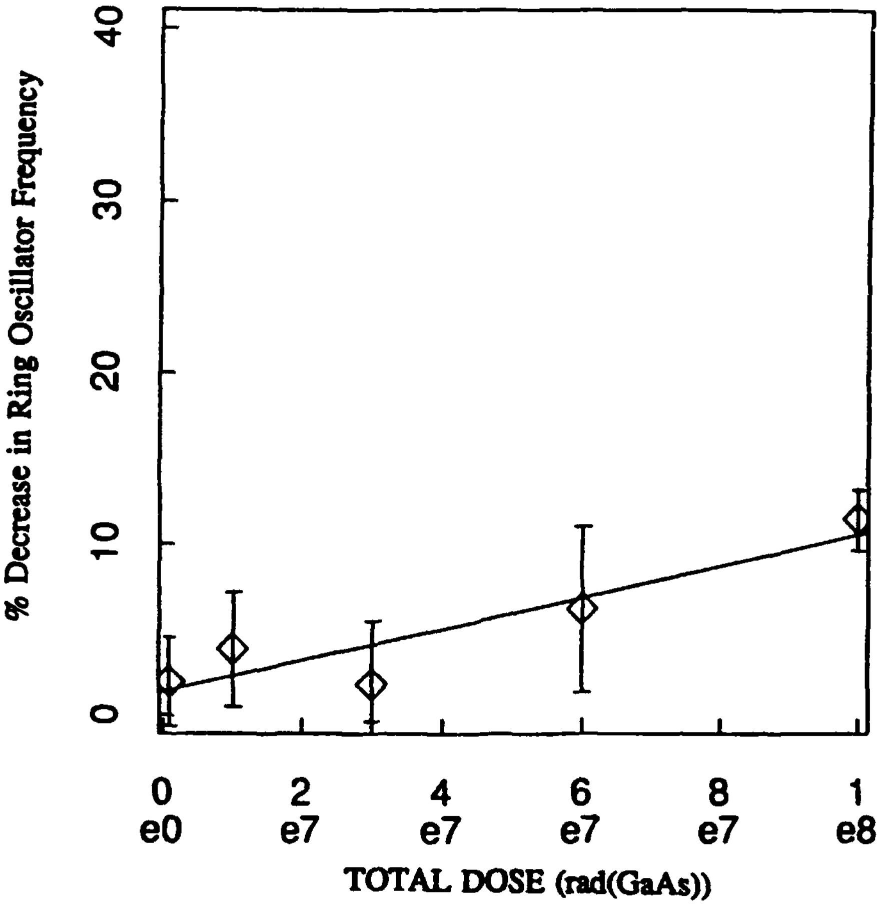
APT ring oscillators stopped oscillating at dose rates of approximately $5x10^8$rad(GaAs)/sec with recovery time in milliseconds. These results differ greatly from the Baseline Technology ring oscillators where oscillations stopped at approximately $5x10^9$rad(GaAs)/sec with prompt recovery times of less than 50 ns.



Change in threshold voltage versus total dose gamma radiation of advanced technology (APT) (A) EFETs and (B) DFETs.

Total dose effects in Advanced Technology HFETs (Gamma Radiation)

Figure 20.



Total Dose Irradiation of Advanced Technology Ring Oscillator

Figure 21.

APPENDIX D

Industry Survey of High Speed Packages

Revised September, 1988

(R. S. Moyer and K. J. Brady)

Introduction

The industry survey of high speed packages presented in the June 2, 1988 Semi-annual Technical Report has been reproduced for this technical report with some modifications. Two sets of drawings have been added to the survey. Manufacturer's data sheets and/or drawings describing the packages listed in Tables D-1 and D-2 have been included at the end of this survey.

The contract Statement of Work says "Contractor shall survey the industry for appropriate high speed packages with Input/Output (I/O) ranging from 20 pins to 230 pins. The survey shall be fully documented in contract Semi-Annual Technical Reports." We shall interpret "appropriate high speed" term as meaning appropriate to the chips being designed for the contract, i.e. for clock speed of 200 MHz.

There are hundreds of packages available in the marketplace, but very few have the necessary combination of high-speed capability and high I/O count. Typically, a high-speed chip and its package are designed serially, with the package designed to the specific geometric and electrical requirements of the chip and also the system requirements of the circuit.

In contrast to the ideal situation described above, where the package is custom-designed to the chip and its application, this contract requires that we locate suitable high–speed packages in the marketplace in which the demonstration circuits are to be delivered. Inherent in such a strategy is the need for minimizing the performance loss possibly associated with non-custom packages.

To find the optimum commercial packages, we will consider only those packages whose characteristics are consistent with high-speed operation, and will organize the package data of this survey into areas of concern for high speed operation. A candidate package for one of our deliverable circuits can thus be analyzed for suitability by determining the performance risk associated with each area of concern listed. An overview of the areas of concern is shown in Figure D-1.

We have divided the packaged circuit into five areas of concern:

I. **Chip-to-Cavity Match** The chip obviously has to fit into the cavity, but if the cavity is too large, there is an inductance penalty in the overly-long wire bonds required.

II. **Electrical Characteristics of the Package Body** The signal rise and fall times for the circuits in the contract typically correspond to bandwidths of ~1.3 GHz, so the package must be able to transmit these signals out to the external leads at these frequences (see Figure D-2). Typically the package body should incorporate ground planes, controlled impedance signal lines, and interspersed ground and signal lines to prevent crosstalk. The performance degradation of candidate packages which don't have these design features will have to be determined on a case-by-case basis for use in the contract. Additionally, the ability to connect by-pass capacitors and terminating resistors to the package I/Os is useful for minimizing noise.

III. **External Connection Geometry** Generally, packages for IC chips fall into two broad families, through-hole mount and surface mount. The through-hole family contains the DIPs and the pin grid arrays, (PGAs). The surface mount family contains Small Outline Integrated Circuits (SOICs), chip carriers and flatpacks. Examples of these package types are shown in Figures D-3 - D-12. The through-hole mount package pins present large discontinuities where the package pin meets the board. This large discontinuity limits the use of these packages to applications to bandwidths below 500 MHz, less than half the required bandwidth for use in this contract work.

In the surface mount family the SOIC is a molded plastic package not well suited for high frequency applications. The chip carriers and the flatpacks are the package styles best suited for high frequency applications. The flatpacks offer the least discontinuity at the package/board interface and therefore is the style most used.

IV. **Thermal Characteristics** High-speed in ICs is often associated with more power dissipation than comparable circuits operating at lower speeds, and the heat must be removed to maintain junction temperatures at low enough levels consistent with noise margins and reliability.

V. **Associated Components** All else being equal, a package system consisting of test fixturing, burn-in sockets and carriers is preferred. This aspect is often overlooked, but the best package in the world has to be connected somehow to a test system for evaluation. These system components are often as expensive and time consuming to design and make as the package itself.

The relative importance factors affecting package choice for a give chip are shown schematically in Figure D-13.

THE PACKAGE SURVEY

Several manufacturers offer open-tooled packages with controlled impedance signal lines for high frequency applications. The manufacturers and the packages they offer are listed in Table D-1. Manufacturer's data sheets and/or drawings of these packages are given in the attached figures. The pin counts offered cover the range from 20 to 164 with signal line counts from 8 to 148. Listed at the bottom of Table D-1 are several package from Mini Systems Inc. (MSI), these packages do not have controlled impedance signal lines, but these packages have been tested and found to be useful at frequencies up to 2 GHz.

Two points are obvious from the entries in Table D-1: First, the packages at the top of the table have been designed to have a characteristic impedance, Zo=50Ω. The second point is that the entries in the table do not cover the high end of the pin count range. For example, the Casino Test Chip has 177 signal lines, therefore, none of the packages listed could accommodate this chip.

Devices designed to operate with 75Ω characteristic impedance signal lines would dissipate less power. Consequently, the three manufacturers listed at the top of the Table D-1 were asked about the possibility of designing packages with 75Ω characteristic impedance transmission lines. The two ceramic manufacturers, Interamics and TriQuint answered that they felt that such high impedance packages would not be manufacturable. The reason for this is the high dielectric constant of the alumina ceramic, $E_r = 9.6$, and the relation that governs the characteristic impedance Zo of a transmission line:

$$Zo = \sqrt{\frac{L}{C}} = \frac{[\text{Geometric Factors}]}{\sqrt{E_r}}$$

where L = inductance per unit length, C = the capacitance per unit length, and E_r = the dielectric constant. To produce a package with 75Ω characteristics impedance signal lines would require pushing the geometric factors to values which are impractical for manufacture. Only Rogers-Microtic using polymide with $E_r \leq 3.8$ would attempt to fabricate packages with 75Ω impedance signal lines. Some samples of packages with 75Ω signal lines have been ordered from Rogers-Microtic but have not yet been delivered and are in fact six months late from the promised delivery date, indicating some difficulty in achieving the required 75Ω characteristics.

Since packages with controlled impedance signal lines are not available with sufficient signal line count, the second option is to keep the length of these signal lines to a minimum. The length of these lines should be less then $\frac{\lambda}{4}$ where λ is the signal wavelength. An estimate of the signal wavelength can be obtained from the signal rise time (see Figure D-2). The equivalent frequency is approximately 1.3 GHz and this leads to a signal wavelength of approximately 7.5 cm; thus $\frac{\lambda}{4} \approx 1.9$ cm. Therefore, the second choice in selecting packages for this application is to choose those packages with signal line lengths less than 1.9 cm.

The viability of this second option is demonstrated by the experience with the MSI packages listed at the bottom of Table D-1. These packages do not have controlled impedance signal lines, yet they have been shown to be useful up to frequencies of 2 GHz. The reason for this is the packages are very small, and the length of the signal lines is very small compared to the signal wavelength.

There are two types of packages that have pin counts that cover the high end of the required range, the pin grid arrays (PGA's) and the fine pitch leaded chip carriers or flatpacks. The PGA's are through hole mount packages and as noted earlier are not used for high frequency applications because of the severe impedance discontinuity at the pin/board interface. The other type of package, the leaded flatpack, is the choice for high frequency applications. All of the entries in Table D-1 are leaded flatpacks, whether standard lead pitch, .050", or fine pitch with lead center ≤ .050".

Table D-2 is a list of available production tooled leaded flatpacks with pincounts above the 148 signal lines of the packages listed in Table D-1. Manufacturer's drawings and/or data sheets are presented in the attached figures; the packages listed in table D-2. These packages do not have dedicated ground and power lines so all lines are potentially available for signals. All the lines on these packages satisfy the line length requirement noted above. The converse of the fact that all lines are potential signal lines is the fact that these packages do not have built-in ground and power planes. The lack of these built-in planes will mean significantly increased cross-talk on the signal lines and significantly increased inductive noise on the DC lines. The obvious way to reduce these problems is to intersperse among the signal lines as many as possible ground and power lines. The ideal would be a ground-signal-ground line arrangement. Table D-2 lists the body size, the lead pitch and the cavity size for the flatpack packages. The packages listed are all fine pitch, with lead pitch of .020" or .025". Also listed is the information on the availability of carriers and (low frequency) sockets for the packages. Carriers and sockets are considered **necessary** support elements to the chip packaging operation; **if they do not exist, they will have to be developed.** It is not possible to deliver devices in fine pitch flatpacks without carriers and sockets.

Listed at the bottom of Table D-2 is a 256 I/O flatpack designed by AT&T for the EMSP project.

AT&T has given permission to use this package and its supporting carriers and sockets in the DARPA project. The package has been production tooled and parts are on hand. The supporting carriers and sockets have been developed and will be available starting in May, 1988.

In addition to the availability of the support elements the EMSP has two electrical advantages. The first is that the package does have a built-in ground plane and although it is not ideally located, this ground plane still offers significant reduction in signal cross-talk. The second is that with the highest available I/O count the package offers the best opportunity of distributing DC lines among the signals.

THE FOLLOWING SECTION DESCRIBES HOW THE RESULT OF THE INDUSTRY SURVEY AND THE ANALYSIS OF THE HIGH SPEED REQUIREMENTS DETAILED HERE WERE USED TO SELECT PACKAGES FOR THE CONTRACT.

RECOMMENDATIONS

The 24 signal, 44 total I/O package from TriQuint was selected for use with the PT-1 chips. This is a true high frequency package, designed with 50Ω signal lines and provision for mounting bypass capacitors on the package. It is recommended that this package be used for the final 4K SRAM. The package is ceramic can be hermetically sealed. A photograph of this package is shown in Figure D-14. The body of the package is .650" sq. with leads on .050" pitch. Carriers are not necessary for packages with this pitch. Low frequency sockets are available for this package. A high frequency test fixture is also commercially available to fit this package. Some preliminary tests have shown that this test fixture performs well to frequencies beyond 1GHz, certainly sufficient for the present application.

Another important feature of this package is that it is designed to accommodate high power chips. The die attach substrate is a copper/tungsten composite that is coexpansive with the ceramic body but has a thermal conductivity an order of magnitude higher than ceramic. This high conductivity die mount is not the total solution to the thermal management problem for a high power chip but it is an important contribution to the solution.

The 64 signal, 88 total I/O package from Interamics was selected for use with the PT-2 logic chips. Again, this is a true high frequency package with 50Ω signal lines, some built in bypass capacitance and the high thermal conductivity die attach substrate. This package is recommended for use with any of the logic chip deliverables. A photograph of this package is shown in Figure D-15. This package is also ceramic with provision for a hermetic seal. The package body is .500" sq. with 23 leads per side, at .020" pitch. (The two leads that surround each of the four corners are tied together, hence the designation 88 rather than 92 total I/O.) This is a fine pitch package, but the carriers and sockets are not available, neither are high speed test fixtures. These support elements will have to be developed.

The 256 I/O fine pitch leaded flatpack designed by AT&T for the EMSP project appears to be the best available package for the high pin count logic devices. A photograph of this package is shown in Figure D-16. This package is not ideal but it does have several advantages, namely a built-in ground plane, spare I/O for signal isolation, and available carriers and sockets. The principal drawback to this package is that the die cavity (.560"sq.) is too large for the expected size of the Casino Test Chip, .320"sq. This same problem exists to a greater or lesser extent for all of the high pin count packages however. The high frequency test fixtures for this package will have to be developed, but this same development would be required for any of the high pin count packages. The 256 I/O package does not have a high thermal conductivity die attach substrate, but again neither do any of the other high pin count packages. This adds an important resistance in the heat flow path but it doesn't preclude a solution to the thermal management problem.

A request for approval to use the 256 I/O EMSP will be submitted to the COTR.

TABLE D-1

Packages with Controlled Impedance ($Z_o = 50\Omega$) Signal Lines

VENDOR	I/O COUNT (SIGNAL/TOTAL)	PACKAGE BODY MATERIAL	CAVITY SIZE (in)	COMMENTS
INTERAMICS	28/32	ALUMINA	.190X.250	
	64/88	"	.250X.250	MAYO DESIGN
TRIQUINT	8/20	ALUMINA	.060X.060 (CHIP)	NO CAVITY, PERFORMANCE VERIFIED TO 18GHz
	24/44	"	.130X.130	PROVISION FOR MOUNTING BYPASS CAPACITORS.
	64/132	"	.210x.210	PROVISION FOR MOUNTING BYPASS CAPACITORS.
ROGERS - MICROTEC	64/88	POLYMIDE	.250X.250	MAYO DESIGN
	116/132	"	.400X.400	PROVISION FOR MOUNTING BYPASS CAPACITORS.
	148/164	"	.400X.400	PROVISION FOR MOUNTING BYPASS CAPACITORS.
Additional Packages Usable in High Frequency Applications				
MSI	20/20	ALUMINA	.140X.140	PACKAGE BODY .270"SQ.
	32/32	"	.265X.265	" " "
	64/64	"	.360X.360	PACKAGE BODY .640"SQ.
	84/84	"	.300X.300	" " "

TABLE D-2

High I/O Count Leaded Flatpacks

I/O #	Manufacturer	I/O Pitch in.	Body Size in. (SQ)	Cavity Size in.	Carrier/Burn-In Socket	Comments
152	NTK	.020	.840	.380x.380	YES	Open Tooled, No Ground or Power Planes
172	NTK	.020	.940	.380x.380	YES	
172	KYOCERA	.025	1.150	.380x.380	NO	
196	KYOCERA	.025	1.350	.410x.410	NO	
256	NTK	.020	1.380	.540x.550	YES	
256	KYOCERA	.020	1.480	.500x.500	NO	
256	NTK	.020	1.450	.560X.560	YES	AT&T design, Ground and Power Planes

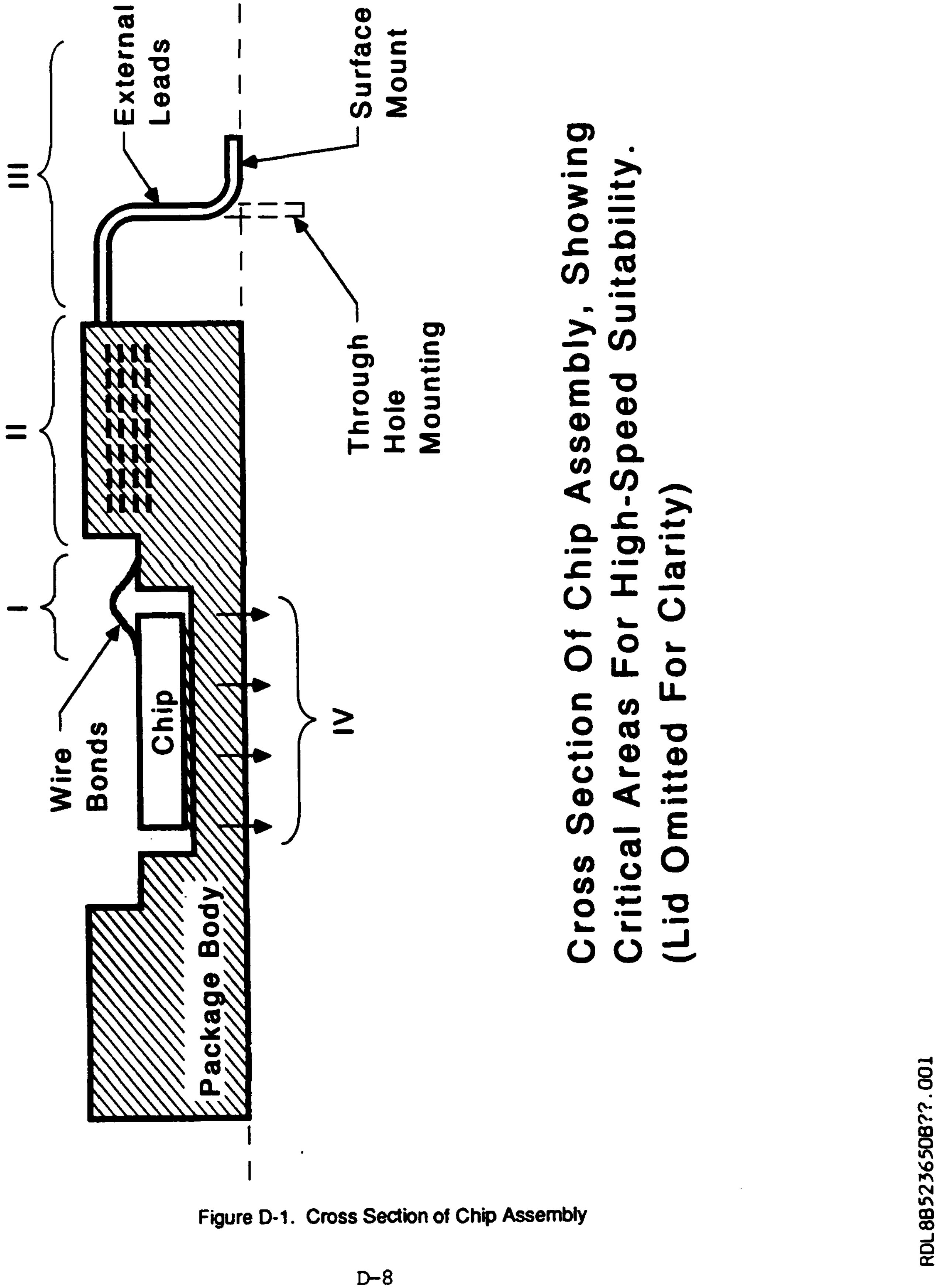
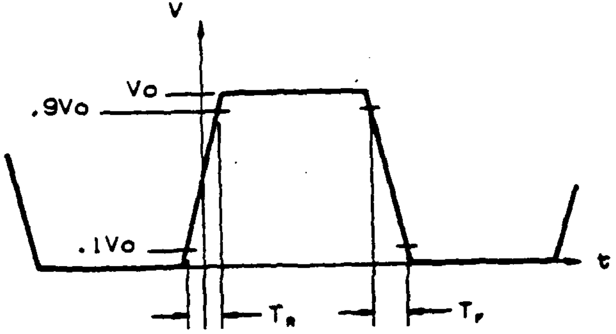

Cross Section Of Chip Assembly, Showing
Critical Areas For High-Speed Suitability.
(Lid Omitted For Clarity)
External Leads
Surface Mount
Through Hole Mounting
Wire Bonds
Chip
Package Body
I
II
III
IV
RDL8B523650B??.001

Figure D-1. Cross Section of Chip Assembly

To obtain a signal frequency from a signal with a known signal rise time T_r and signal fall time T_f, one compares the signal



to a sine wave with the same amplitude and the unknown frequency f,

$$V(t) = \frac{Vo}{2} [1 + \sin 2 \Pi ft]$$

For simplicity assume $T_r = T_f$, then equating the sine wave value to the signal value at $t=T_r/2$ yields

$$.9Vo = \frac{Vo}{2} [1 + \sin \Pi \, fT_r]$$

which has the solution

$$f = \frac{\sin^{-1}(.80)}{\Pi \, T_r} = \frac{.295}{T_r}$$

For a signal with a rise time $T_r = 225$ ps, the frequency is

f=1.3 GHZ

Then, from the wavelength/frequency relationship

$$\lambda f = \frac{C}{\sqrt{E_r}}$$

where λ is the wavelength, C is the speed of light and E_r is the relative dielectric constant for the package body material. For a ceramic package $E_r = 9.6$, then

$$\lambda = 7.4cm$$

Figure D-2. The Calculation of the Signal Frequency and Wavelength

The calculation of the signal frequency and wavelength from the signal rise time

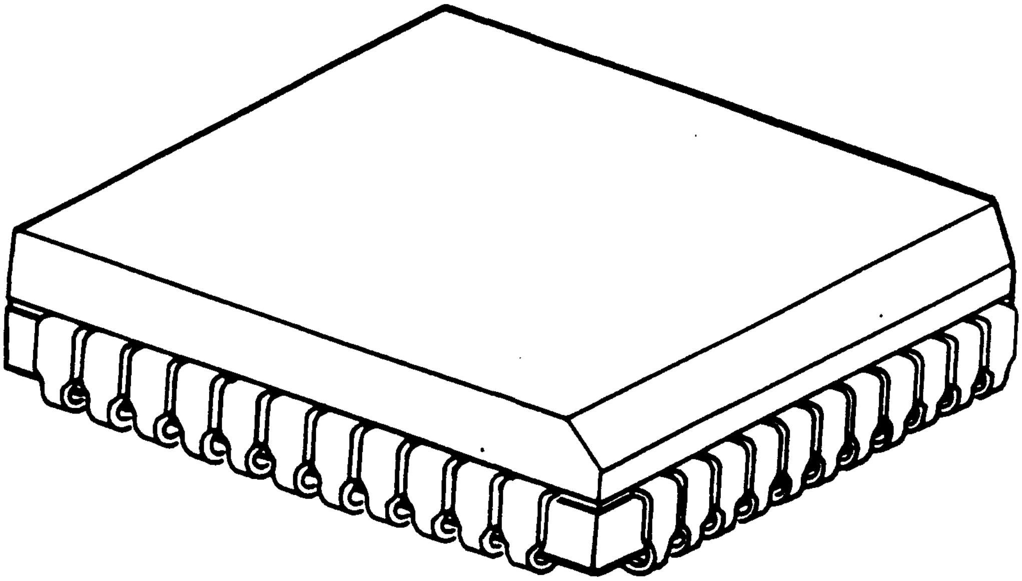


Figure D-3. Post Molded Plastic Chip Carrier

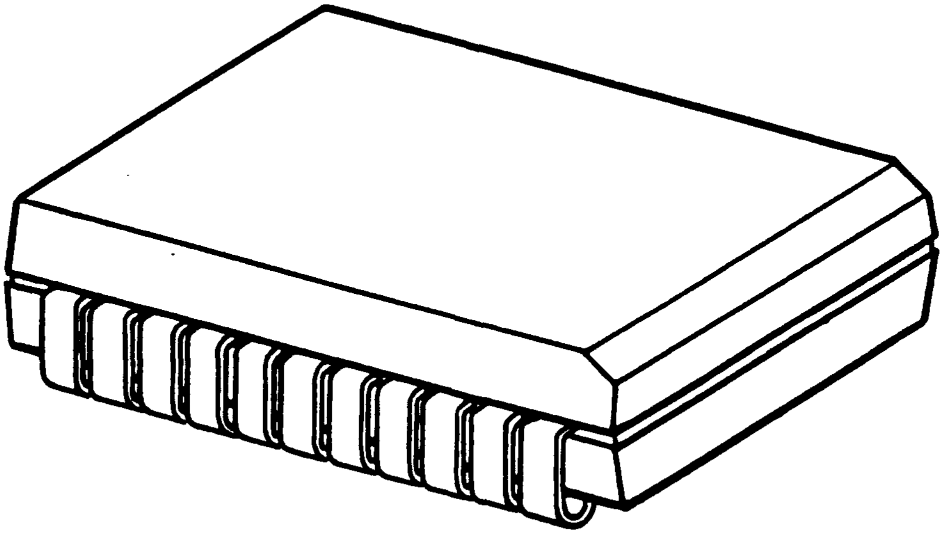


Figure D-4. SOJ (Small Outline J Lead)

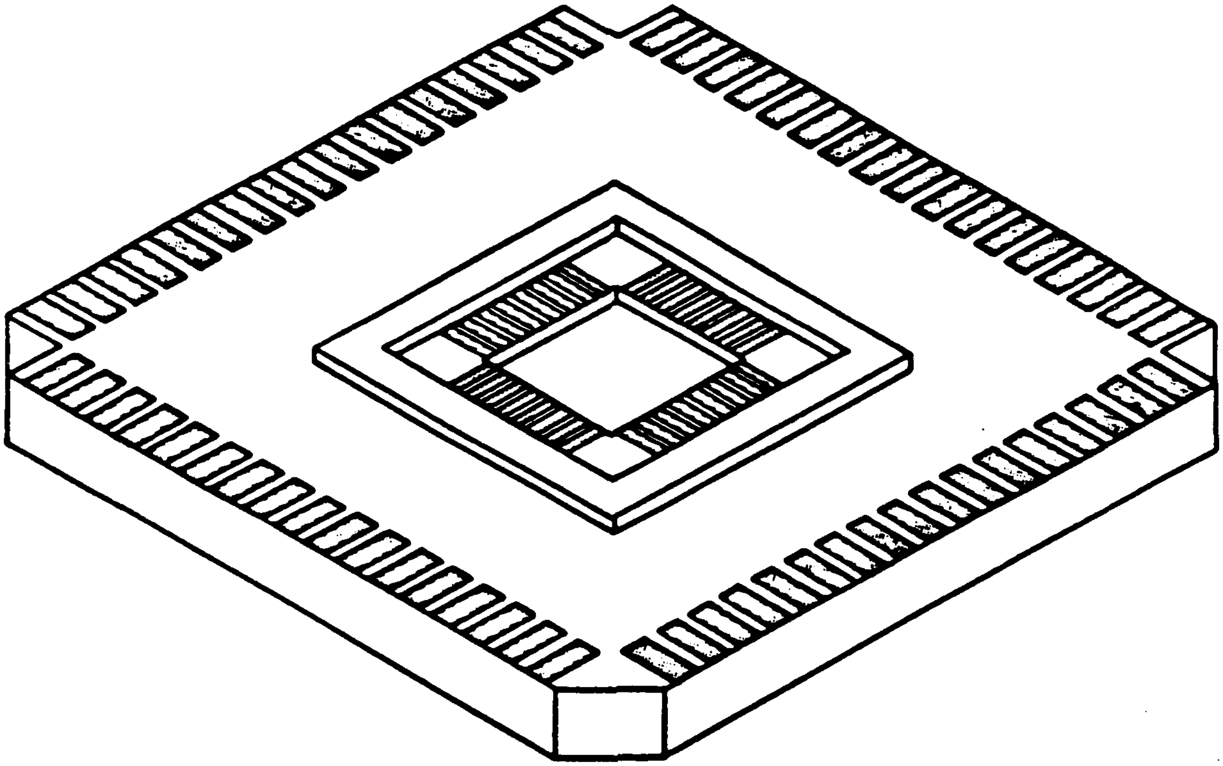


Figure D-5. Leadless Ceramic Chip Carrier

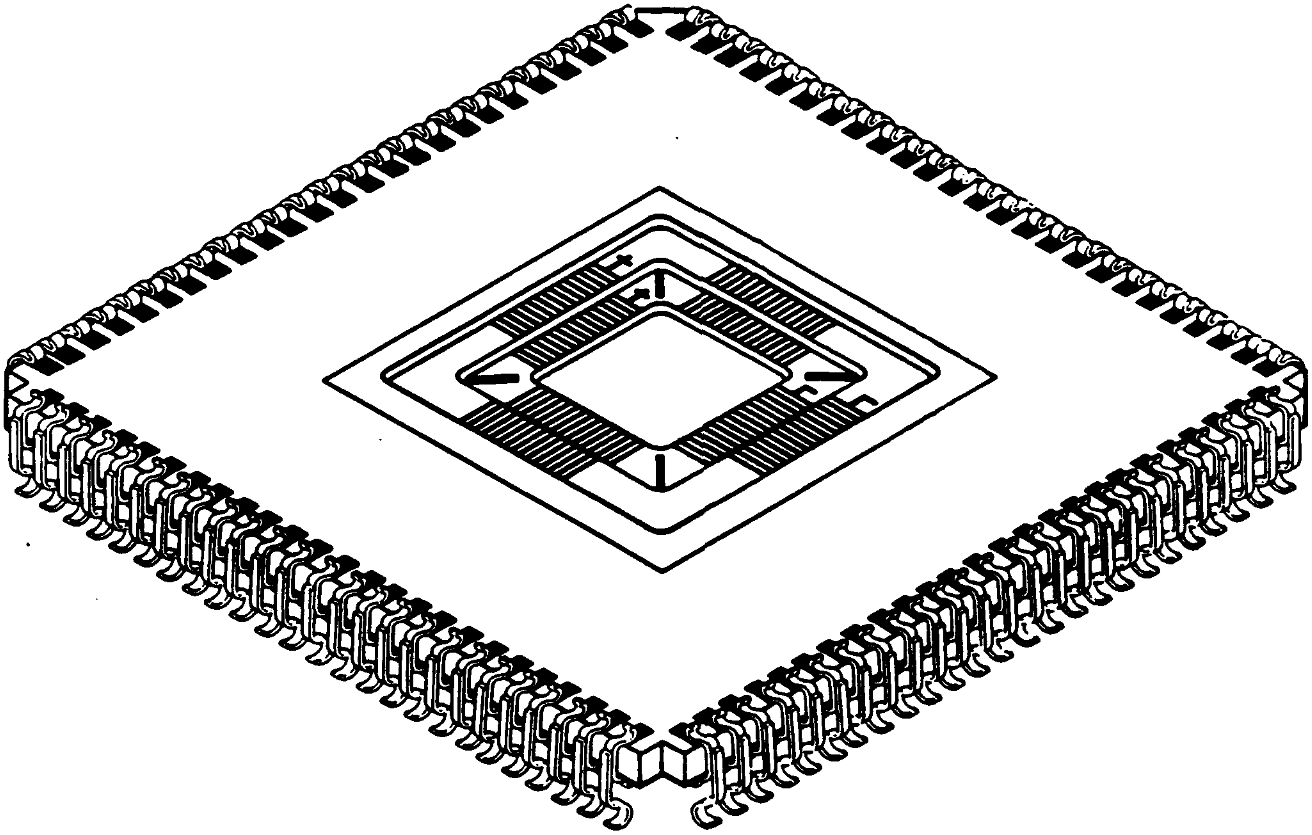


Figure D-6. Leaded Ceramic Chip Carrier

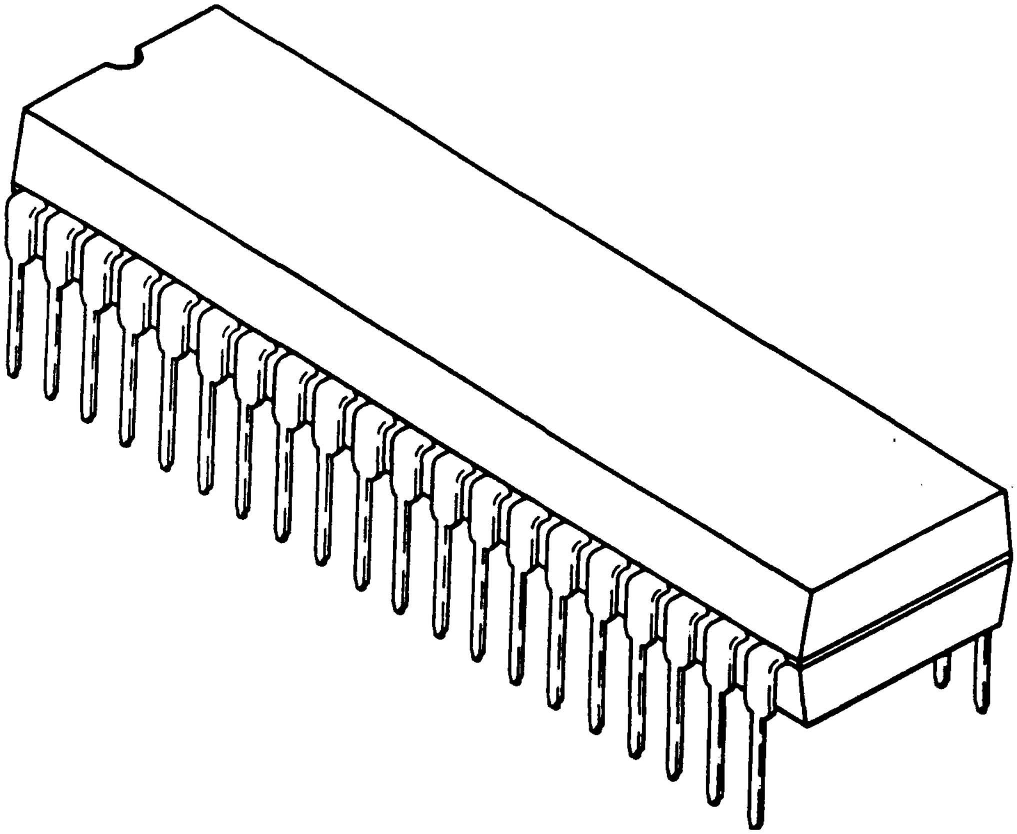


Figure D-7. Post Molded Plastic Dip

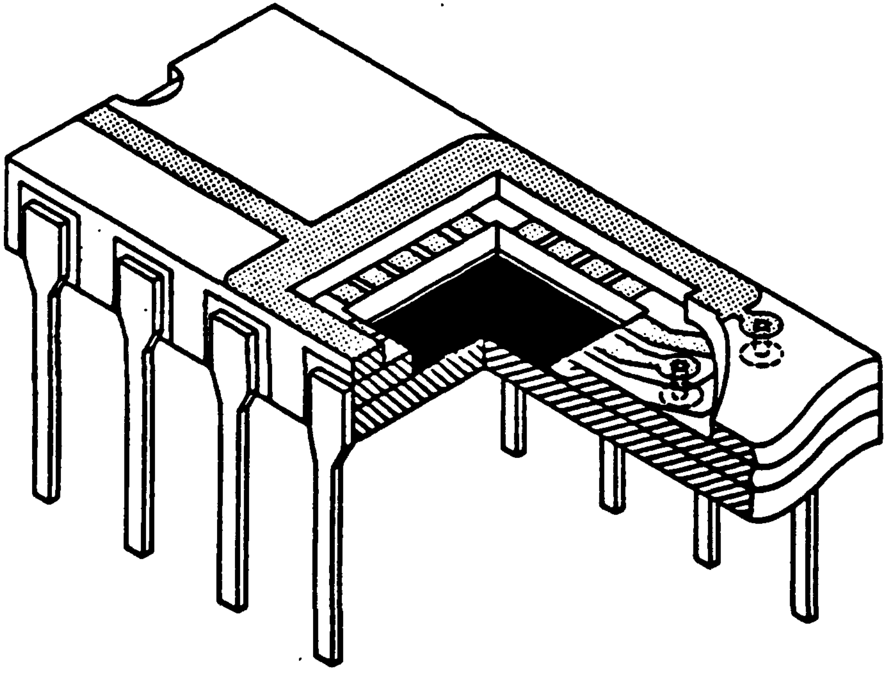


Figure D-8. Ceramic Dip

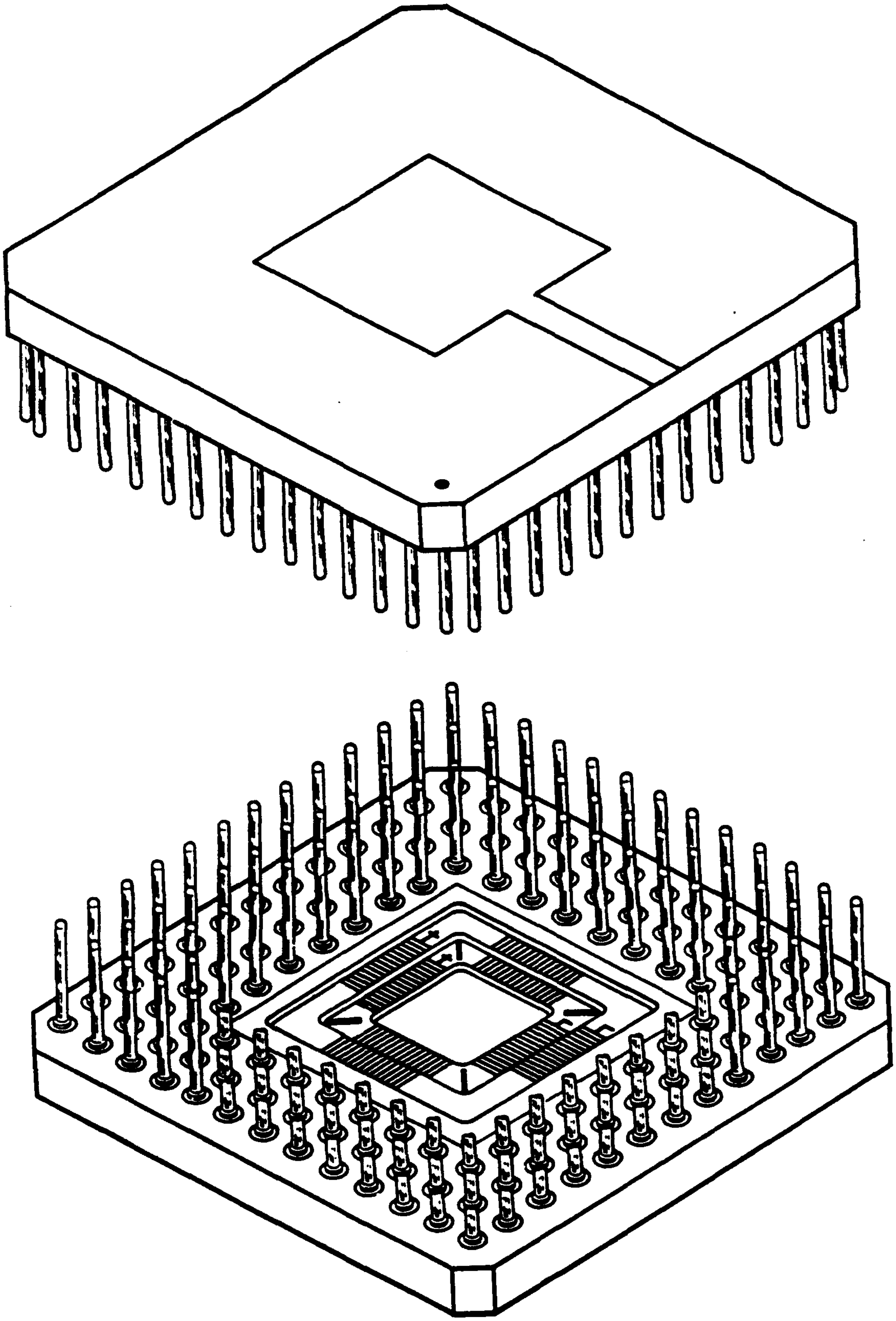


Figure D-9. Ceramic Pin Grid Array

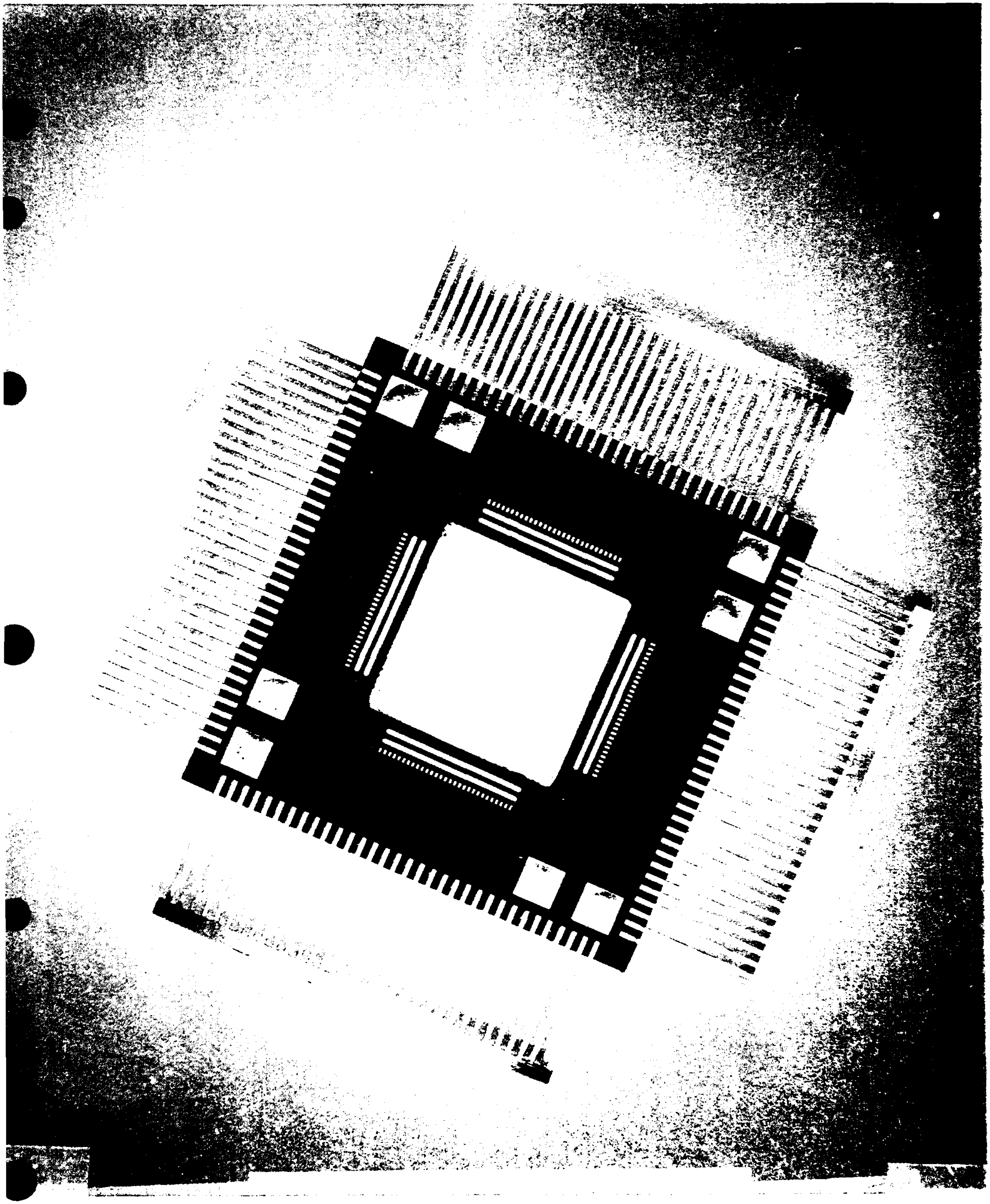
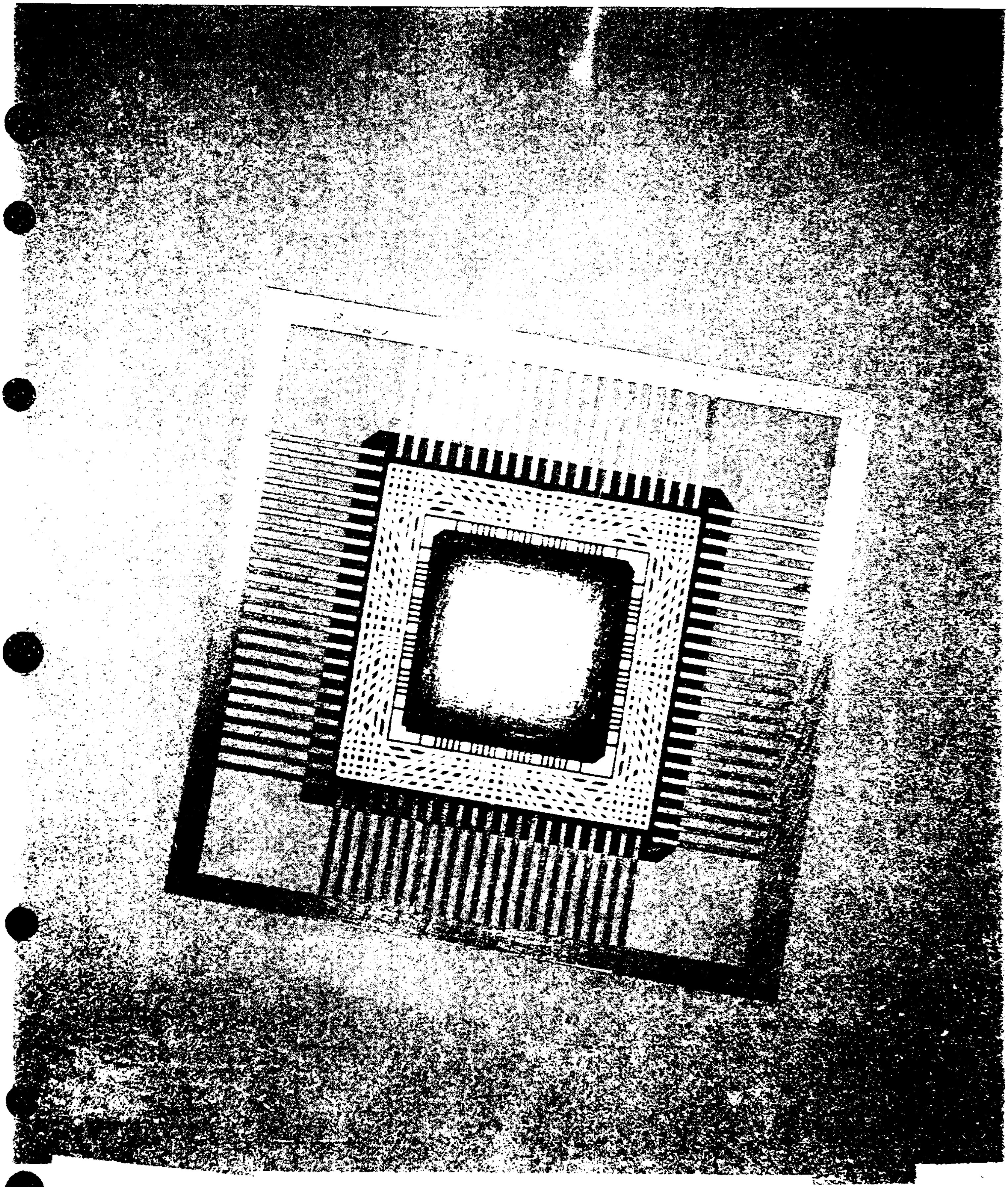
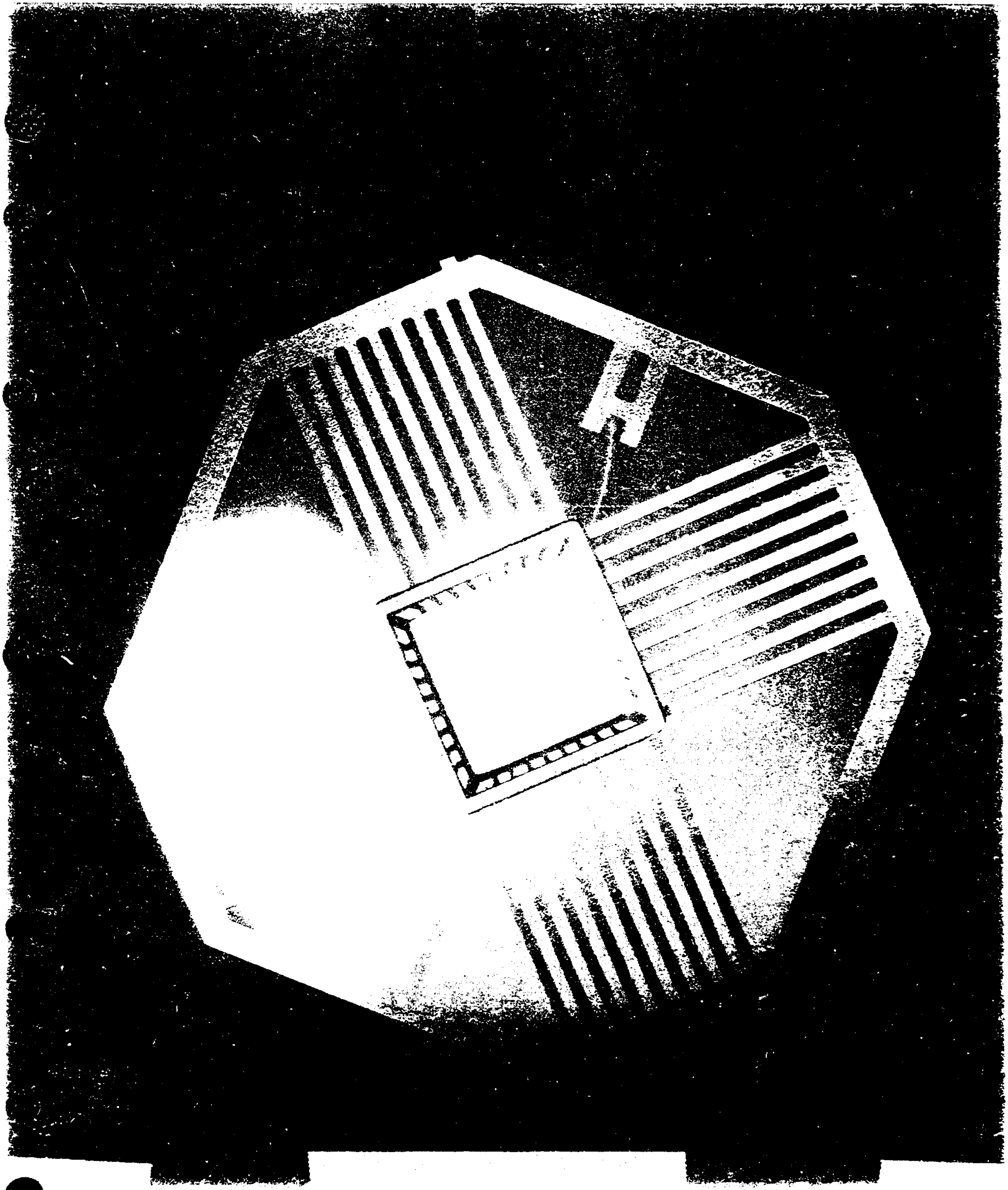


Figure D-10. 132 I/O Flatpack





HIGH-SPEED PACKAGE SELECTION PROCESS

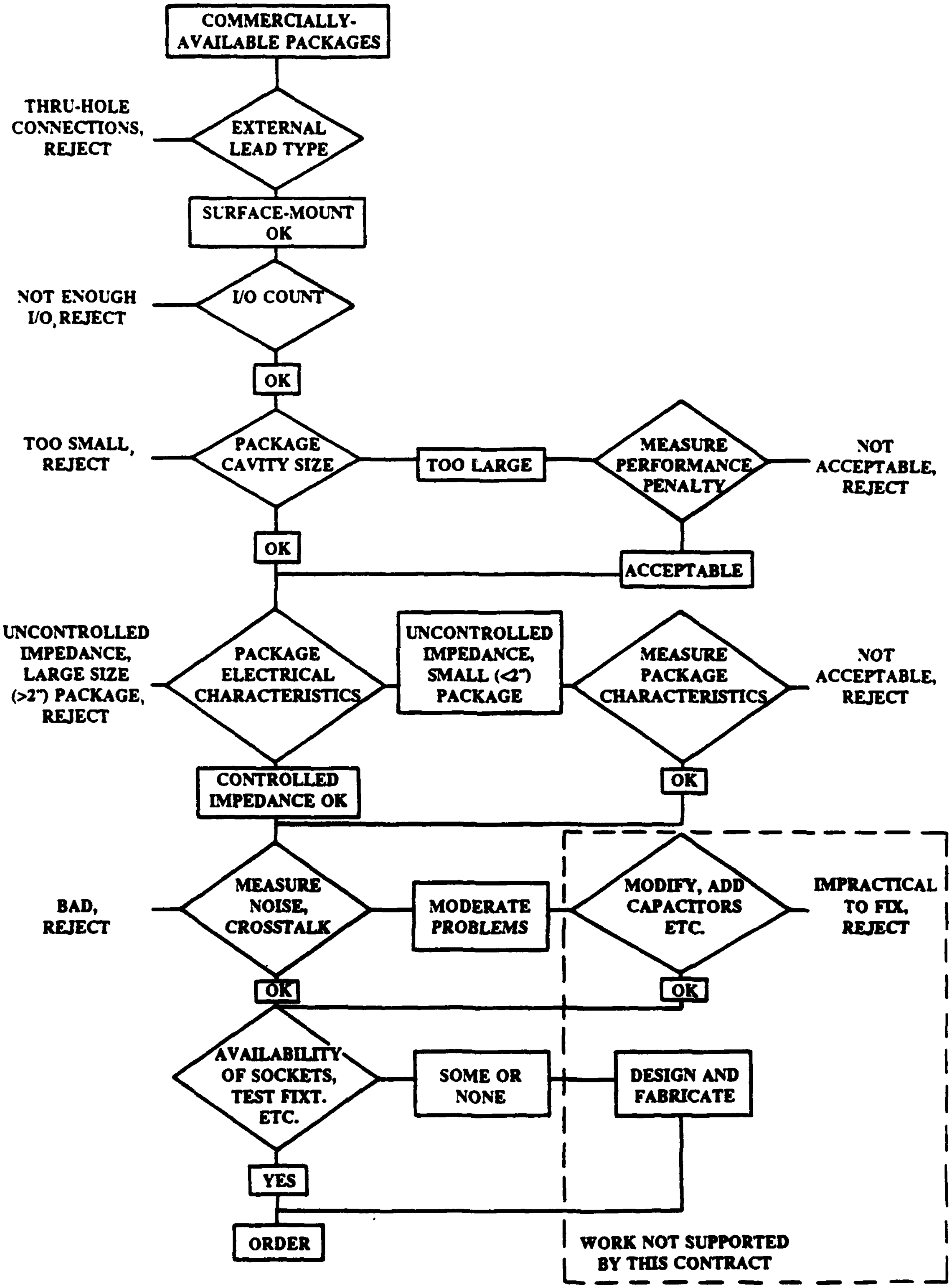

COMMERCIALLY-AVAILABLE PACKAGES
THRU-HOLE CONNECTIONS, REJECT
EXTERNAL LEAD TYPE
SURFACE-MOUNT OK
NOT ENOUGH I/O, REJECT
I/O COUNT
OK
TOO SMALL, REJECT
PACKAGE CAVITY SIZE
TOO LARGE
MEASURE PERFORMANCE PENALTY
NOT ACCEPTABLE, REJECT
OK
ACCEPTABLE
UNCONTROLLED IMPEDANCE, LARGE SIZE (>2") PACKAGE, REJECT
PACKAGE ELECTRICAL CHARACTERISTICS
UNCONTROLLED IMPEDANCE, SMALL (<2") PACKAGE
MEASURE PACKAGE CHARACTERISTICS
NOT ACCEPTABLE, REJECT
CONTROLLED IMPEDANCE OK
OK
BAD, REJECT
MEASURE NOISE, CROSSTALK
MODERATE PROBLEMS
MODIFY, ADD CAPACITORS ETC.
IMPRACTICAL TO FIX, REJECT
OK
OK
AVAILABILITY OF SOCKETS, TEST FIXT. ETC.
SOME OR NONE
DESIGN AND FABRICATE
YES
ORDER
WORK NOT SUPPORTED BY THIS CONTRACT

Figure D-13. High Speed Package Selection Process

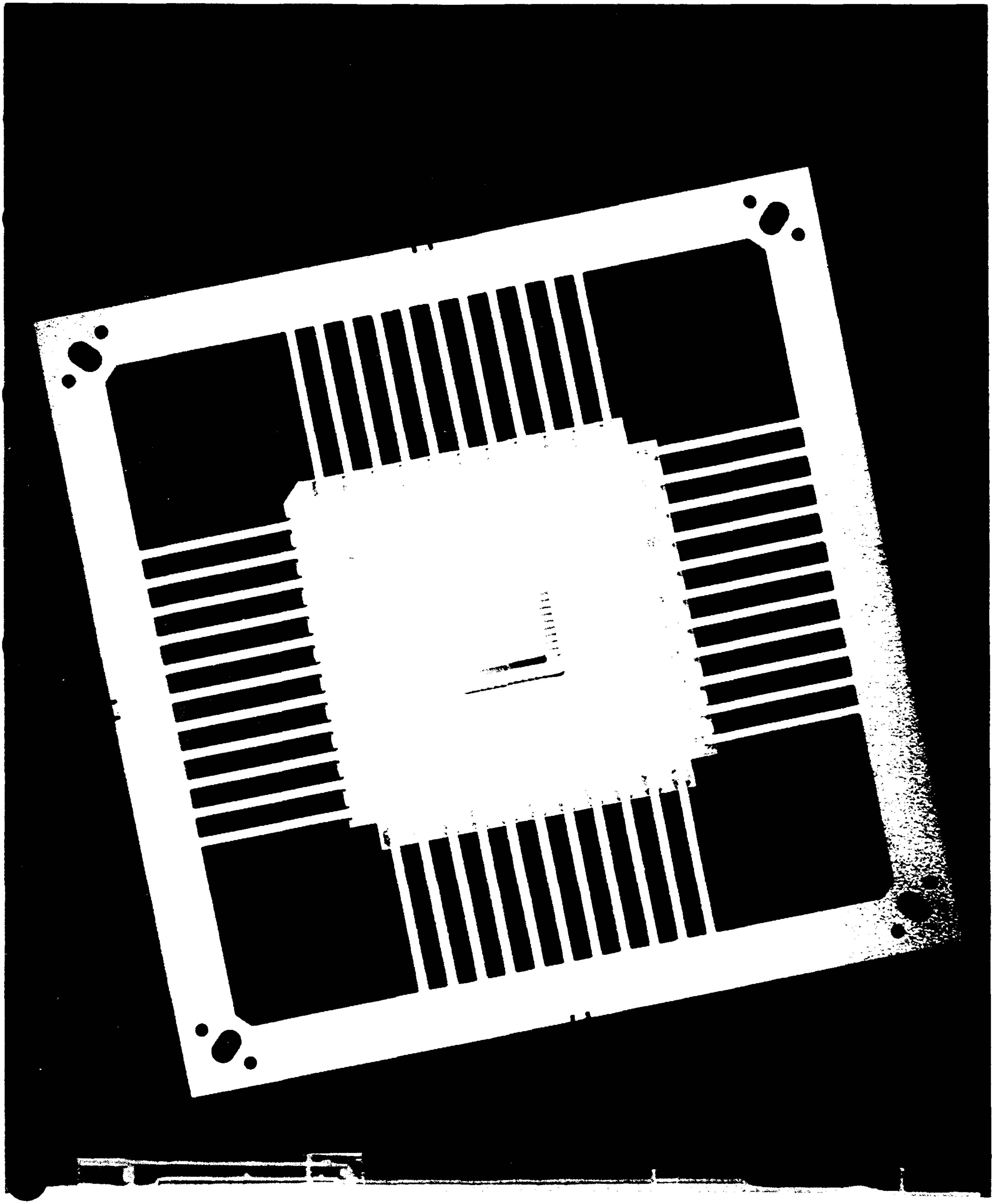
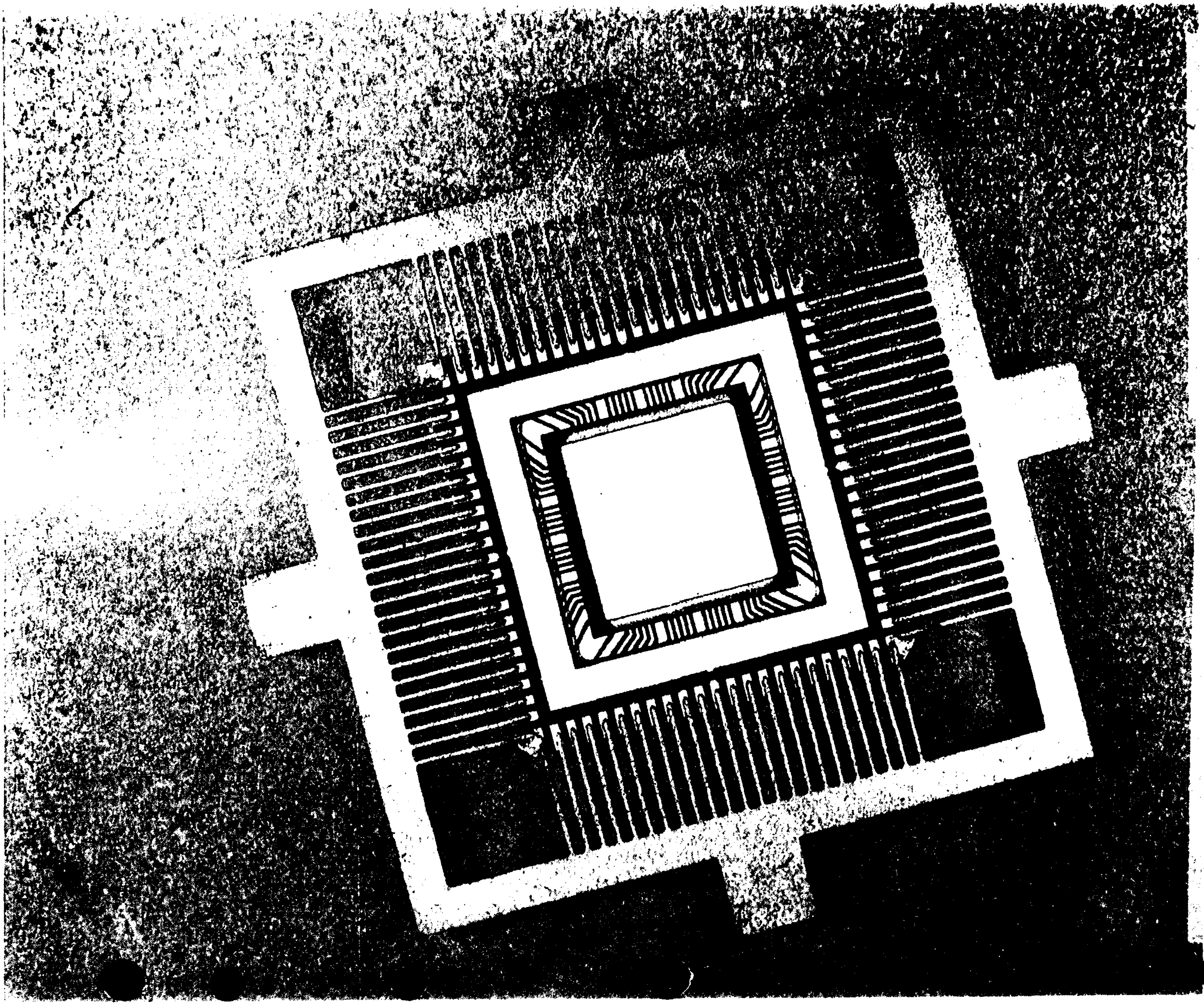
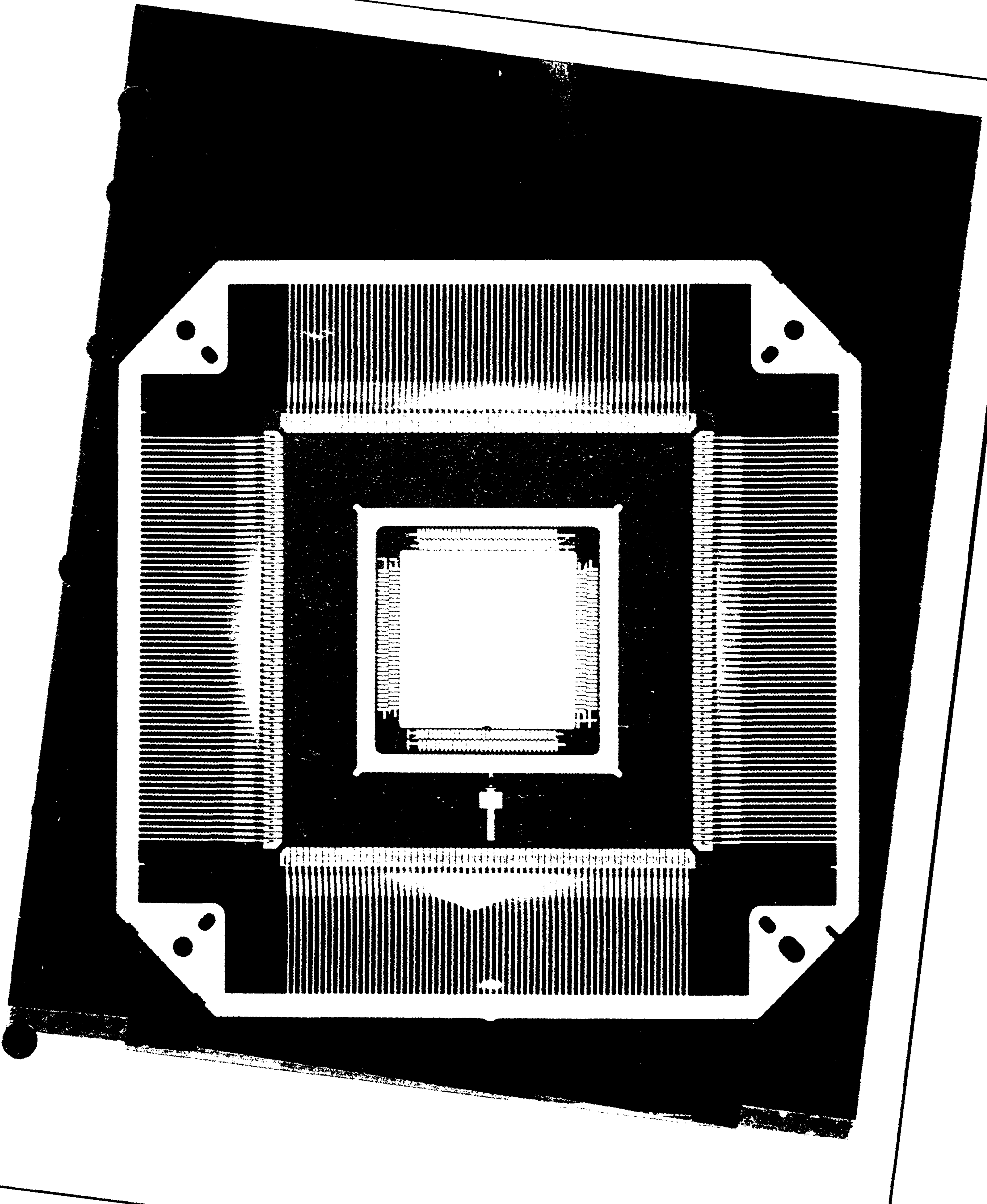


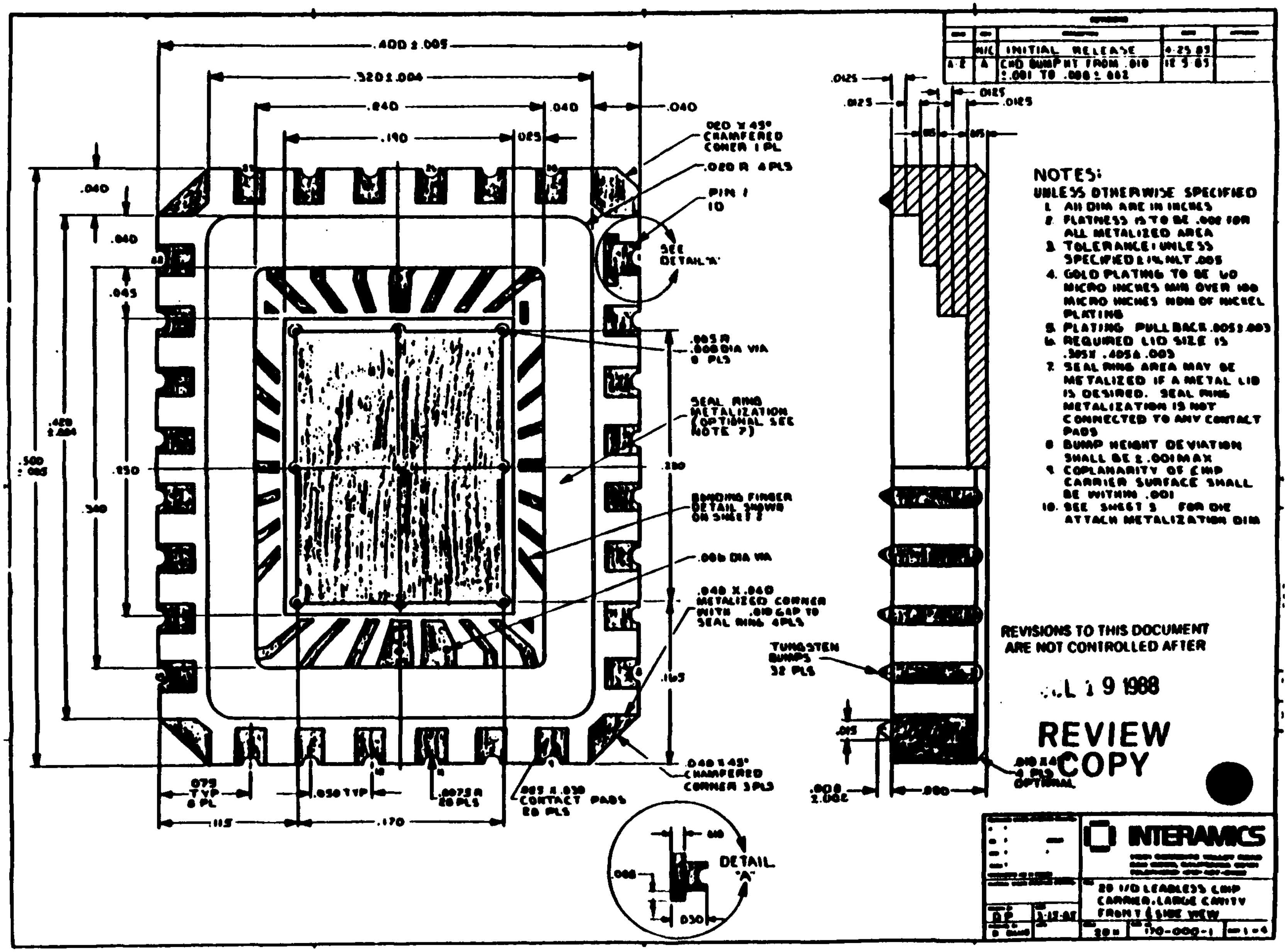
Figure D-14. 44 I/O TriQuint Package





Drawings for Packages

Described in Table D-1


.400 ±.005
.320±.004
.240
.040
.040
.190
.025
.040
.040
.045
.420 ±.004
.500 ±.005
.150
.340
.020 X 45° CHAMFERED CONER 1 PL
.020 R 4 PLS
PIN 1 ID
SEE DETAIL 'A'
.005 R .0080 DIA VIA 8 PLS
SEAL RING METALIZATION (OPTIONAL SEE NOTE 7)
.230
BONDING FINGER DETAIL SHOWN ON SHEET 2
.006 DIA VIA
.040 X .040 METALIZED CORNER WITH .010 GAP TO SEAL RING 4 PLS
.165
.040 X 45° CHAMFERED CORNER 3 PLS
.075 TYP 8 PL
.050 TYP
.0075 R 28 PLS
.025 X .030 CONTACT PADS 28 PLS
.115
.170
.0125
.0125
.0125
.0125
.005
.005
TUNGSTEN BUMPS 32 PLS
.015
.008 ±.002
.080
.010 X 45° 4 PLS OPTIONAL
DETAIL 'A'
.010
.008
.030
N/C
INITIAL RELEASE
4-25-83
A-2
A
CHD BUMP HT FROM .010 ±.001 TO .008±.002
12-5-83
INTERAMICS
28 I/O LEADLESS CHIP CARRIER, LARGE CAVITY FRONT & SIDE VIEW
D P
3-12-83
170-000-1

NOTES:

UNLESS OTHERWISE SPECIFIED

1. ALL DIM ARE IN INCHES
2. FLATNESS IS TO BE .002 FOR ALL METALIZED AREA
3. TOLERANCE: UNLESS SPECIFIED ±1% NLT .005
4. GOLD PLATING TO BE 60 MICRO INCHES MIN OVER 100 MICRO INCHES NOM OF NICKEL PLATING
5. PLATING PULLBACK .005±.003
6. REQUIRED LID SIZE IS .305 X .405 ± .003
7. SEAL RING AREA MAY BE METALIZED IF A METAL LID IS DESIRED. SEAL RING METALIZATION IS NOT CONNECTED TO ANY CONTACT PADS
8. BUMP HEIGHT DEVIATION SHALL BE ±.001 MAX
9. COPLANARITY OF CHIP CARRIER SURFACE SHALL BE WITHIN .001
10. SEE SHEET 3 FOR DIE ATTACH METALIZATION DIM

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REVIEW COPY

Figure D-17. Interamics 28/32 Leadless Package

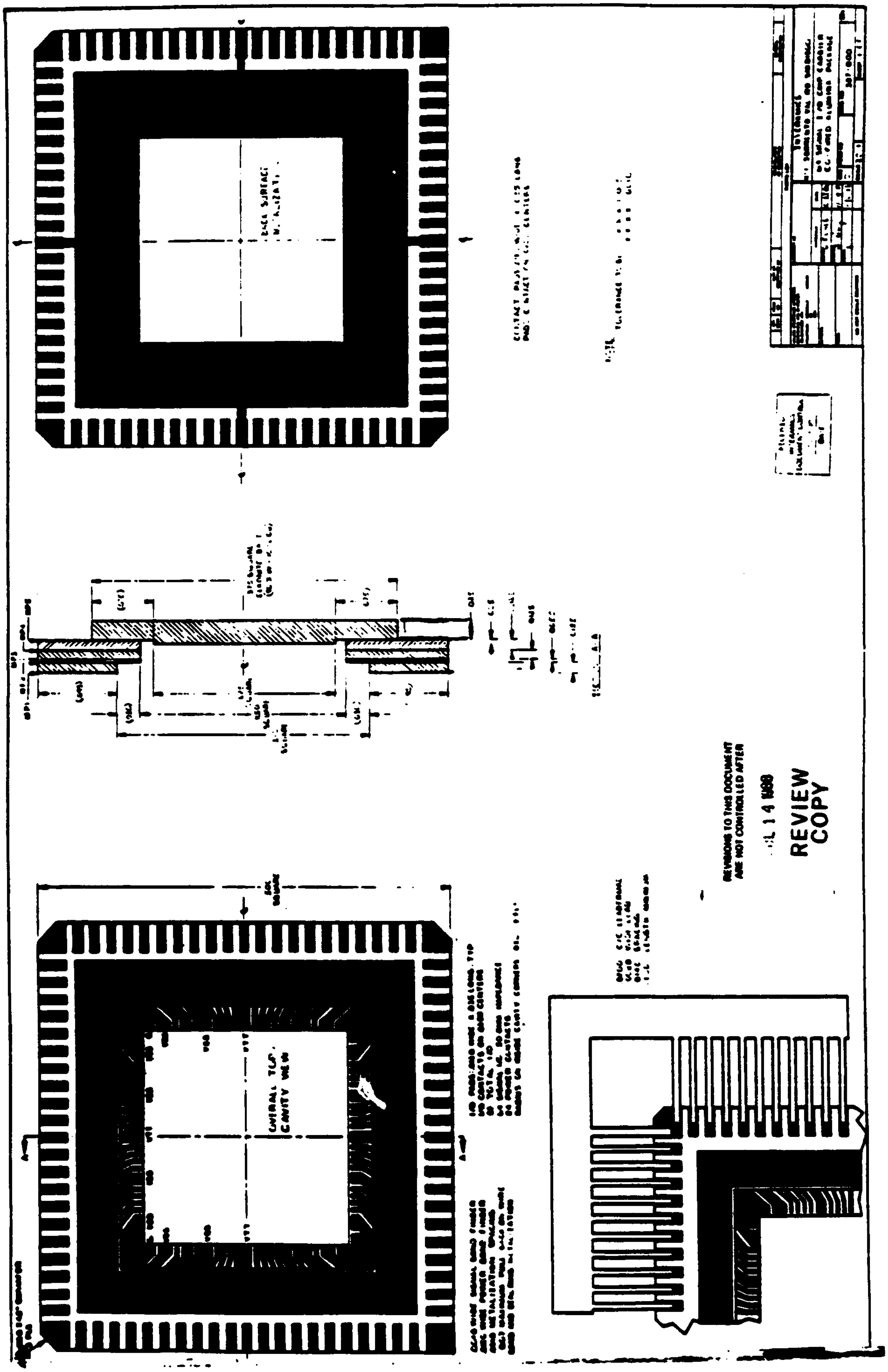
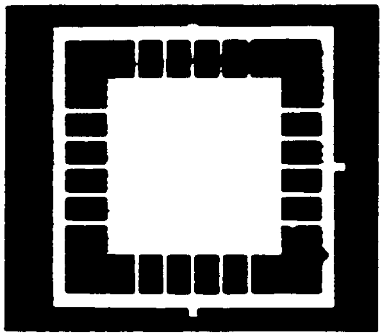

OVERALL TOP CAVITY VIEW
BACK SURFACE METALIZATION
REVISIONS TO THIS DOCUMENT ARE NOT CONTROLLED AFTER
REVIEW COPY

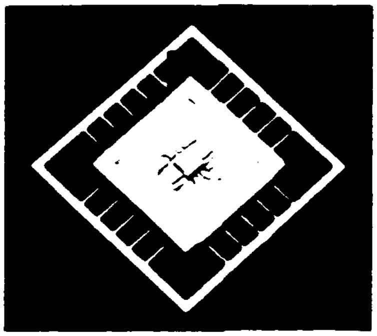
Figure D-18. Interamics 64/88 Leaded Package

TEK TPAX SERIES DATA SHEET Listed as TriQuint 8/20 SPECIFICATIONS ORDERING INFORMATION

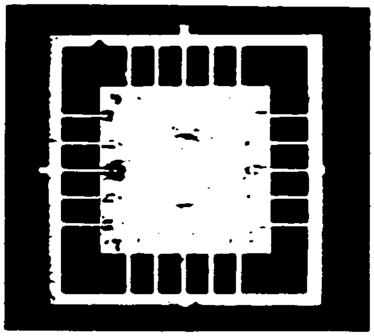
TEKPAC:™ HERMETIC MMIC PACKAGE PRODUCT LINE



TPAX142 (top view)



Typical Application used in Micro-S product line, TriQuint Semiconductor, Inc



TPAX142 (bottom view)

TEKPAC™ Hermetic MMIC Packages

- Multiple RF signal lines from motherboard to chip
- $10^{-8\ \text{atm-cc sec}}$ hermeticity
- Direct-contact heatsinking

The TPAX Series MMIC package represents a new benchmark for low cost surface-mountable and hermetically sealable microelectronic packages designed for Monolithic Microwave Integrated Circuits (MMICs)

The TPAX Series is a first in a series of low-cost, 12 GHz performance MMIC packages. Thick film technology and well established fabrication techniques provide a cost-effective solution without sacrificing performance

TPAX142 CHARACTERISTICS

	0–6 GHz	6–12 GHz
VSWR[1]	1 2 1 max	2 0 1 max
Insertion loss[1]	5 dB max	1 dB max
Isolation[2]	40 dB min	30 dB min

[1] Measured for one signal line from leadframe to die attach pad.

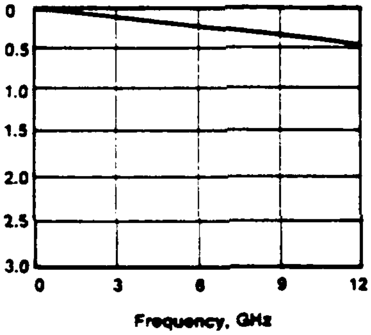
[2] Measured for two opposite signal lines with all unconnected lines grounded.

Environmentally tested per MIL-STD-883.

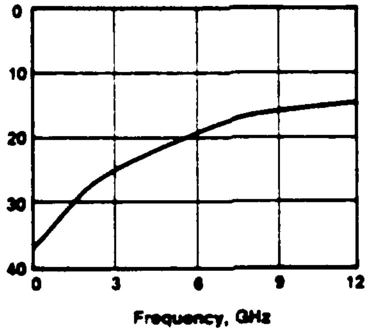
OTHER SERVICES AVAILABLE

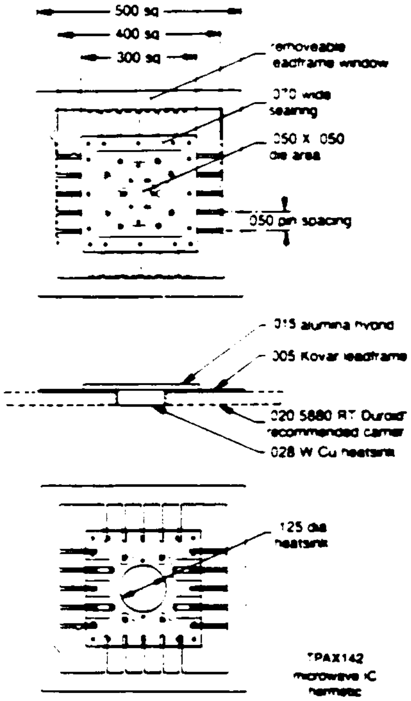
- Product technology licensing
- Custom design/applications

INSERTION LOSS dB (TYPICAL)



RETURN LOSS dB (TYPICAL)




500 sq
400 sq
300 sq
removeable leadframe window
070 wide sealring
050 X 050 die area
050 pin spacing
015 alumina hybrid
005 Kovar leadframe
020 5880 RT Duroid* recommended carrier
028 W Cu heatsink
125 dia heatsink

TPAX142 microwave IC hermetic surface-mount package

*RT Duroid is a registered trademark of the Rogers Corp.

ORDERING INFORMATION

Tektronix Product	Frequency Performance	Case Size (inches)	Motherboard Recommended	Diepad Area (inches)	TEKPAC Options
TPAX142	12 GHz	3 x 3	020 5880 RT Duroid	054 x 054	Option 01—Lid perform set Option 05—Leadframe window removed

TKIT14F — Evaluation kit for the TPAX142

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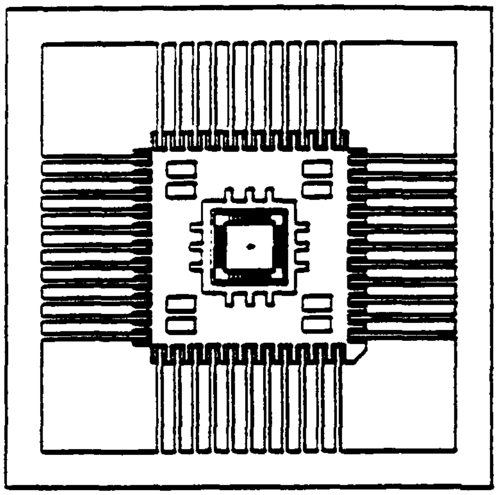
Figure D-19. TriQuint 8/20 Leaded Package

PRODUCT DATA | *PK-MLC44E / PK-MLC44S*

44 LEAD HIGH SPEED CERAMIC PACKAGE



FEATURES:

- *24 High-Speed 50-Ohm Controlled Impedance Signal Lines*
- *Power Supply Decoupling via Power Planes and Optional On-Package Capacitors*
- *Multiple Power and Ground Connections*
- *Optional Metalized Seal Ring for Hermetic Sealing*

DESCRIPTION

The MLC44 package is a high-speed multilayer ceramic package developed at TriQuint to support the special requirements of very high performance ICs. The package is designed to handle clock rates up to 4GHz and fast edge speeds less than 100ps. Signals are carried on 50-Ohm controlled impedance transmission lines from the package leads to the bond pads. Excellent signal isolation is provided by the use of multiple ground lines. Capacitive power planes and decoupling capacitors minimize switching noise on the power supplies.

The package is fabricated from cofired alumina ceramic. In most applications it easily handles power dissipation of 1 Watt, and can handle 3-4 Watts with the addition of a suitable heat sink. The package is suited for surface mounting with appropriate lead bend. The package body is available with a solder seal ring around the cavity, or without for epoxy sealing.

April 21, 1988 14-0083-A

TriQuint SEMICONDUCTOR

Figure D-20. TriQuint 24/44 Leaded Package; Description

SIGNAL CONNECTIONS

The illustrations below identify package pin and die cavity bond pad connections.

Each signal bond pad connects to one package pin through a 50-Ohm controlled impedance line. All the ground bonding pads are connected together, as are all the pins labeled GND. All points labeled GND are common with all the internal ground planes and the back surface of the package. Each of the two power supplies has two pins, at opposite corners of the package which are common with two corresponding bond pads at opposite corners of the bond cavity. Both power supplies and ground are brought to pads beside the bond cavity where optional decoupling capacitors may be added.

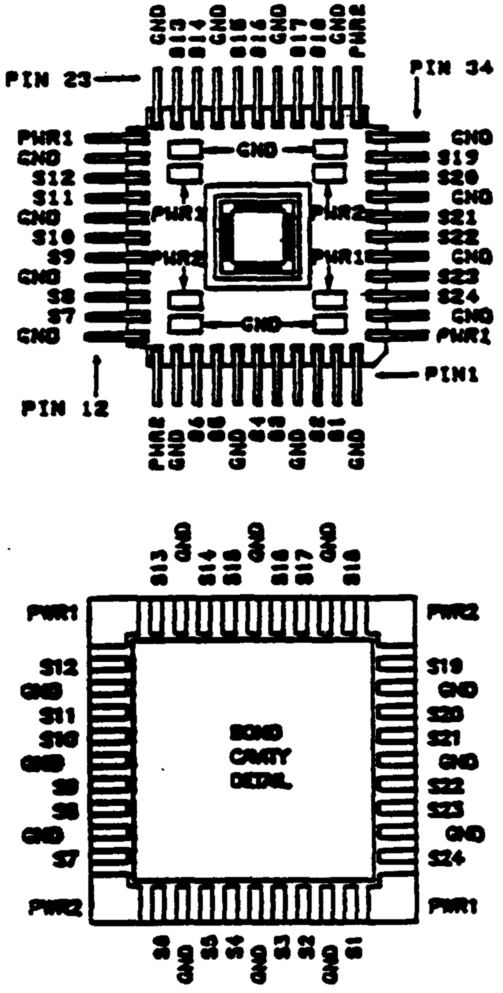
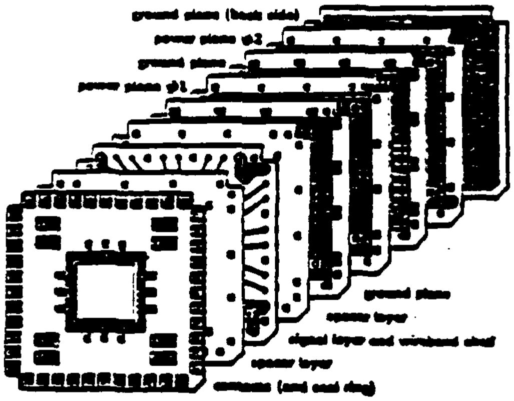

GND
S13
S14
GND
S15
S16
GND
S17
S18
GND
PWR2
PIN 23
PIN 34
PWR1
GND
S12
S11
GND
S10
S9
GND
S8
S7
GND
GND
S19
S20
GND
S21
S22
GND
S23
S24
GND
PWR1
PWR1
PWR2
PWR2
PWR1
GND
GND
PIN1
PIN 12
PWR2
GND
S6
S5
GND
S4
S3
GND
S2
S1
GND
S13
GND
S14
S15
GND
S16
S17
GND
S18
PWR1
PWR2
S12
GND
S11
S10
GND
S9
S8
GND
S7
S19
GND
S20
S21
GND
S22
S23
GND
S24
BOND
CAVITY
DETAIL
PWR2
PWR1
S6
GND
S5
S4
GND
S3
S2
GND
S1

Figure D-21. TriQuint 24/44 Leaded Package; Signal Connections

PACKAGE STRUCTURE

The package is constructed of several metal layers with a layer of ceramic between each pair of metal layers. This structure gives a controlled impedance environment for the signal lines. The figure below shows a representation of the layered structure.


ground plane (back side)
power plane φ2
ground plane
power plane φ1
ground plane
spacer layer
signal layer and wirebond shelf
spacer layer
contacts (and seal ring)

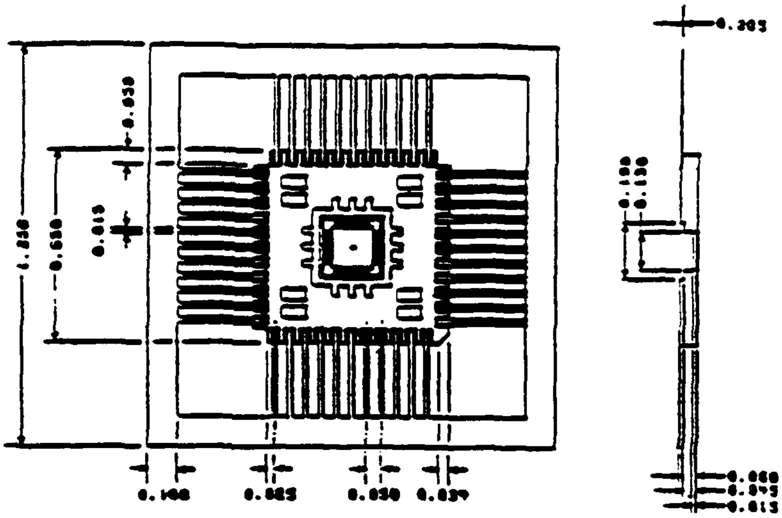
SPECIFICATIONS

Materials:	Body	Alumina Ceramic
	Leads	Kovar
	Metalization	Tungsten/Nickel/Gold
Dimensions:	Body Size	0.650 x 0.650 x 0.060 inches
	Die Cavity Size	0.130 x 0.130 inch
	Max recommended die size	0.090 x 0.090 inch
Leads:	Spacing	0.050 inch
	Lead Count	44
	Signal Leads	24
	Ground Leads	16
	Power Leads	4 (2 per supply)
Misc.	Power plane Capacitance (each supply)	150 pF
	Die-to-Case Thermal Impedance[1]	10°C/Watt

Note 1: The thermal impedance value shown is typical for a [illegible] x [illegible] die. Use thermal impedance numbers with caution: operating temperature is a sensitive function of die size, circuit layout, and other factors.

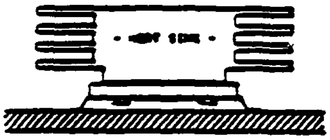
Figure D-22. TriQuint 24/44 Leaded Package; Structure and Specifications

MECHANICAL DIMENSIONS



SUGGESTED MOUNTING

Bending the leads in a gull-wing fashion as shown allows the package to be surface mounted face down. In this way, a heat sink can be mounted on the back of the package, physically close to the die.



PRODUCT DESIGNATIONS

PK-MLC44E	Package body without seal ring, for use with Epoxy seal.
PK-MLC44S	Package body with gold metalized seal ring, for use with AuSn solder lid seal.

Each above product contains: one package body, one lid, and four power supply decoupling capacitors.

RELATED PRODUCTS

ETF-MLC44	Demountable (solderless) Engineering Test Fixture for the PK-MLC44.

For further information, please contact:

Sales Department
TriQuint Semiconductor, Inc.
Group 700, P.O. Box 4935
Beaverton, OR 97076
(503) 641-4227
FAX: (503) 644-3198

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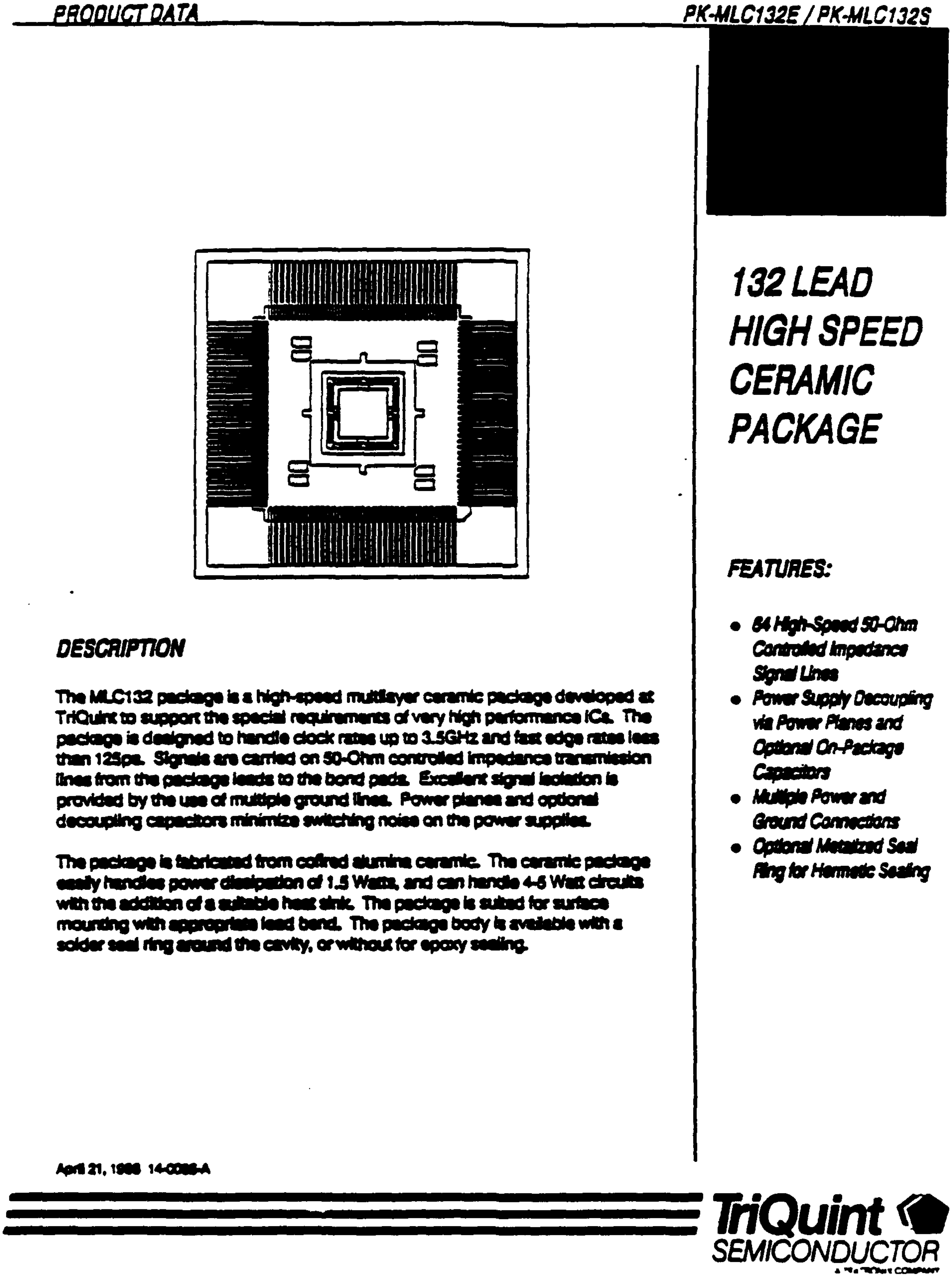
Figure D-23. TriQuint 24/44 Leaded Package; Mechanical Dimensions, Suggested Mounting, Product Designations and Related Products



PRODUCT DATA

PK-MLC132E / PK-MLC132S

132 LEAD HIGH SPEED CERAMIC PACKAGE

DESCRIPTION

The MLC132 package is a high-speed multilayer ceramic package developed at TriQuint to support the special requirements of very high performance ICs. The package is designed to handle clock rates up to 3.5GHz and fast edge rates less than 125ps. Signals are carried on 50-Ohm controlled impedance transmission lines from the package leads to the bond pads. Excellent signal isolation is provided by the use of multiple ground lines. Power planes and optional decoupling capacitors minimize switching noise on the power supplies.

The package is fabricated from cofired alumina ceramic. The ceramic package easily handles power dissipation of 1.5 Watts, and can handle 4-6 Watt circuits with the addition of a suitable heat sink. The package is suited for surface mounting with appropriate lead bend. The package body is available with a solder seal ring around the cavity, or without for epoxy sealing.

FEATURES:

- *64 High-Speed 50-Ohm Controlled Impedance Signal Lines*
- *Power Supply Decoupling via Power Planes and Optional On-Package Capacitors*
- *Multiple Power and Ground Connections*
- *Optional Metalized Seal Ring for Hermetic Sealing*

April 21, 1988 14-0088-A

TriQuint
SEMICONDUCTOR

Figure D-24. TriQuint 64/132 Leaded Package; Description

SIGNAL CONNECTIONS

The illustrations below identify package pin and cavity bond pad connections.

Each signal bond pad connects to one package pin through a 50-Ohm controlled impedance line. All the ground bonding pads are connected together, as are all the pins labeled G. All points labeled G or GND are common with all internal ground planes and the back surface of the package. Each of the two power supplies has four pins, two pairs at opposite corners of the package, which are common with four bonding pads, one on each side of the bond cavity. Both power supplies and ground are brought to pads beside the bond cavity where optional decoupling capacitors may be added.

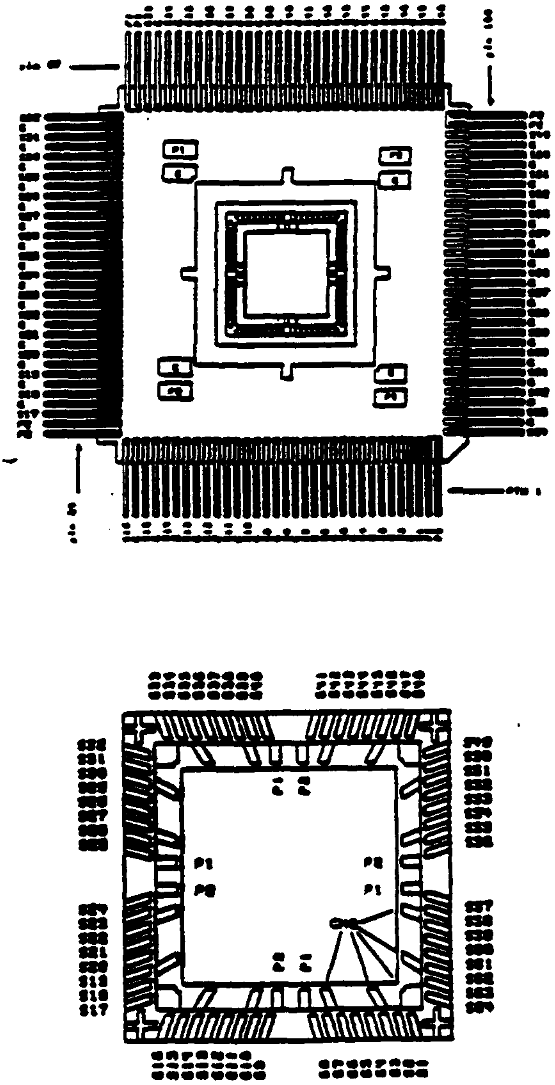
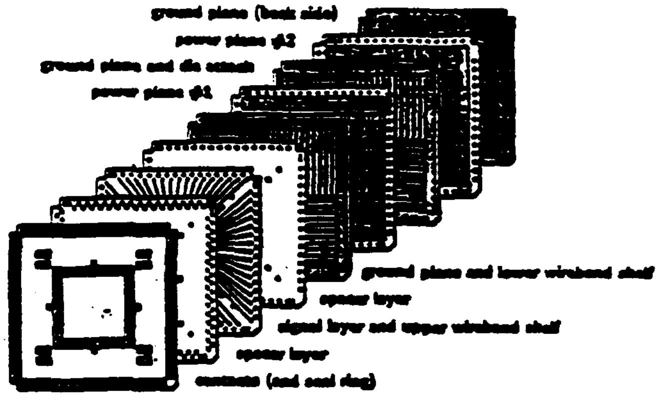


Figure D-25. TriQuint 64/132 Leaded Package;Signal Connections

PACKAGE STRUCTURE

The package is constructed of several metal layers with a layer of ceramic between each pair of metal layers. This structure gives a controlled impedance environment for the signal lines. The figure below shows a representation of the layered structure.


ground plane (back side)
power plane #2
ground plane and die attach
power plane #1
ground plane and lower wirebond shelf
spacer layer
signal layer and upper wirebond shelf
spacer layer
contacts (and seal ring)

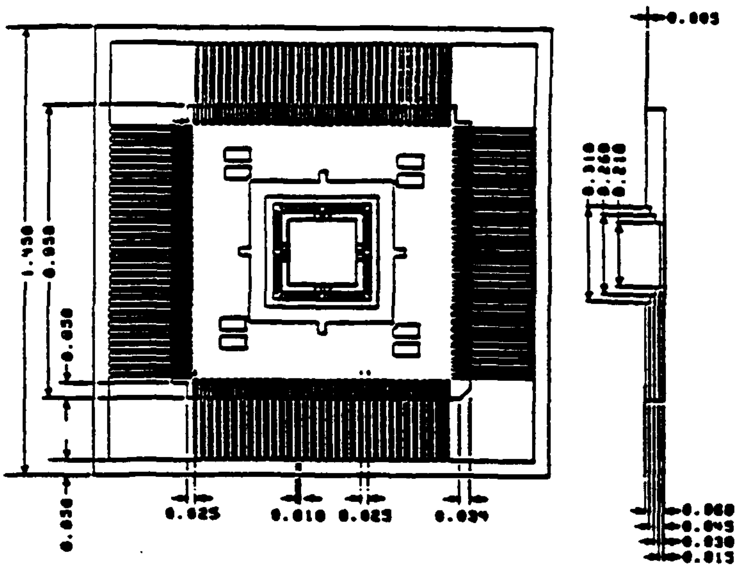
SPECIFICATIONS

Materials:	Body	Alumina Ceramic
	Leads	Kovar
	Metalization	Tungsten/Nickel/Gold
Dimensions:	Body Size	0.950 x 0.950 x 0.080 inches
	Die Cavity Size	0.210 x 0.210 inch
	Max Recommended Die Size	0.170 x 0.170 inch
Leads:	Spacing	0.025 inch
	Lead Count	132
	Signal Leads	64
	Ground Leads	60
	Power Leads	8 (4 per supply)
Misc.	Power Plane Capacitance (each supply)	350 pF
	Pads for Decoupling Capacitor	2/supply
	Recommended Chip Capacitor size	0.050 x 0.080
	Die-to-Case Thermal Impedance(1)	5 °C/Watt

Note (1): The thermal impedance value shown is typical for a 0.160 x 0.160 die. Use thermal impedance numbers with caution; operating temperature is a complex function of die size, circuit layout, and other factors.

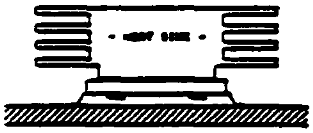
Figure D-26. TriQuint 64/132 Leaded Package; Structure and Specifications

MECHANICAL DIMENSIONS



SUGGESTED MOUNTING

Bending the leads in a gull-wing fashion as shown allows the package to be surface mounted face down. In this way, a heat sink can be mounted on the back of the package, physically close to the die.



PRODUCT DESIGNATIONS

PK-MLC132E	Package body without seal ring, for use with Epoxy seal.
PK-MLC132S	Package body with gold metalized seal ring, for use with AuSn solder lid seal.

Each above product contains: one package body, one lid, and four power supply decoupling capacitors.

RELATED PRODUCTS

ETF-MLC132	Demountable (solderless) Engineering Test Fixture for the PK-MLC132.

For further information please contact:
Sales Department
TriQuint Semiconductor, Inc.
Group 700, P.O. Box 4935
Beaverton, OR 97076
(503) 641-4227
FAX: (503) 644-3198

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Figure D-27. TriQuint 64/132 Leaded Package; Mechanical Dimensions, Suggested Mounting, Product Designations and Related Products

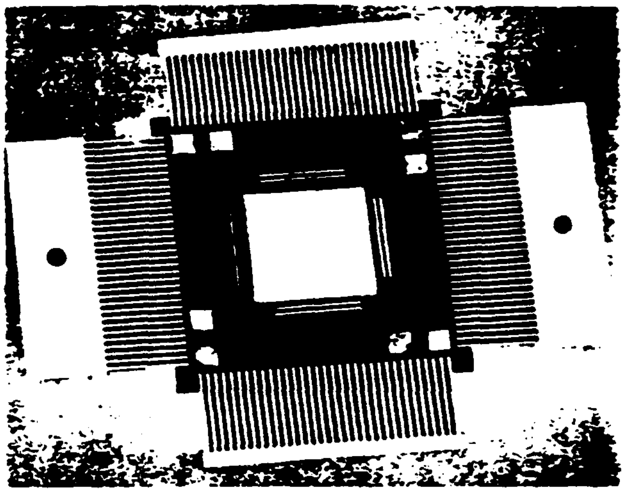
Bulletin 103

Leaded Polyimide Chip Carriers

High Performance Series (PHIP)
High I/O Count Series (PHIL)

Features

- **Microstrip Construction**
  ...for High Performance Circuit Applications
- **High Interconnect Densities**
  with 132 and 164 Leads
- **IC Bonding Pads on 0.010" Centers and I/O Leads on 0.025" Centers**
  ...to Facilitate Interconnections
- **Controlled Impedance (PHIP Only)**
  ...50 Ohm Standard. 25 to 75 Ohm Available; for low transmission and return loss and high system performance
- **Integral Heat Sink**
  ...Die Bonded Directly to Heat Sink for Cooler Operation and Higher Reliability
- **Provisions for Four Capacitors Directly on the Chip Carrier**
  ...for Improved Decoupling



Augat Microtec offers high performance chip carriers (PHIP Series), employing the unique Copper-Polyimide "additive" process ideally suited to applications involving CMOS, ECL, GaAs and other semiconductor technologies which require high density interconnect, thermal management and controlled impedance characteristics. These carriers provide high performance and improved environmental protection, and feature superior electrical characteristics, as well as JEDEC conformance.

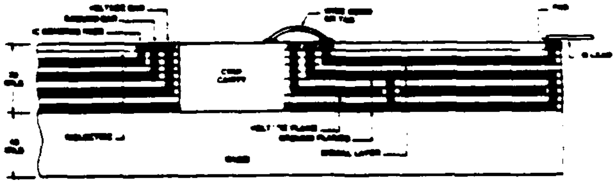
Also available is a companion series (PHIL) of chip carriers, for applications requiring only high I/O densities. These more economical units differ from the high performance (PHIP) series in that ground planes, controlled impedance signal lines, and provisions for integral capacitors have been deleted.

Augat Microtec Polyimide Chip Carriers utilize the firm's "additive" process, which facilitates customization to fit virtually any special high speed application. A wide range of signal, power and ground layers, with appropriate via layers, may be designed into the chip carrier.

Performance Specifications

Dielectric Constant	3.8
Capacitance	<1 pf
Resistance	<30 mΩ
Inductance	<2 nh

MICROSTRIP CONSTRUCTION



To Order, specify...

PHIP Part No.	PHIL Part No.	Leads	I/O	O.D.	Cavity	Z_0 (Ω)	Gnd	Co-Planar	Base** Material
P132-001		132	025	950" x 950"	400	50	Yes	Yes	Copper
	L132-001	132	025	950" x 950"	400	N/A	N/A	N/A	Copper
P164-001		164	025	1 150" x 1 150"	400	50	Yes	Yes	Copper
	L164-001	164	025	1 150" x 1 150"	400	N/A	N/A	N/A	Copper

Notes:** Optional Base Materials
— BEO
— Aluminum
— Copper/Invar/Copper

AUGAT® MICROTEC

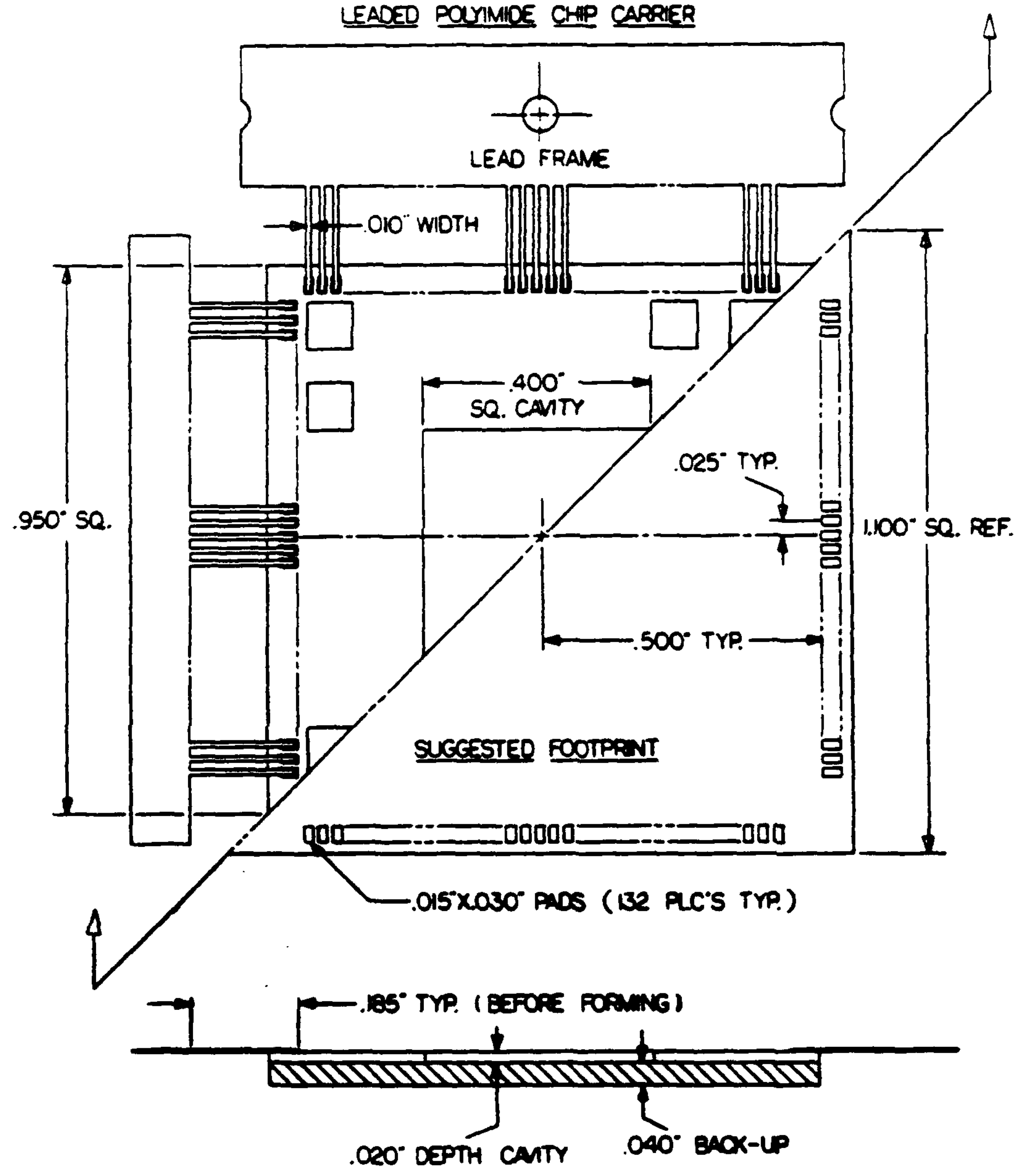
Quality and Innovation

2520 Turquoise Circle, Newbury Park, CA 91320-1211 • (805) 498-9643
.. 86

Figure D-28. Rogers 116/132 and 148/164; Features and Specifications

AUGAT MICROTEC

P132-001


LEADED POLYIMIDE CHIP CARRIER
LEAD FRAME
.010" WIDTH
.400" SQ. CAVITY
.025" TYP.
.950" SQ.
1.100" SQ. REF.
.500" TYP.
SUGGESTED FOOTPRINT
.015"X.030" PADS (132 PLC'S TYP.)
.185" TYP. (BEFORE FORMING)
.020" DEPTH CAVITY
.040" BACK-UP

2520 TURQUOISE CIRCLE, NEWBURY PARK, CALIFORNIA 91320 (805) 498-9643

Figure D-29. Rogers 116/132 Leaded Package, P-132-001; Mechanical Dimensions

WIRING DIAGRAM
FOR
P132-001

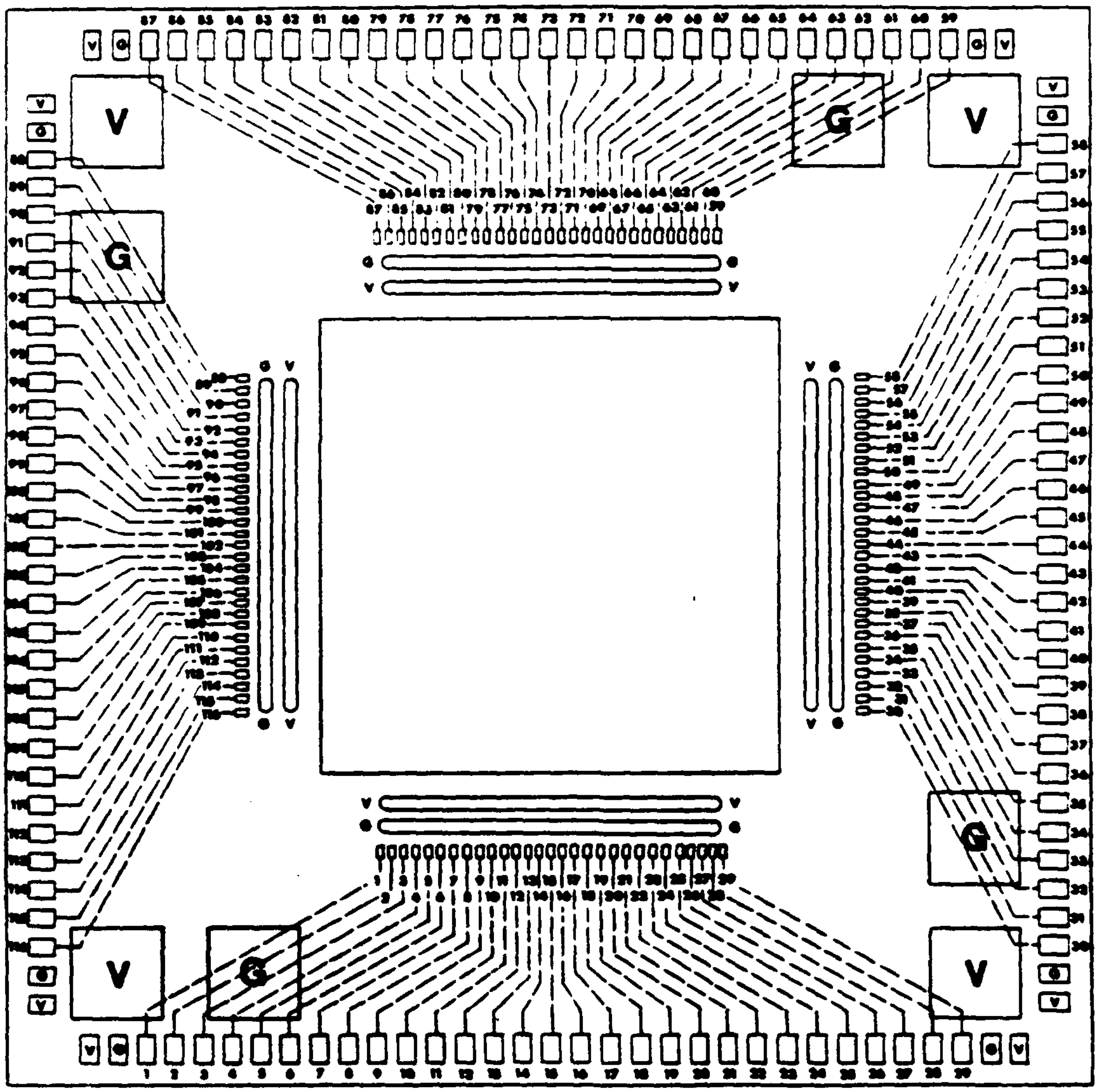
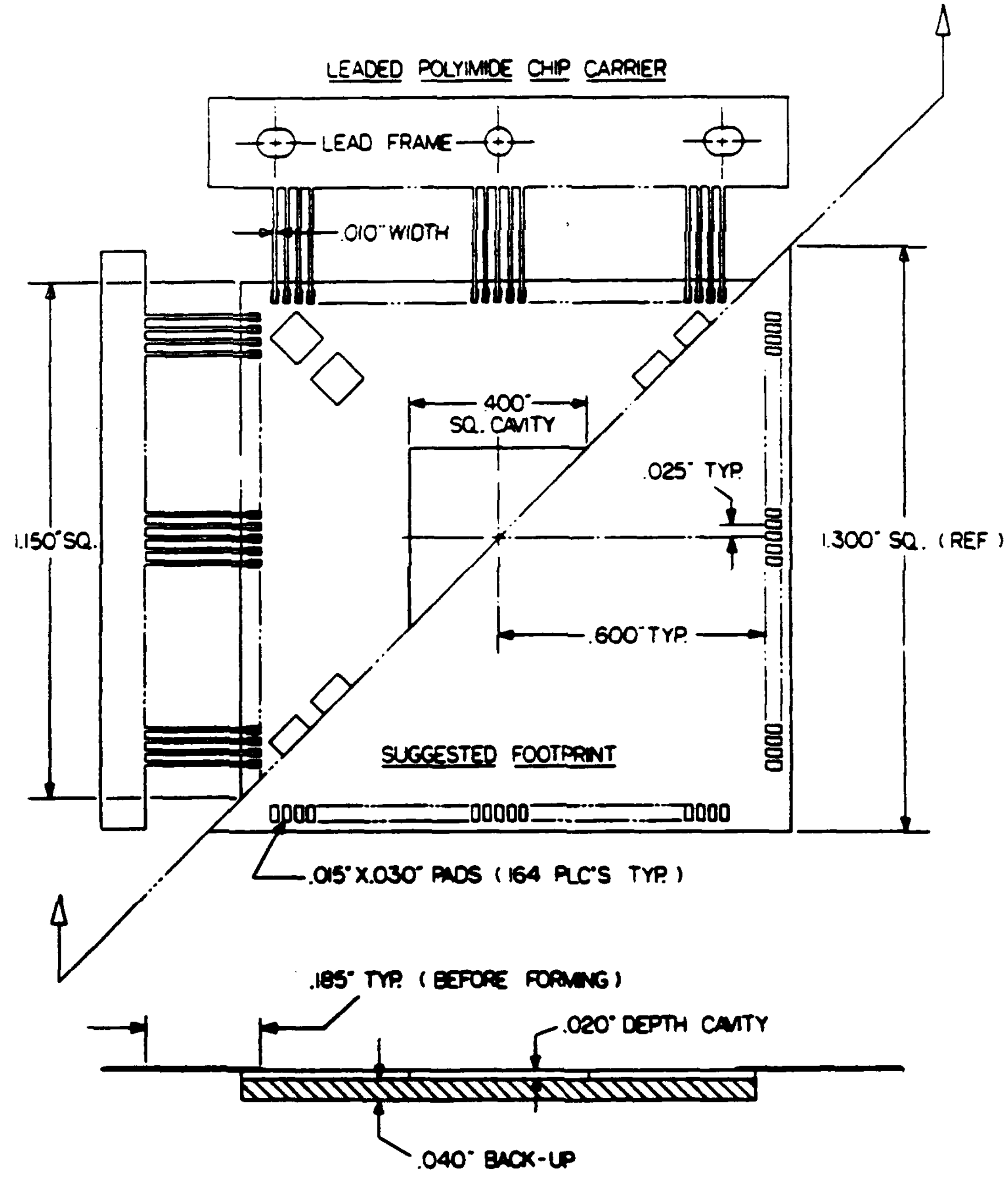

V
G
V
G
V
G
V
G
87 86 85 84 83 82 81 80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29

Figure D-30. Rogers 116/132 Leaded Package, P-132-001; Wiring Diagram

AUGAT MICROTEC

P164-001


LEADED POLYIMIDE CHIP CARRIER
LEAD FRAME
.010" WIDTH
.400"
SQ. CAVITY
.025" TYP.
1.150" SQ.
1.300" SQ. (REF)
.600" TYP.
SUGGESTED FOOTPRINT
.015" X .030" PADS (164 PLC'S TYP.)
.185" TYP. (BEFORE FORMING)
.020" DEPTH CAVITY
.040" BACK-UP

2520 TURQUOISE CIRCLE, NEWBURY PARK, CALIFORNIA 91320 (805) 498-9643

Figure D-31. Rogers 148/164 Leaded Package, P-164-001; Mechanical Dimensions

WIRING DIAGRAM
FOR
P164-001

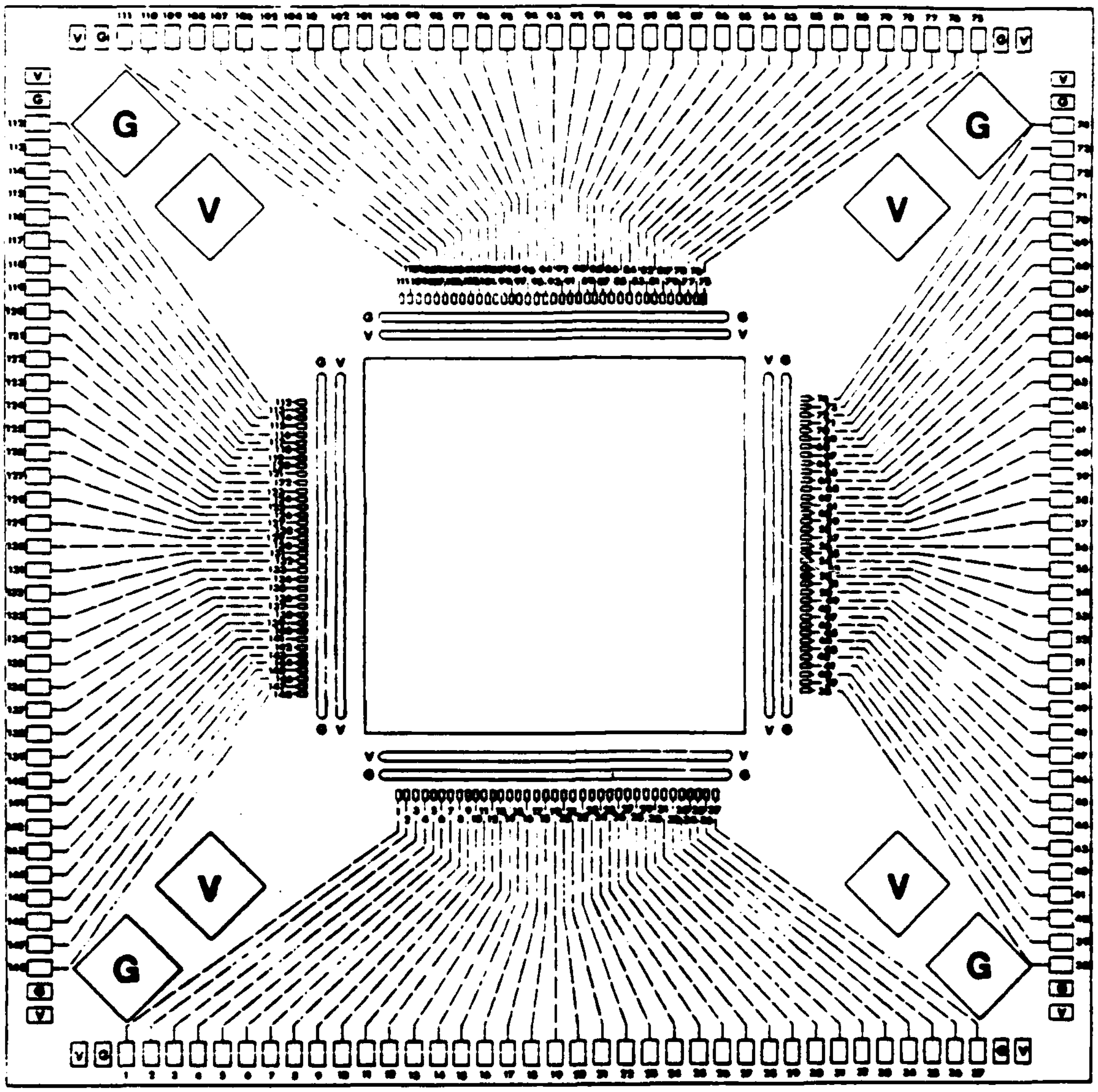
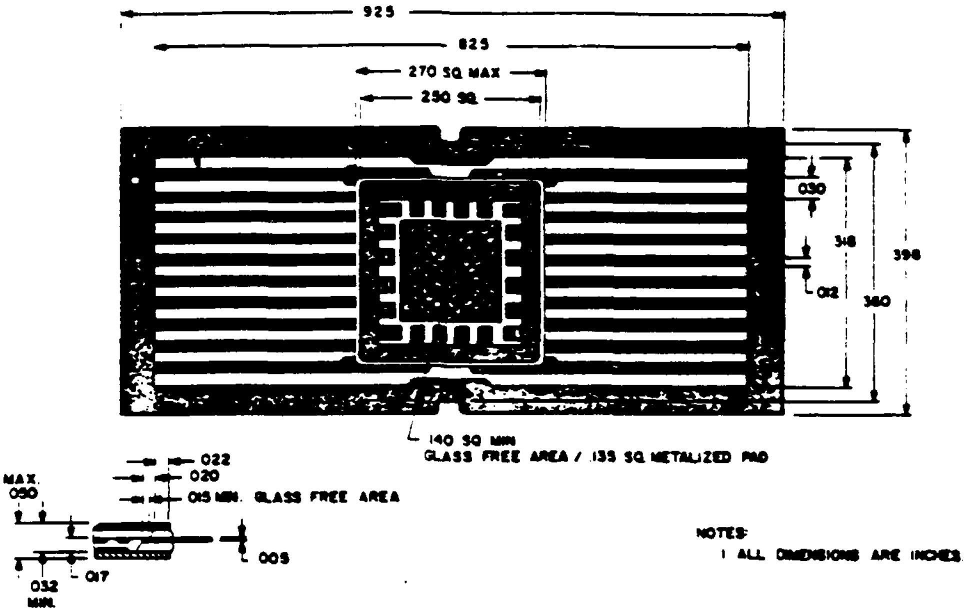


Figure D-32. Rogers 148/164 Leaded Package, P-164-001; Wiring Diagram

ELECTRONIC PACKAGE DIVISION
168 EAST BACON ST., P.O. BOX 1597
PLAINVILLE, MA 02762

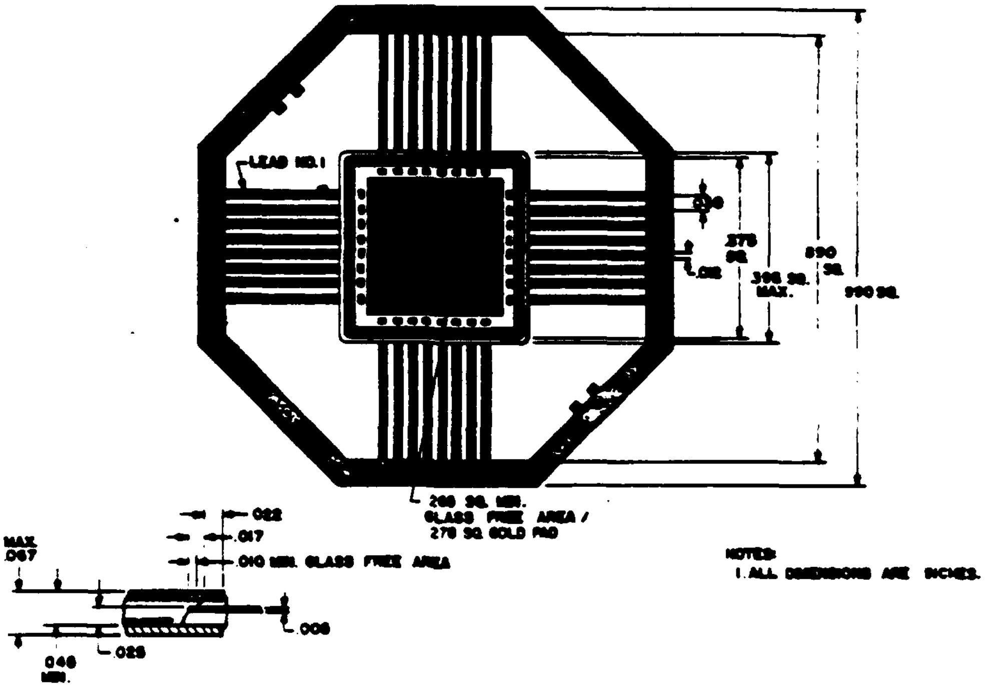
MINI-SYSTEMS, INC.

(617) 695-2000
TWX (710) 348-0564


925
825
270 SQ MAX
250 SQ
030
348
398
012
360
140 SQ MIN
GLASS FREE AREA / .135 SQ METALIZED PAD
022
020
015 MIN. GLASS FREE AREA
MAX.
050
005
017
032
MIN.

NOTES:
1. ALL DIMENSIONS ARE INCHES.

METALIZED CERAMIC BASE	20 LEADS	.140x.140	3H20CM


LEAD NO.1
.030
.012
275 SQ.
305 SQ. MAX.
890 SQ.
990 SQ.
265 SQ. MIN.
GLASS FREE AREA /
275 SQ GOLD PAD
.022
.017
.010 MIN. GLASS FREE AREA
MAX.
.067
.005
.025
.040
MIN.

NOTES:
1. ALL DIMENSIONS ARE INCHES.

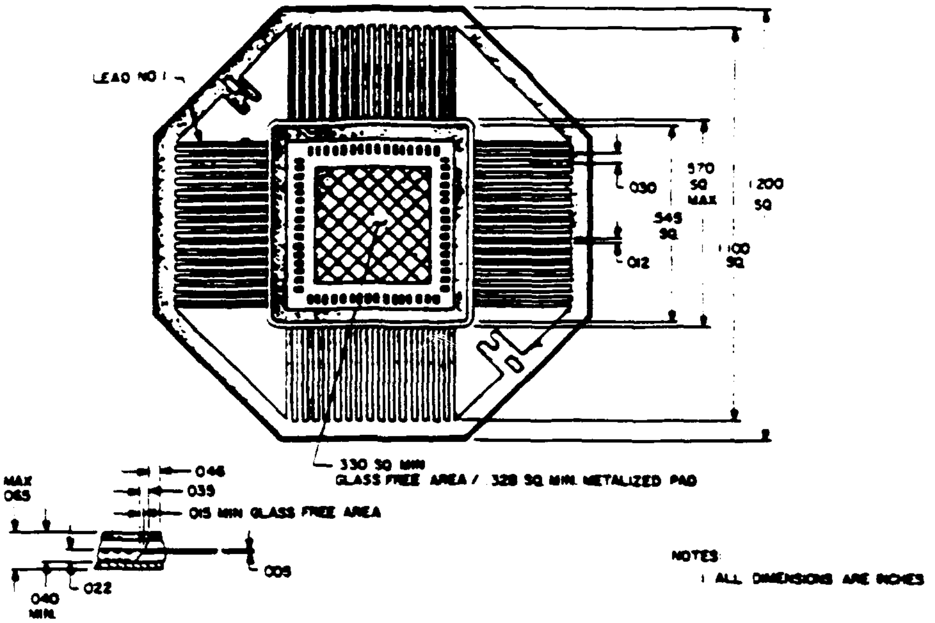
METALIZED CERAMIC BASE	32 LEADS	.265x.265	3LN32CM

Figure D-33. MSI 20/20 (Upper), MSI 32/32 (Lower)

ELECTRONIC PACKAGE DIVISION
168 EAST BACON ST P O BOX 1597
PLAINVILLE MA 02762

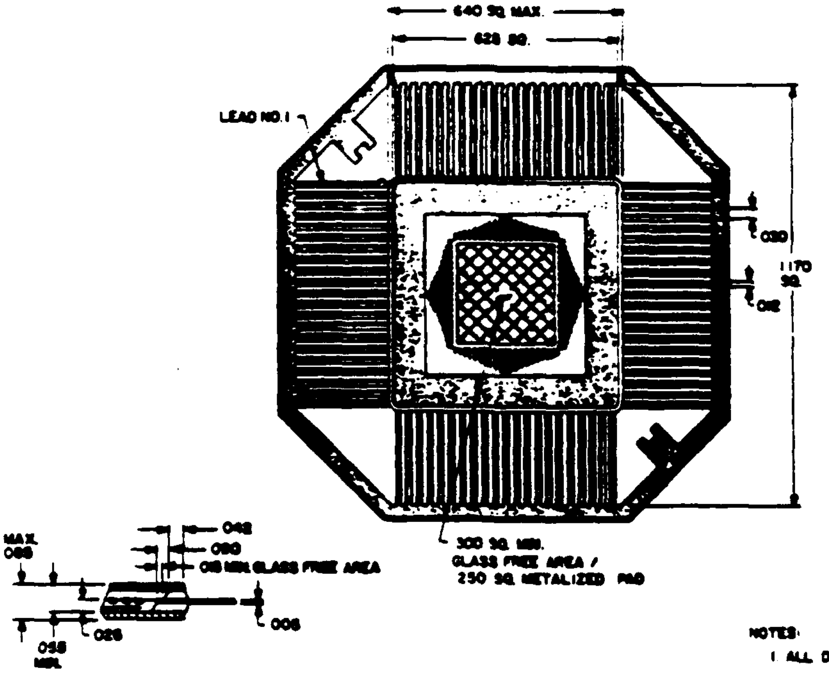
MSI
MINI-SYSTEMS, INC.

(617) 695-2000
TWX (710) 348-0564


LEAD NO 1
.030
.570
SQ
MAX
1.200
SQ
.545
SQ
1.100
SQ
.012
.330 SQ MIN
GLASS FREE AREA / .328 SQ MIN METALIZED PAD
MAX
.065
.046
.035
.015 MIN GLASS FREE AREA
.005
.022
.040
MIN

NOTES:
1 ALL DIMENSIONS ARE INCHES

METALIZED CERAMIC BASE	64 LEADS	.330 x.330	3T64CM


.640 SQ MAX.
.628 SQ.
LEAD NO.1
.030
1.170
SQ.
.012
.300 SQ. MIN.
GLASS FREE AREA /
.250 SQ. METALIZED PAD
MAX.
.085
.042
.030
.015 MIN GLASS FREE AREA
.005
.028
.058
MIN.

NOTES:
1. ALL DIMENSIONS ARE INCHES.

METALIZED CERAMIC BASE	84 LEADS	.300x.300	3U84CM

Figure D-34. MSI 64/64 (Upper), MSI 84/84 (Lower)

Drawings for Packages

Described in Table D-2

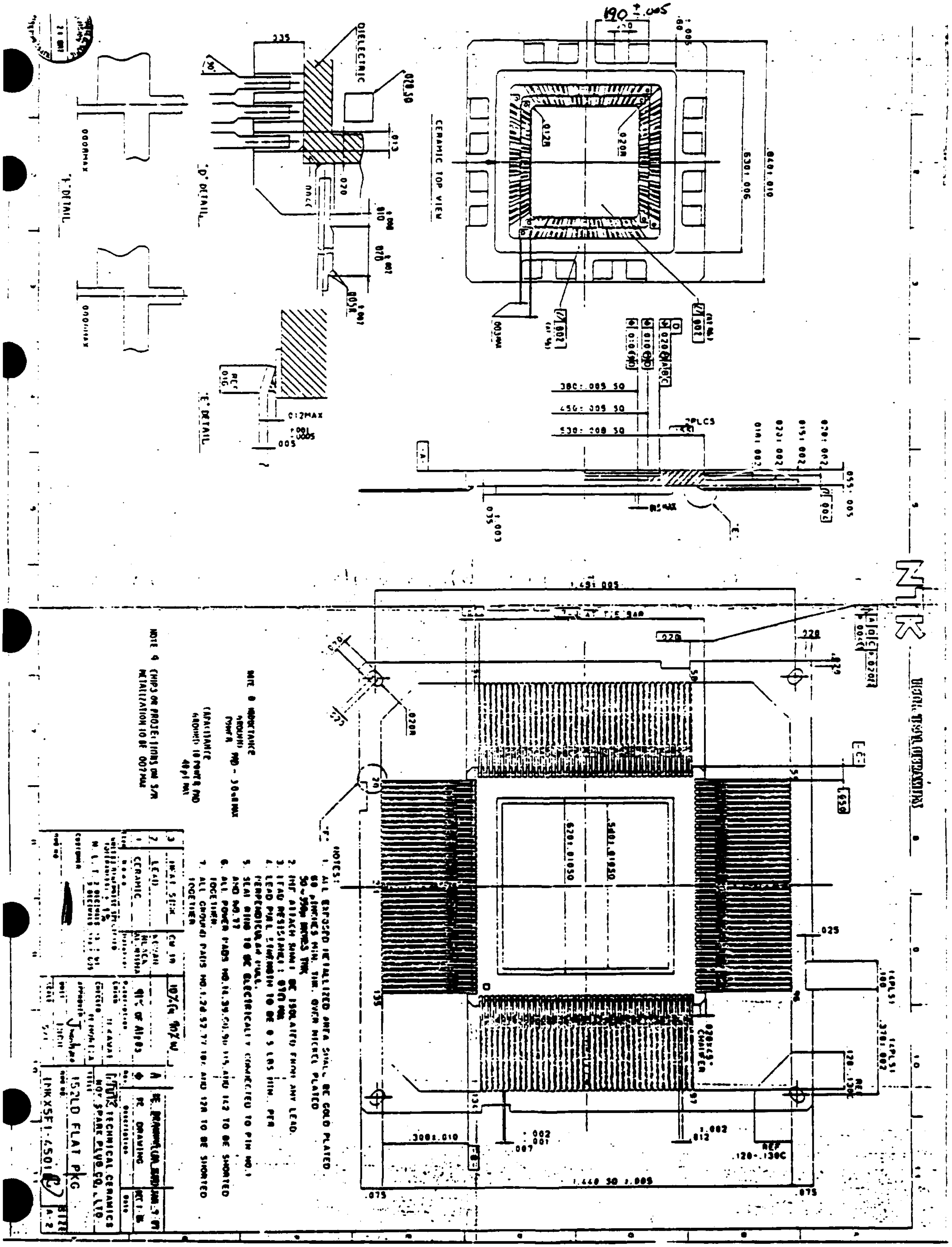

190 ±.005
CERAMIC TOP VIEW
DIELECTRIC
"D" DETAIL
"E" DETAIL
"F" DETAIL
NTK
1.491 .005
1.440 SQ ±.005
.300±.010
.025
.075
NOTES:
1. ALL EXPOSED METALLIZED AREA SHALL BE GOLD PLATED.
2. DIE ATTACH SHALL BE ISOLATED FROM ANY LEAD.
5. SEAL RING TO BE ELECTRICALLY CONNECTED TO PIN NO.1
6. ALL POWER PADS
7. ALL GROUND PADS
CERAMIC
LEAD
91% OF Al2O3
DRAWING
NTK TECHNICAL CERAMICS
NGK SPARK PLUG CO., LTD.
152LD FLAT PKG
NKX5F1-4501C
A-2

Figure D-35. NTK 152 Leaded Package

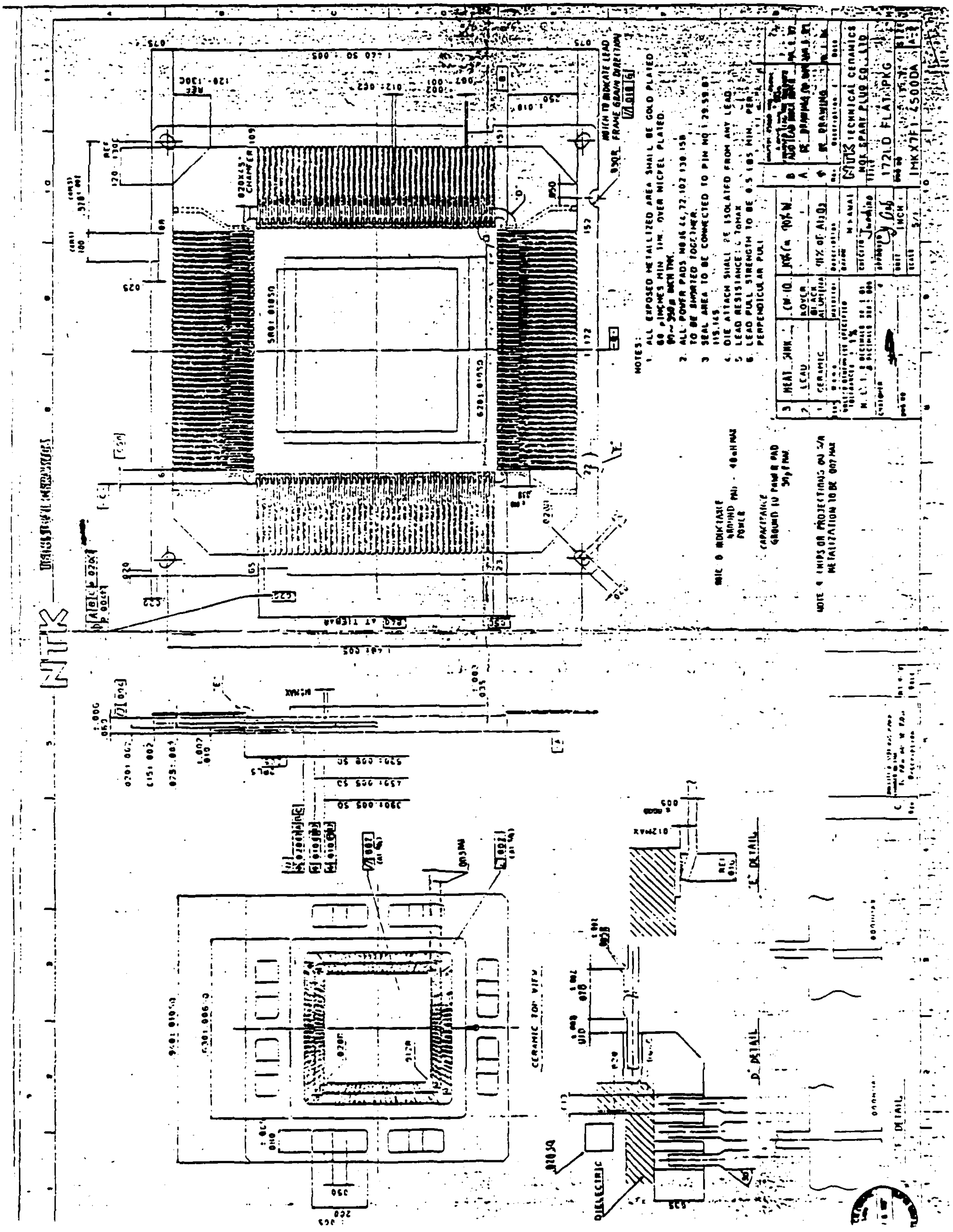

NTK
CERAMIC TOP VIEW
DIELECTRIC
'D' DETAIL
'E' DETAIL
NOTES:
1. ALL EXPOSED METALLIZED AREA SHALL BE GOLD PLATED
2. ALL POWER PADS
3. SEAL AREA TO BE CONNECTED TO PIN
4. DIE ATTACH SHALL BE ISOLATED FROM ANY LEAD
5. LEAD RESISTANCE
6. LEAD PULL STRENGTH
HEAT SINK
LEAD
CERAMIC
NTK TECHNICAL CERAMICS
172LD FLAT PKG
IMKX7F1-4500DA

Figure D-36. NTK 172 Leaded Package

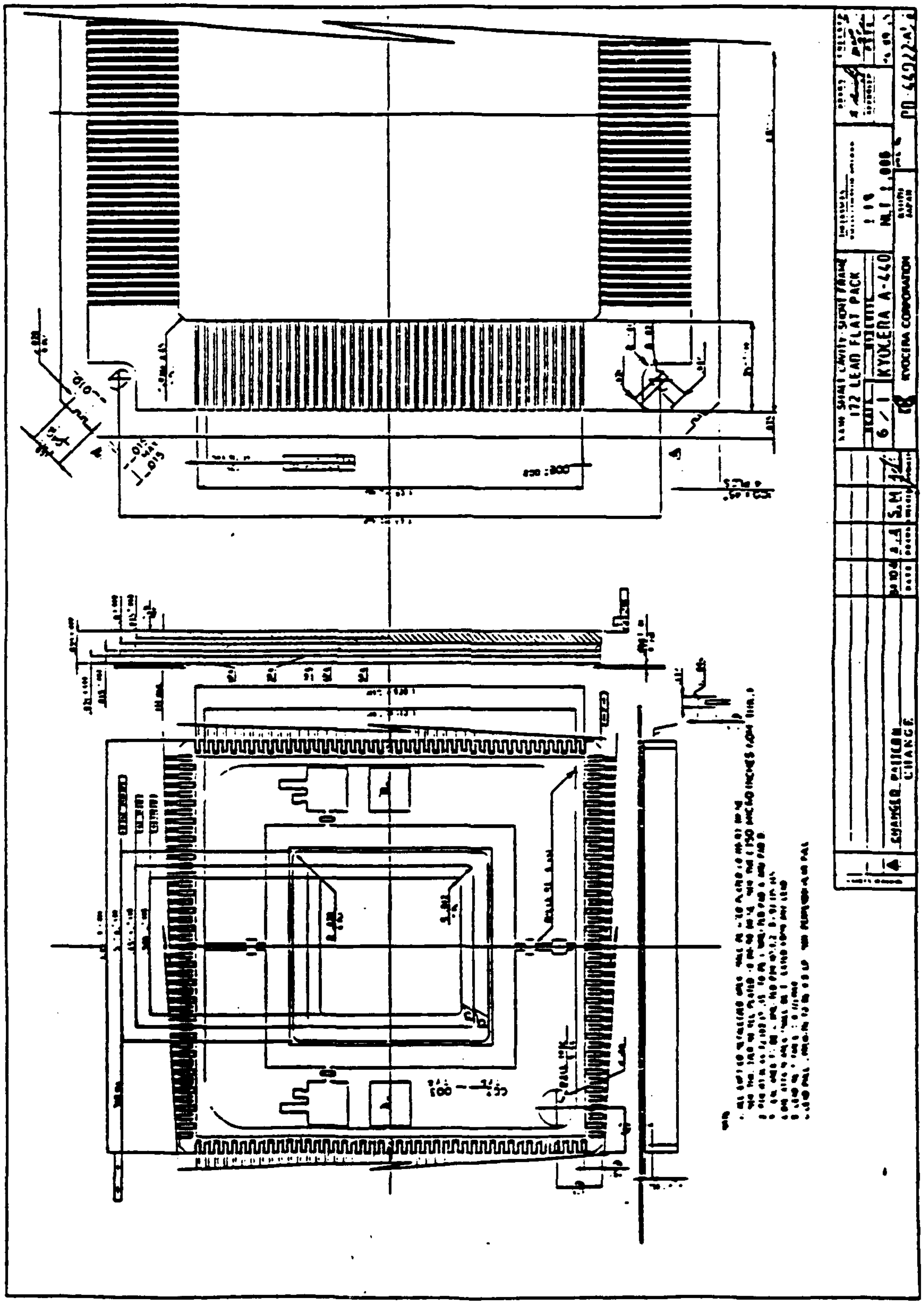

172 LEAD FLAT PACK
6 / 1
KYOCERA A-440
KYOCERA CORPORATION
NL 1 1,000
JAPAN
S.M
CHANGED PATTERN
CHANGE

Figure D-37. Kyocera 172 Leaded Package

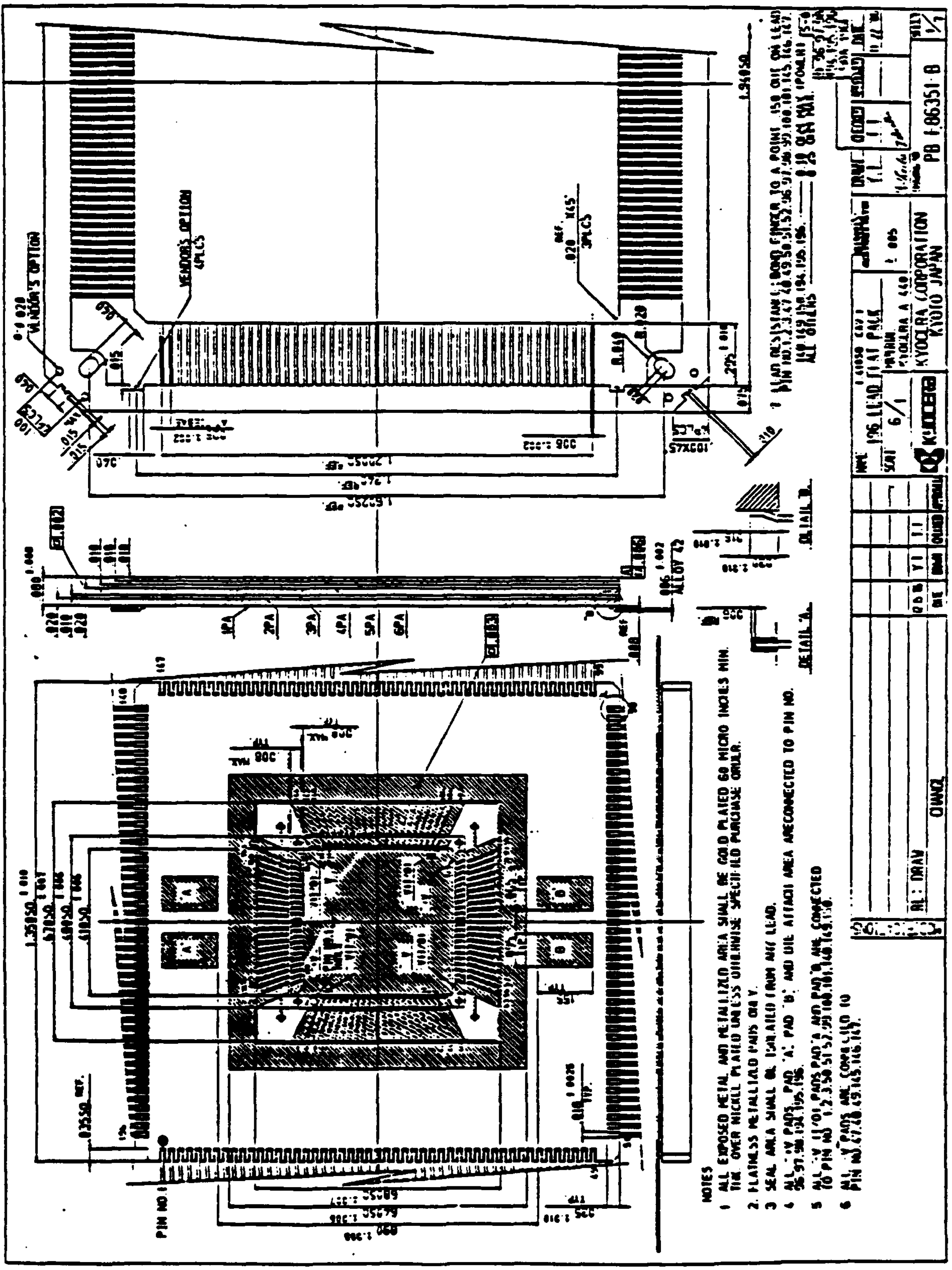


Figure D-38. Kyocera 196 Leaded Package

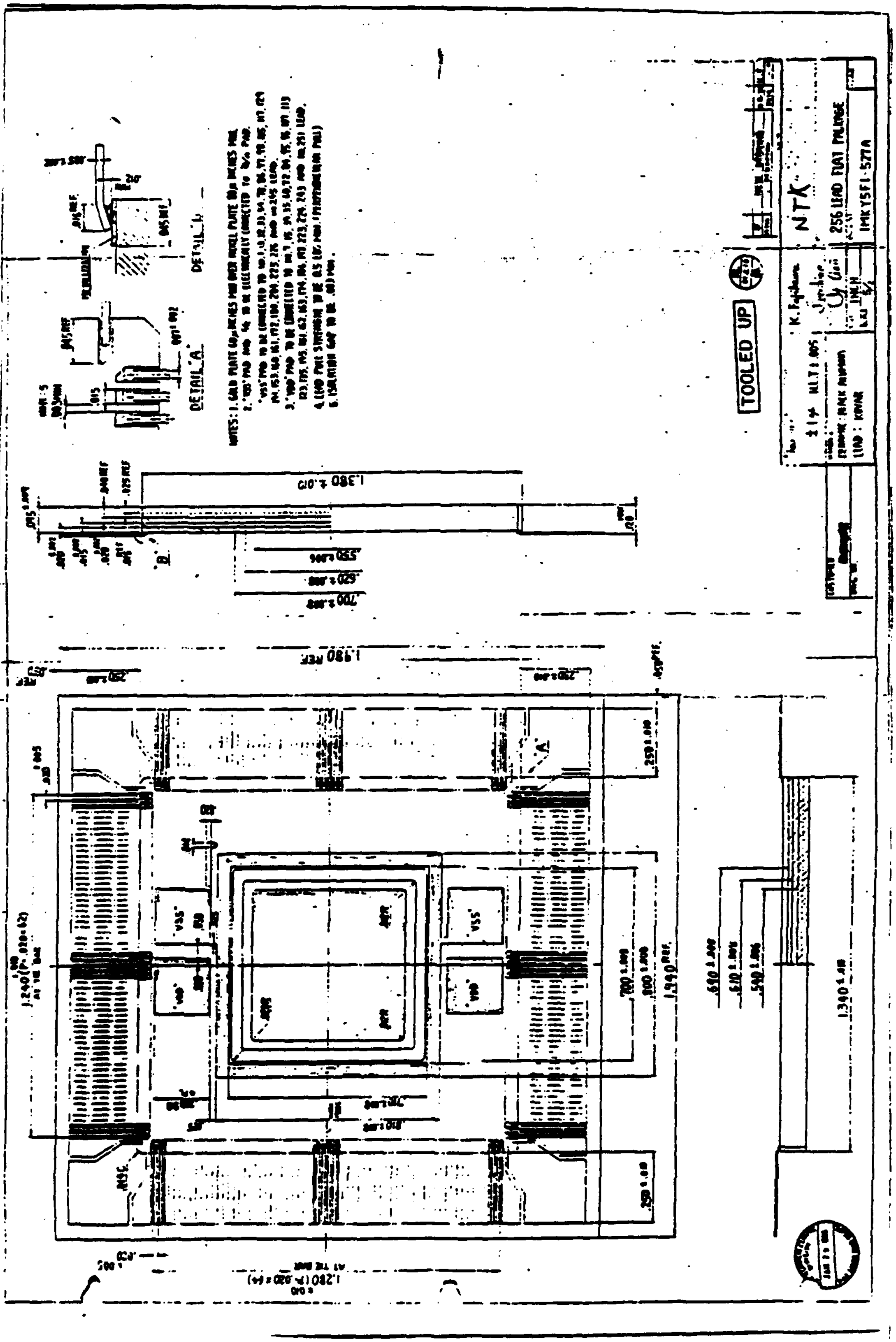
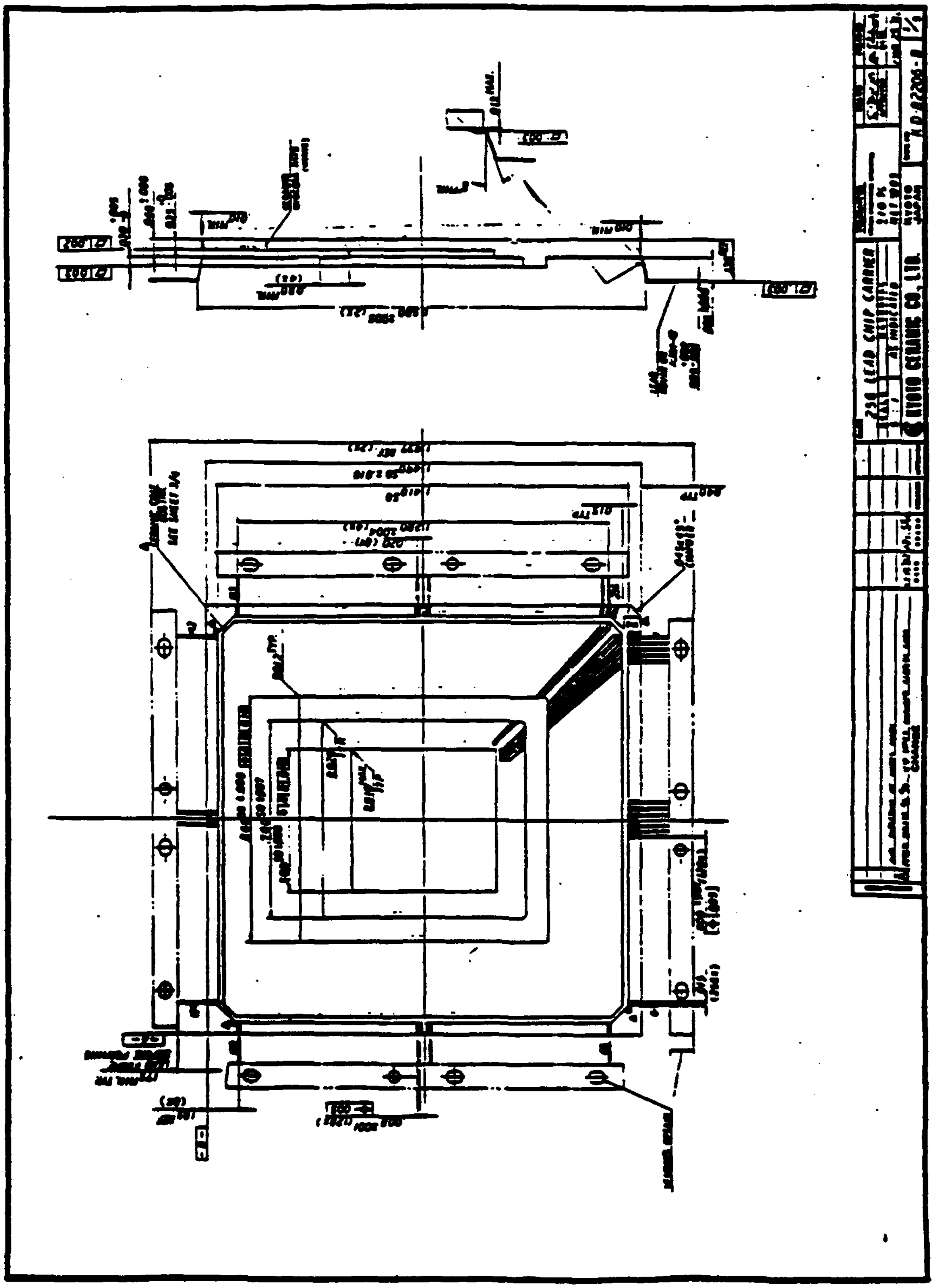

TOOLED UP
NTK
256 LEAD FLAT PACKAGE
DETAIL 'A'
DETAIL 'B'
1.380 ±.015
1.980 REF
1.940 REF.
1.340 ±.010
VSS
VDD

Figure D-39. NTK 256 Leaded Package


256 LEAD CHIP CARRIER
KYOCERA CERAMIC CO., LTD.
KYOTO JAPAN
1/1

Kyocera

Figure D-40. Kyocera 256 Leaded Package

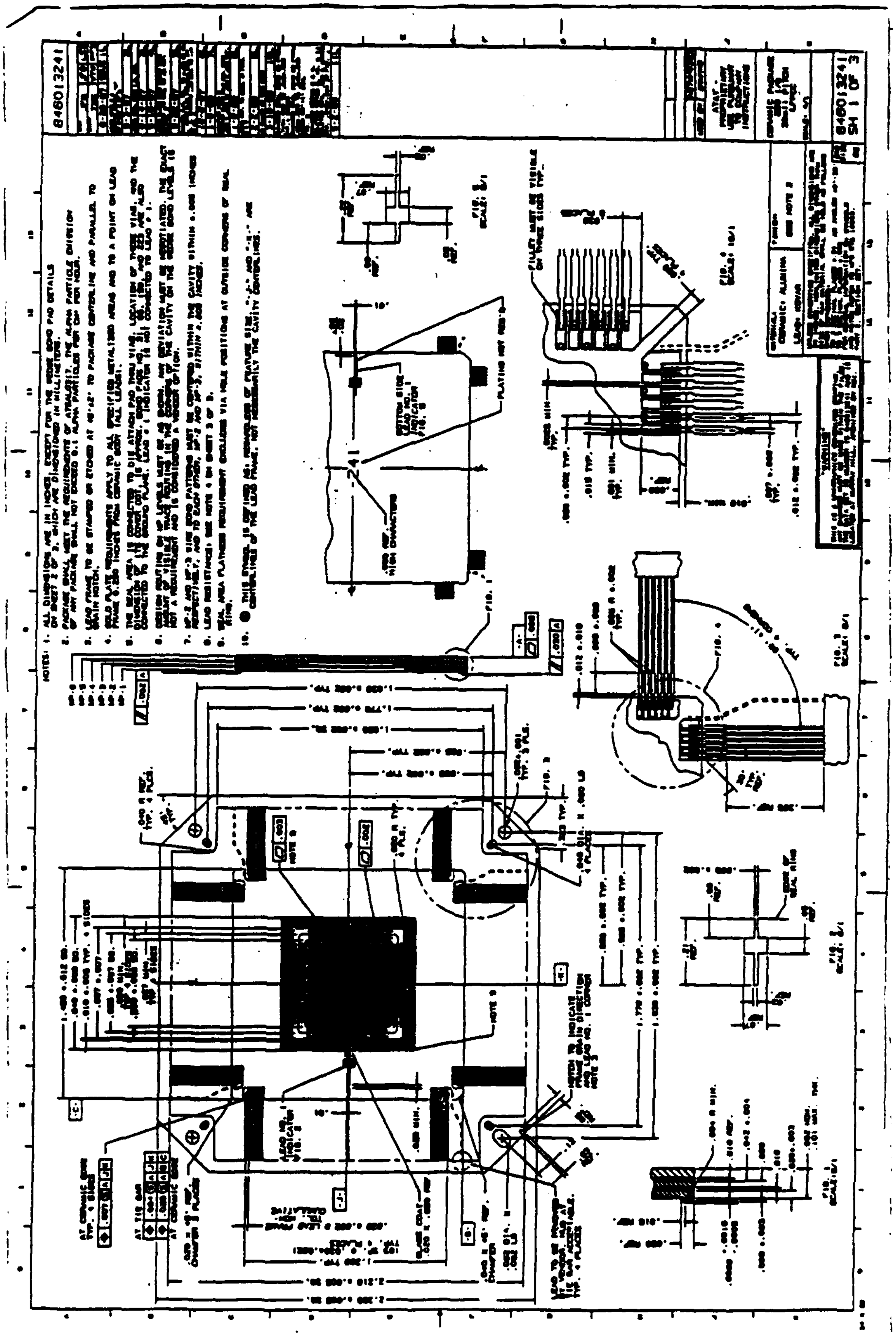


Figure D-41. NTK 256 Leaded Package; AT&T Design, Mechanical Dimensions

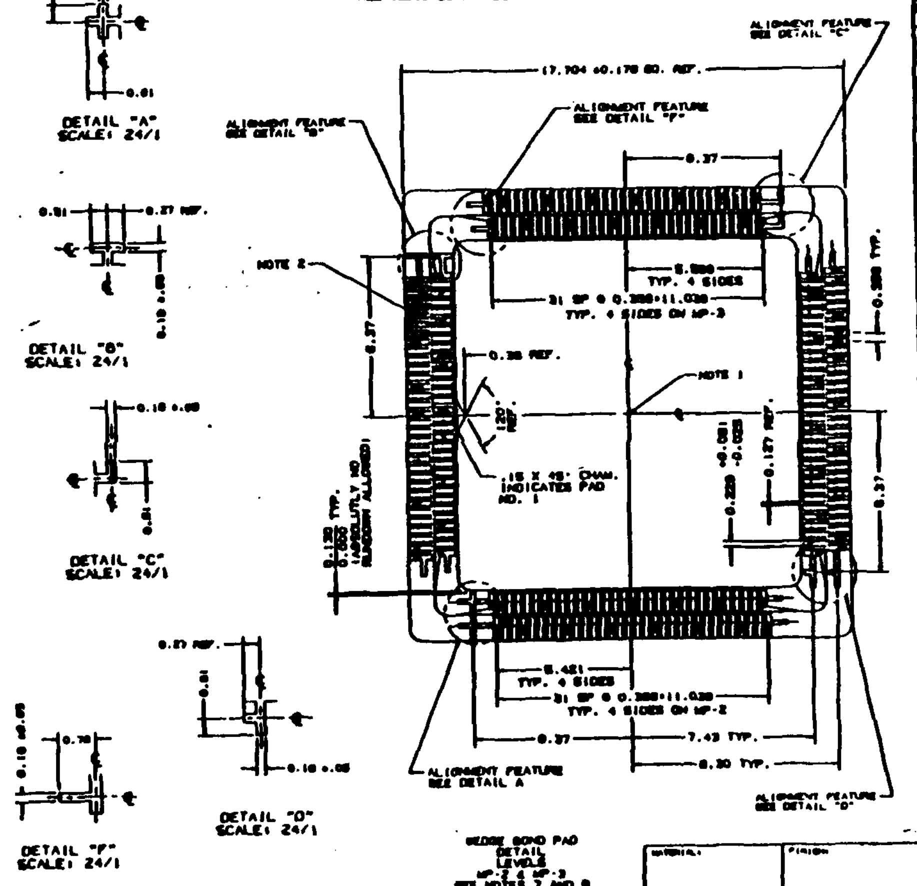
WEDGE BOND PAD/PACKAGE LEAD INTERCONNECTION PLAN

WEDGE BOND PAD NO.	256 PKG LEAD NO.	WEDGE BOND PAD NO.	256 PKG LEAD NO.	WEDGE BOND PAD NO.	256 PKG LEAD NO.	WEDGE BOND PAD NO.	256 PKG LEAD NO.
1	1	65	65	129	129	193	193
2	2	66	66	130	130	194	194
3	3	67	67	131	131	195	195
4	4	68	68	132	132	196	196
5	VSS	69	VSS	133	VSS	197	VSS
6	6	70	70	134	134	198	198
7	7	71	71	135	135	199	199
8	8	72	72	136	136	200	200
9	9	73	73	137	137	201	201
10	10	74	74	138	138	202	202
11	11	75	75	139	139	203	203
12	12	76	76	140	140	204	204
13	13	77	77	141	141	205	205
14	14	78	78	142	142	206	206
15	VDD	79	VSS	143	VDD	207	VDD
16	16	80	80	144	144	208	208
17	17	81	81	145	145	209	209
18	18	82	82	146	146	210	210
19	19	83	83	147	147	211	211
20	20	84	84	148	148	212	212
21	21	85	85	149	149	213	213
22	22	86	86	150	150	214	214
23	VSS	87	VDD	151	VSS	215	VSS
24	24	88	88	152	152	216	216
25	25	89	89	153	153	217	217
26	26	90	90	154	154	218	218
27	27	91	91	155	155	219	219
28	28	92	92	156	156	220	220
29	29	93	93	157	157	221	221
30	30	94	94	158	158	222	222
31	VSS	95	VSS	159	VSS	223	VSS
32	32	96	96	160	160	224	224
33	VDD	97	VDD	161	VDD	225	VDD
34	34	98	98	162	162	226	226
35	35	99	99	163	163	227	227
36	36	100	100	164	164	228	228
37	37	101	101	165	165	229	229
38	38	102	102	166	166	230	230
39	39	103	103	167	167	231	231
40	40	104	104	168	168	232	232
41	41	105	VSS	169	VSS	233	VSS
42	42	106	106	170	170	234	234
43	VSS	107	107	171	171	235	235
44	44	108	108	172	172	236	236
45	45	109	109	173	173	237	237
46	46	110	110	174	174	238	238
47	47	111	111	175	175	239	239
48	48	112	112	176	176	240	240
49	49	113	VSS	177	VSS	241	VDD
50	50	114	114	178	178	242	242
51	VSS	115	115	179	179	243	243
52	52	116	116	180	180	244	244
53	53	117	117	181	181	245	245
54	54	118	118	182	182	246	246
55	55	119	119	183	183	247	247
56	56	120	120	184	184	248	248
57	57	121	121	185	185	249	249
58	58	122	122	186	186	250	250
59	VDD	123	VDD	187	VDD	251	VSS
60	60	124	124	188	188	252	252
61	61	125	125	189	189	253	253
62	62	126	126	190	190	254	254
63	63	127	127	191	191	255	255
64	64	128	128	192	192	256	256

METRIC

NOTES:

1. CENTERLINE TO BE CONSIDERED, IN THIS FIGURE, THE CENTERLINE OF EACH PATTERNED LAYER INDIVIDUALLY; HOWEVER, THE INTERDIGITATED LAYER PATTERN ALIGNMENT IS PER NOTE 8 ON SHEET 1.
2. SCREENED METALIZATION AS SHOWN IS TYPICAL FOR ALL WEDGE BOND PADS AND ROUTES.


DETAIL "A"
SCALE: 24/1
0.18 ±0.05
0.27 REF.
0.01
DETAIL "B"
SCALE: 24/1
0.01
0.27 REF.
0.18 ±.05
DETAIL "C"
SCALE: 24/1
0.18 ±.05
0.01
DETAIL "D"
SCALE: 24/1
0.27 REF.
0.01
0.18 ±.05
DETAIL "F"
SCALE: 24/1
0.18 ±0.05
0.70
17.704 ±0.178 SQ. REF.
ALIGNMENT FEATURE SEE DETAIL "C"
ALIGNMENT FEATURE SEE DETAIL "F"
ALIGNMENT FEATURE SEE DETAIL "B"
ALIGNMENT FEATURE SEE DETAIL A
ALIGNMENT FEATURE SEE DETAIL "D"
NOTE 2
NOTE 1
6.37
5.588 TYP. 4 SIDES
31 SP @ 0.388=11.038 TYP. 4 SIDES ON MP-3
0.38 REF.
120° REF.
.15 X 45° CHAM. INDICATES PAD NO. 1
0.130 TYP. 0.000 (ABSOLUTELY NO RUNDOWN ALLOWED)
0.229 +0.051 -0.025
0.127 REF.
0.388 TYP.
5.421 TYP. 4 SIDES
31 SP @ 0.388=11.038 TYP. 4 SIDES ON MP-2
7.43 TYP.
6.30 TYP.

GND: 5, 23, 31, 43, 51, 69, 79, 95, 105, 113, 133, 151, 159, 169, 177, 197, 215, 223, 233, 251

PWR: 15, 33, 59, 87, 97, 123, 143, 161, 187, 207, 225, 241

WEDGE BOND PAD
DETAIL
LEVELS
MP-2 & MP-3
SEE NOTES 7 AND 8
ON SHEET 1 OF 3

"WARNING"

MATERIAL:

FINISH:

AT&T - PROPRIETARY
USE PURSUANT TO COMPANY INSTRUCTIONS

CERAMIC PACKAGE
256 I/O
SMALL PITCH
LPPQC

SCALE: 10/1

846013241
SH 2 OF 3

Figure D-42. NTK 256 Leaded Package; AT&T Design, Pin Assignment